

P-Channel 100-V (D-S) 175 °C MOSFET

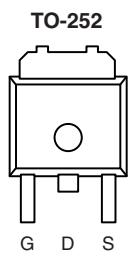
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 100	0.043 at $V_{GS} = - 10$ V	- 37	54 nC
	0.048 at $V_{GS} = - 4.5$ V	- 35	

FEATURES

- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

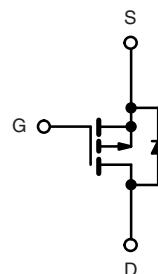


RoHS
COMPLIANT



Drain Connected to Tab

Top View



Ordering Information: SUD50P10-43L-E3 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 100		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 175$ °C) ^b	I_D	- 37.1 ^a		
		- 31 ^a		
		- 9.2 ^{b, c}		
		- 7.7 ^{b, c}		
Pulsed Drain Current	I_{DM}	- 40		A
Continuous Source Current (Diode Conduction)	I_S	- 50 ^a		
		- 6.9 ^{b, c}		
Avalanche Current	I_{AS}	- 35		
Single Pulse Avalanche Energy	E_{AS}	61	mJ	
Maximum Power Dissipation	P_D	136		W
		95		
		8.3 ^{b, c}		
		5.8 ^{b, c}		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	R_{thJA}	15	18	°C/W
		40	50	
Junction-to-Case (Drain)	R_{thJC}	0.85	1.1	

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 40 °C/W.

SUD50P10-43L

Vishay Siliconix



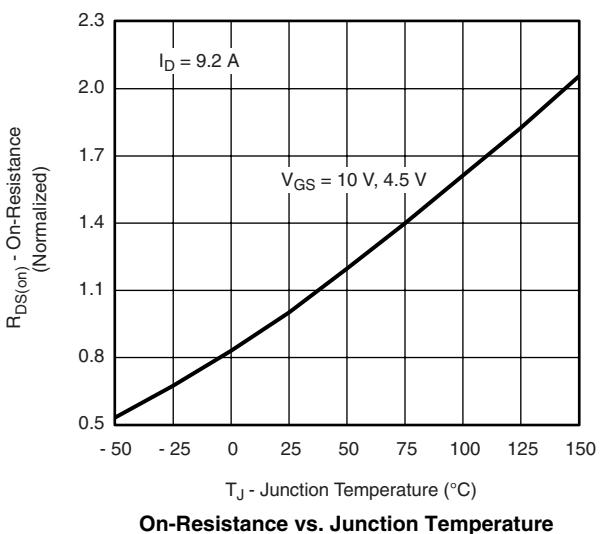
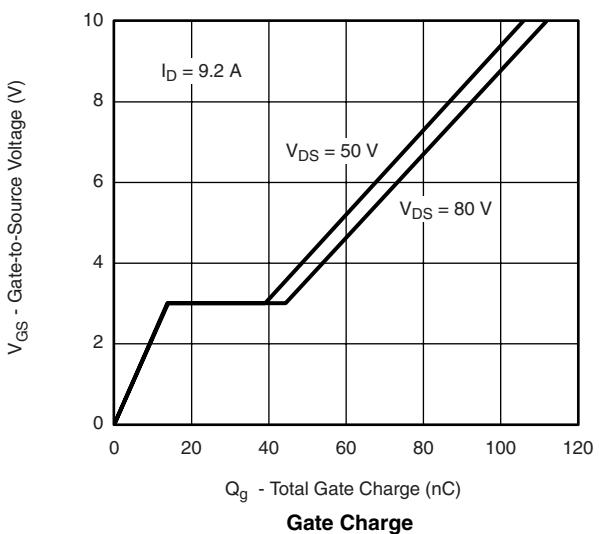
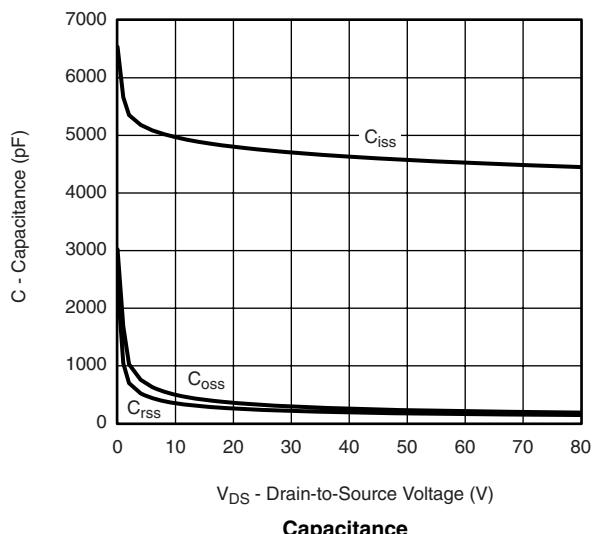
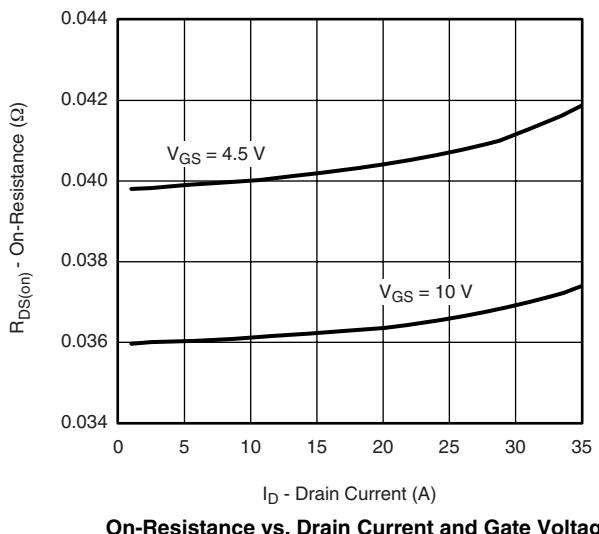
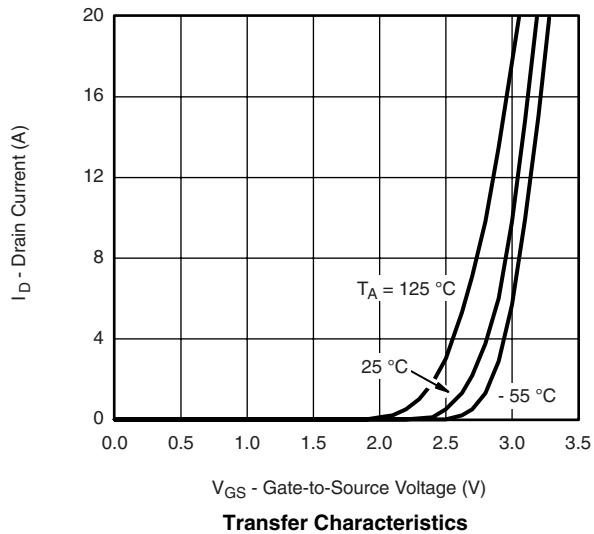
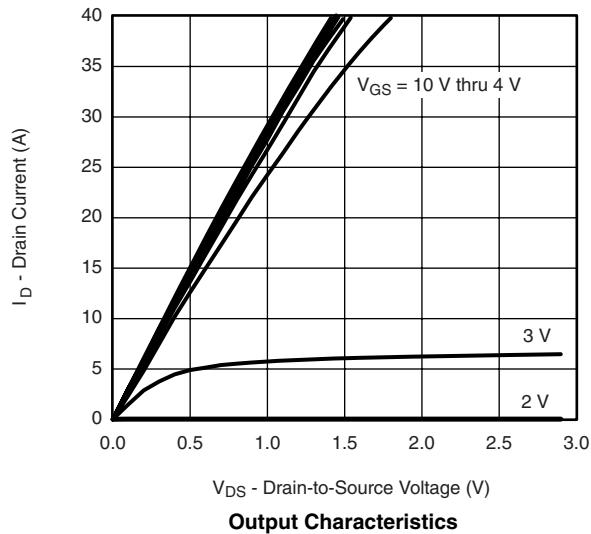
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$		-109		$\text{mV/}^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			5.9		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1		-3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -100 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = -10 \text{ V}$	-40			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}, I_D = -9.2 \text{ A}$		0.036	0.043	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -7.7 \text{ A}$		0.040	0.048	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -9.2 \text{ A}$		38		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		4600		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	$V_{DS} = -50 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -9.2 \text{ A}$		106	160	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -50 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -9.2 \text{ A}$		54	81	
Gate-Drain Charge	Q_{gd}			14		
Gate Resistance	R_g		$f = 1 \text{ MHz}$	26		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -50 \text{ V}, R_L = 6.5 \Omega$ $I_D \approx -7.7 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		4		Ω
Rise Time	t_r			15	25	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			20	30	
Fall Time	t_f			110	165	
Turn-On Delay Time	$t_{d(\text{on})}$			100	150	ns
Rise Time	t_r			42	65	
Turn-Off Delay Time	$t_{d(\text{off})}$			160	240	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-50	A
Pulse Diode Forward Current ^a	I_{SM}				-40	
Body Diode Voltage	V_{SD}	$I_S = -7.7 \text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -7.7 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	225	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			14		

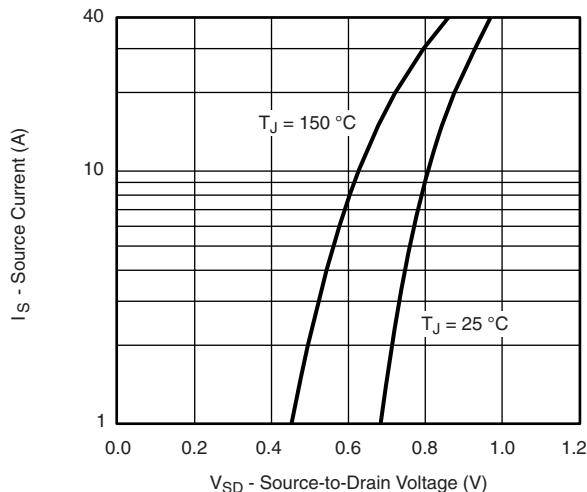
Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

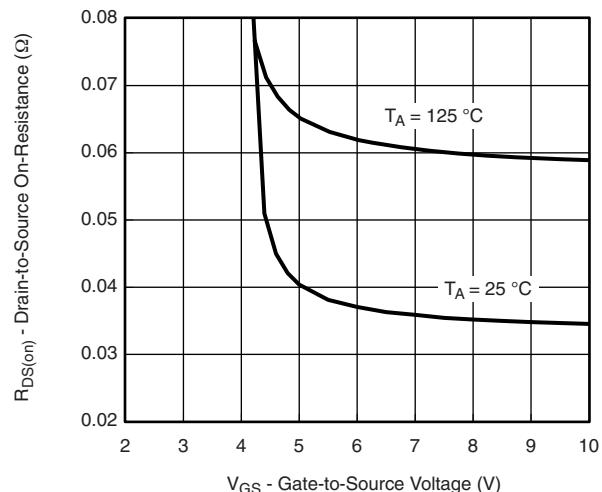
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


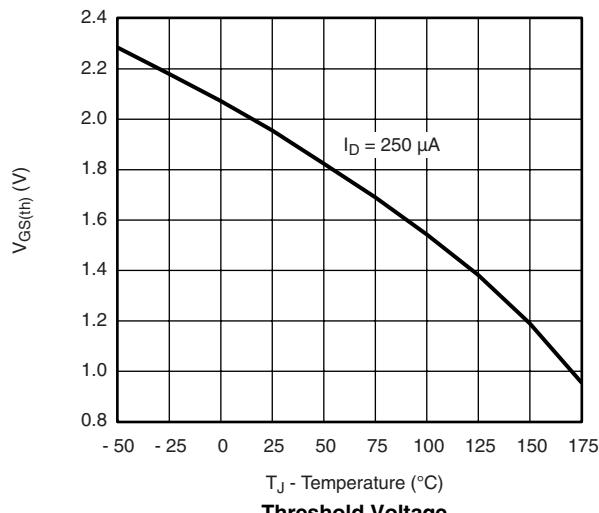
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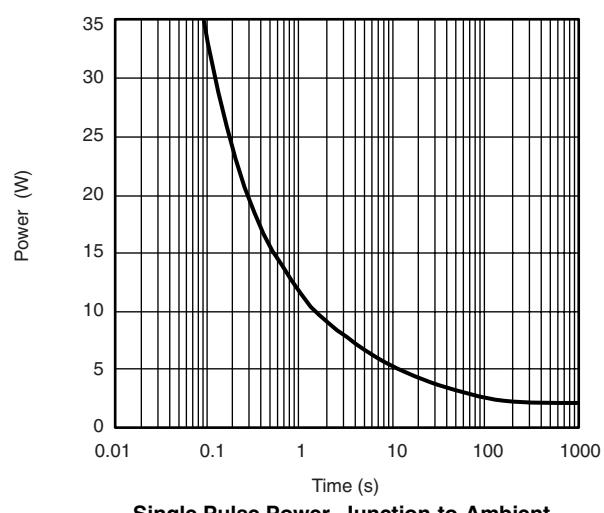
Source-Drain Diode Forward Voltage



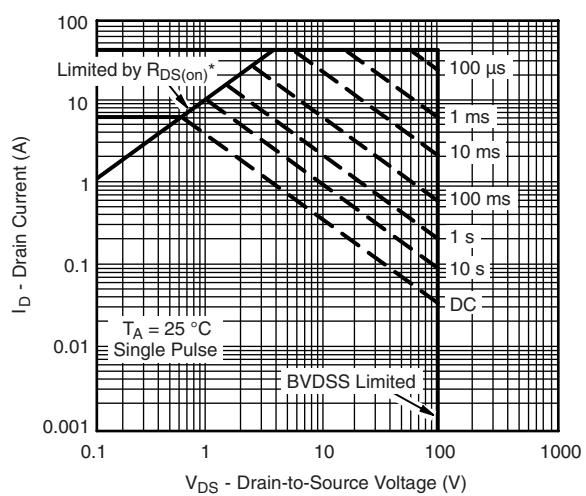
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

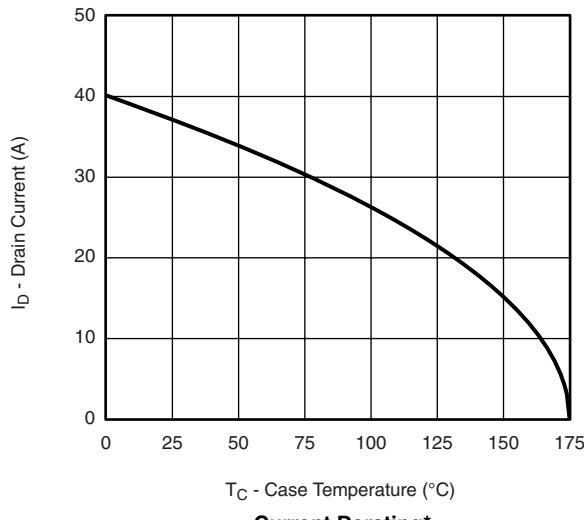
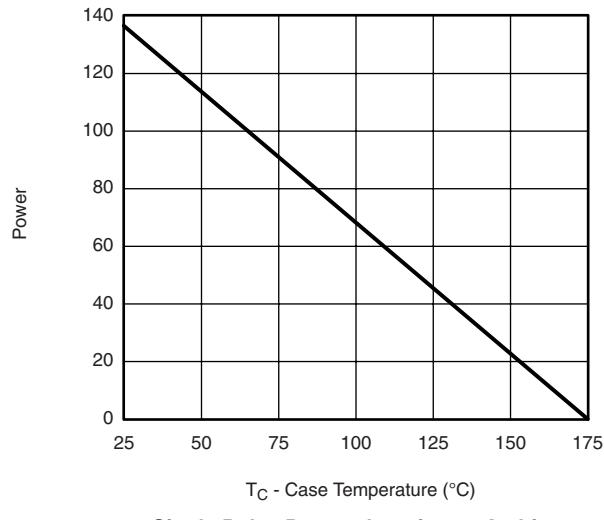
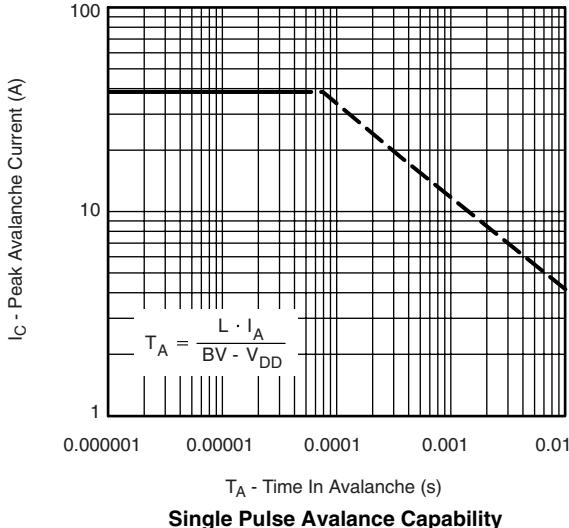


Single Pulse Power, Junction-to-Ambient

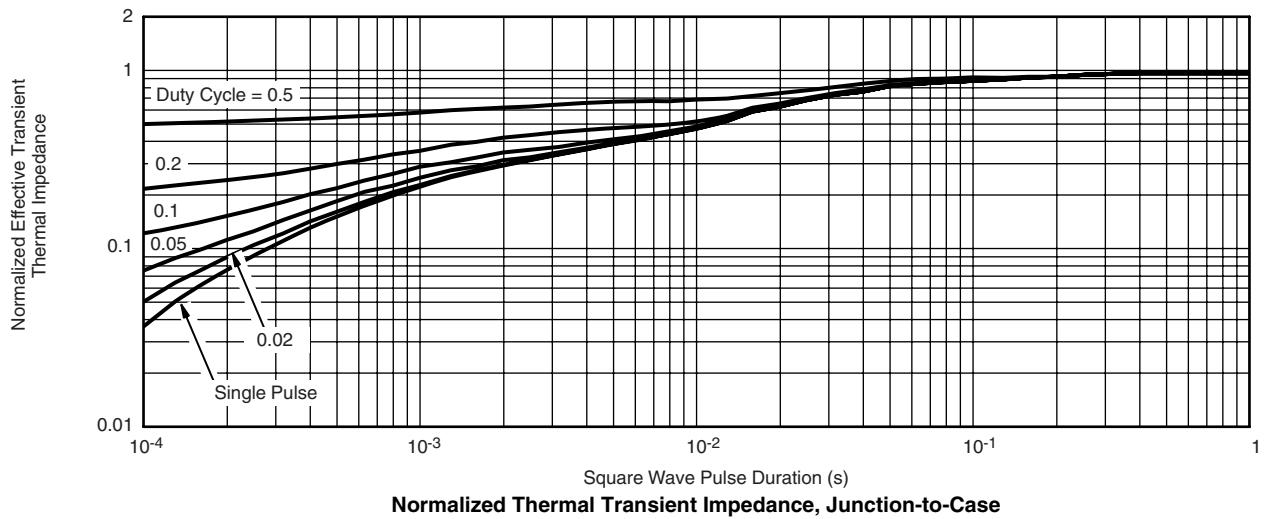
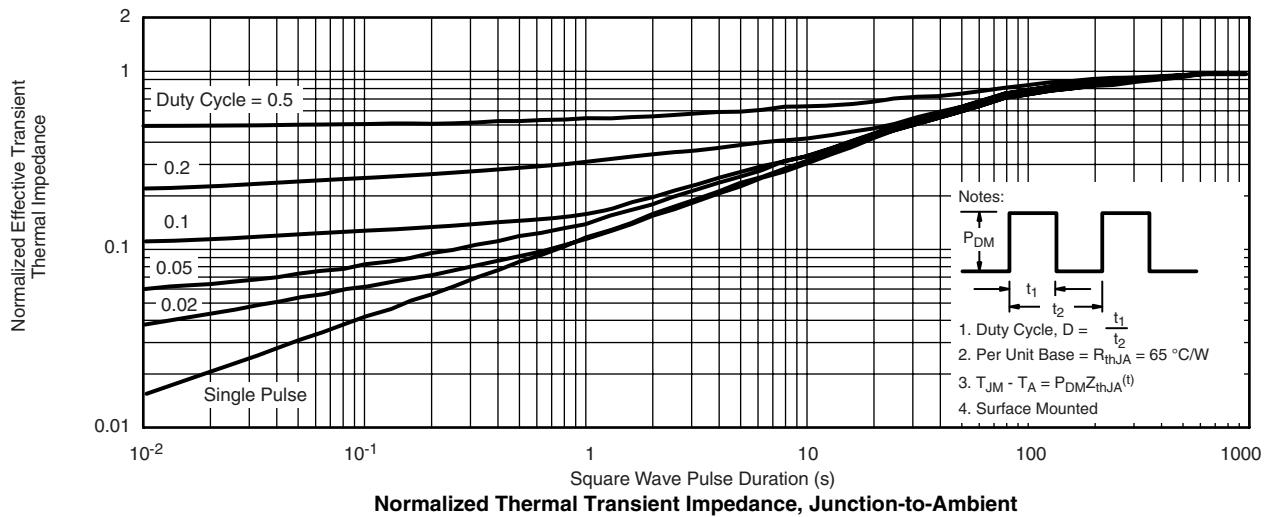


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

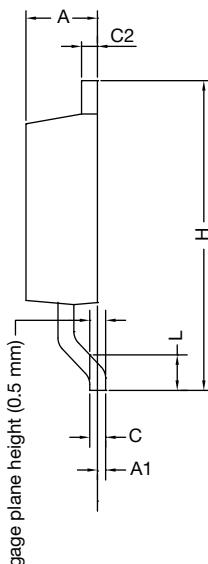
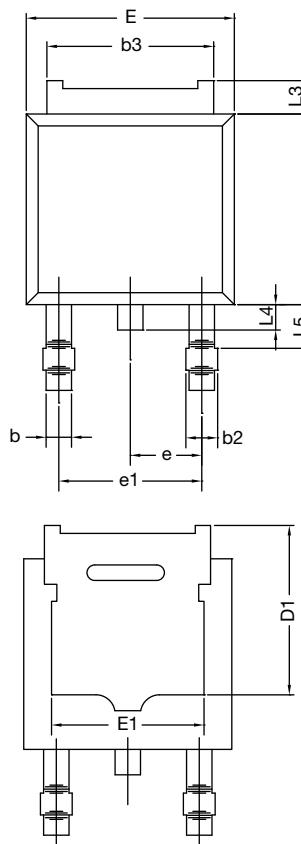
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Current Derating*

Single Pulse Power, Junction-to-Ambient

Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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TO-252AA Case Outline

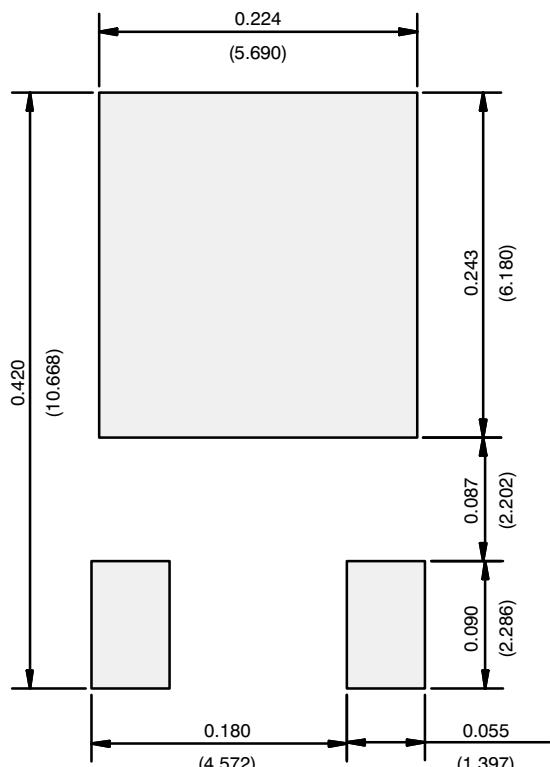


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T16-0236-Rev. P, 16-May-16
DWG: 5347

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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