CS49DV8C Data Sheet

FEATURES

- 32-bit Post-Processor Audio DSP supports Multichannel Dolby® Volume
- Programmable through DSP Composer™
- CS49DV8, supports up to 7.1 Channels of Dolby Volume processing at 48 kHz, 44.1 kHz or 32 kHz.
  - Input Configurable for all input/output digital audio types (I^2S, LJ/RJ, and TDM)
  - 32-bit data path delivers uncompromised dynamic range
  - 192 kHz capable integrated S/PDIF transmitter
  - DAO can operate in master or slave mode (SCLK & LRCLK)
- Integrated Clock Manager/PLL
  - Capable of operating from a wide variety of external crystals or external oscillators
- Input Fs Auto Detection, Reporting and Handling
- Sample rate conversion.
- Master & Slave Host Boot Capability via Serial Interface
- SPI interface capable of running up to 25 MHz during run time
- 1.8V Core and a 3.3V I/O that is tolerant to 5V input

32-bit Dual Audio DSP Engine featuring Multichannel Dolby® Volume

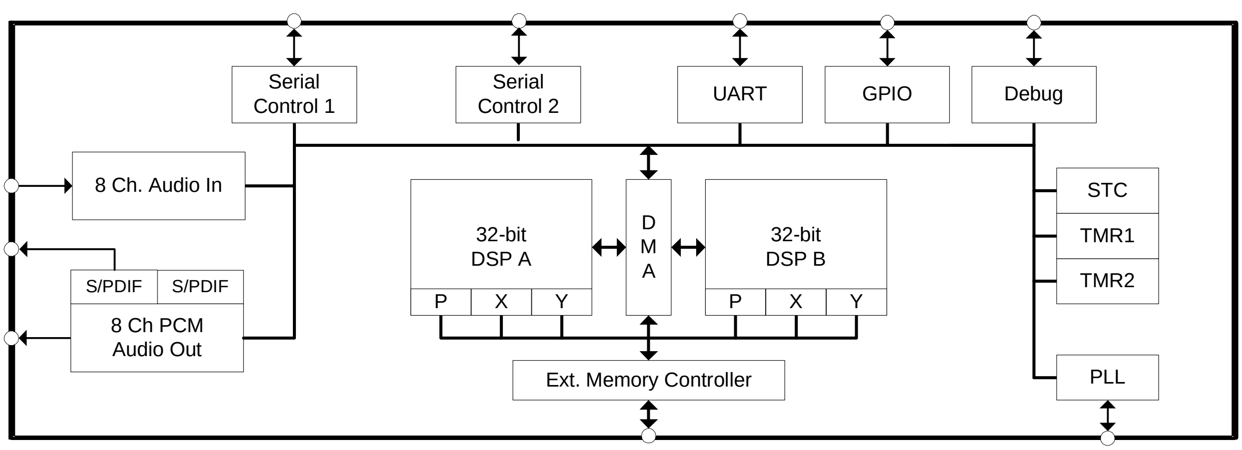
The new CS49DV8C is the fastest time-to-market, mass-production ready Multichannel Dolby Volume solution available. The target applications for the CS49DV8C DSP are:

- Soundbars
- DTVs with Integrated Soundbars
- HDTV Stands/Furniture with Integrated Soundbars
- Automotive Head Units
- Automotive Outboard Amplifiers
- Blu-ray Disc® & DVD Receivers / HTiBs

All of these applications and many more that use volume control and are subject to playback from sources that do not have consistent volume levels will benefit from the CS49DV8C Dolby Volume solution.

Ordering Information

See page 27 for ordering information.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**.

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1. Documentation Strategy

The CS49DV8C data sheet describes the CS49DV8C family of multichannel audio DSPs. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS49DV8C family of processors.

Table 1. CS49DV8C Related Documentation

Document Name	Description
CS49DV8C Data Sheet	This document
CS4953xx Hardware User's Manual	Detailed system design information including Typical Connection Diagrams, boot-procedures, pin descriptions, and other system configuration information.
AN288PPH, "Dolby® Volume Module"	Application note contains an Application Programming Interface (API) used to control the Dolby Volume firmware.
DSP Composer™ User's Manual	Includes detailed configuration and usage information for the GUI development tool.

The scope of the *CS49DV8C Data Sheet* is primarily the hardware specifications of the CS49DV8C devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS49DV8C Data Sheet* is the system PCB designer, MCU programmer, and the quality control engineer.

2. Overview

The CS49DV8C DSP is designed to provide high-performance volume control using the Dolby Volume algorithm. The CS49DV8, supports up to 7.1 Channels of Dolby Volume processing at 48 kHz, 44.1 kHz or 32 kHz while leaving the 2nd core of the DSP completely available for even further processing functions such as Quadruple Crossover Bass Management, Tone Control, and Multiband Parametric EQ.

The CS49DV8C DSP, together with Cirrus Logic's comprehensive library of audio processing algorithms, enables the development of next-generation high-definition audio solutions. Cirrus Logic also provides a broad array of digital interface products, and audio converters, to meet your audio system-level design requirements.

The CS49DV8C is available in a 128-pin LQFP package.

Please refer to Table 2 on page 6 for the processor speed and available firmware for the CS49DV8C product family.

Table 2. Device and Firmware Selection Guide

Device	Pre-Process	Decode Processor A[1]	Mid-processor A[1]	Mid-processor B[1]	Post-processor[1]
CS49DV8C **300 MIPS**	None	• Stereo PCM • Multi-Channel PCM (2:1 Downsampling Option) (4:1 Downsampling Option)	Dolby® Volume (Runs on either DSP A or B) See Section 3. for additional concurrency information.	Dolby® Volume (Runs on either DSP A or B) See Section 3. for additional concurrency information.	• Tone Control • Re-EQ • PEQ (up to 11 bands) • Delay • 7.1 Bass Manager • Audio Manager • 1:2 Upsampling

1. Processing may be restricted and dependent on firmware selected. Contact your Cirrus Logic FAE for concurrency matrix.

2.1 Licensing

Licenses are required for Dolby Volume and for all of the third party audio processing algorithms. Please contact your local Cirrus Sales representative for more information.

3. Firmware Supported

The suite of software available for the CS49DV8C family consists of operating systems (OS) and a library of overlays. The overlays have been divided into three main groups called Decoders, Mid-processors, and Post-processors. All software components are defined as follows:

- **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, auto-detection, error concealment, etc.
- **Dolby Volume** - The CS49DV8C can run Dolby Volume on either DSP A or DSP B. On the DSP that is not running Dolby Volume, it can run the firmware currently available on the CS4953xx family for that DSP (A or B).

4. Hardware Functional Description

4.1 DSP Core

The CS49DV8C is a dual-core DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two memory access control (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS49DV8C functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS49DV8C from a host MCU or external FLASH/EEPROM. Users can choose to use standard audio post-processor modules which are available from Cirrus Logic.

4.1.1 DSP Memory

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS49DV8C DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16k SRAM, 32k ROM	10k SRAM, 8k ROM
Y	24k SRAM, 32k ROM	16k SRAM, 16k ROM
P	8k SRAM, 32k ROM	8k SRAM, 24k ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6 line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM or IEC61937. Up to 32-bit word lengths are supported. Additionally support is provided for audio data input to the DSP via the DAI from an HDMI receiver.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192 kHz SPDIF transmitter (data with embedded clock on a single line).

4.2.3 Serial Control Port 1 & 2 (I^2C® or SPI™)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 25MHz in SPI mode. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control.

4.2.4 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus.

4.2.5 GPIO

Many of the CS49DV8C peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.6 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS49DV8C defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS49DV8C pins are multi-functional. For details on pin functionality please refer to the *CS4953xx Hardware User's Manual.*

4.3.2 Termination Requirements

Open-drain pins on the CS49DV8C must be pulled high for proper operation. Please refer to the *CS4953xx Hardware User's Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS49DV8C are used to select the boot mode upon the rising edge of reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS4953xx Hardware User's Manual*.

4.3.3 Pads

The CS49DV8C I/O operates from the 3.3 V supply and is 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device.

5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = 1.8 V, VDDA = VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
DC power supplies:	Core supply	VDD	–0.3	2.0	V
	PLL supply	VDDA	–0.3	3.6	V
	I/O supply	VDDIO	–0.3	3.6	V
	|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies		I_{in}	-	+/- 10	mA
Input voltage on PLL_REF_RES		V_{filt}	-0.3	3.6	V
Input voltage on I/O pins		V_{inio}	-0.3	5.0	V
Storage temperature		T_{stg}	–65	150	°C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
DC power supplies:	Core supply	VDD	1.71	1.8	1.89	V
	PLL supply	VDDA	3.13	3.3	3.46	V
	I/O supply	VDDIO	3.13	3.3	3.46	V
	|VDDA – VDDIO|			0		V
Ambient operating temperature	Commercial Grade (CVZ/CVZR)	T_A	0	+25	+ 70	°C

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -4mA), except XTI, SDRAM pins	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 4mA), except XTI, SDRAM pins	V_{OL}	-	-	VDDIO * 0.1	V
SDRAM High-level output voltage (I_O = -8mA)	V_{OH}	VDDIO * 0.9	-	-	V
SDRAM Low-level output voltage (I_O = 8mA)	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	-	-	5	µA

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	-	-	50	µA

5.4 Power Supply Characteristics

(Measurements performed under operating conditions.)

Parameter	Min	Typ	Max	Unit
Power supply current:				
Core and I/O operating: VDD[1]	-	500	-	mA
PLL operating: VDDA	-	3.5	-	mA
With external memory and most ports operating: VDDIO	-	120	-	mA

1.Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (128-Pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		-	48	-	
Four-layer Board[2]		-	40	-	
Thermal Resistance (Junction to Top of Package)	Ψ_{jt}				°C / Watt
Two-layer Board[1]		-	.39	-	
Four-layer Board[2]		-	.33	-	

Notes: 1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20% of the top and bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20% of the top and bottom layers and 0.5-oz copper covering 90% of the internal power plane and ground plane layers.

3. To calculate the die temperature for a given power dissipation
T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]

4. To calculate the case temperature for a given power dissipation
$T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

5.6 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	-	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	-	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	-	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	-	ns

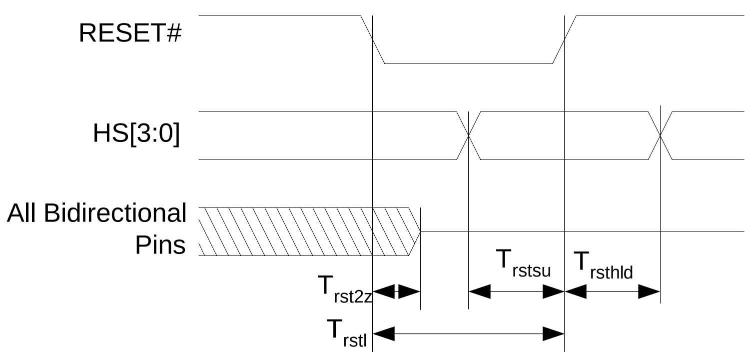

Figure 1. RESET Timing

5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	W

1. Part characterized with the following crystal frequency values: 11.2896, 12.288, 18.432, 24.576, and 27 MHz.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

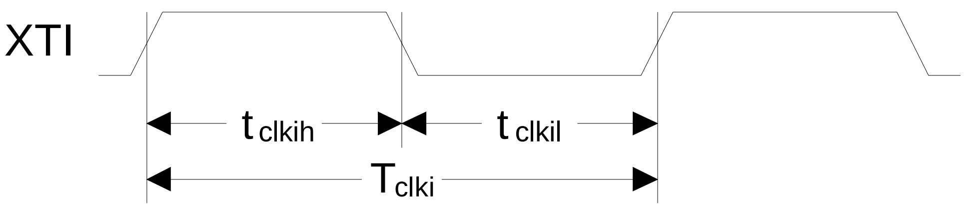

Figure 2. XTI Timing

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1] CS49DV8C-CVZ CS49DV8C-CVZR	F_{dclk}	F_{xtal}	150	MHz
Internal DCLK period[1] CS49DV8C-CVZ CS49DV8C-CVZR	DCLKP	6.7	$1/F_{xtal}$	ns

1.After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode

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Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
SCP_CS falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to SCP_IRQ rising	$t_{spiirqh}$	-		20	ns
SCP_CS rising to SCP_IRQ falling	$t_{spiirql}$	0			ns
SCP_CLK low to SCP_CS rising	t_{spicsh}	24		-	ns
SCP_CS rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to SCP_BSY falling	$t_{spicbsyl}$	-	3∗DCLKP+20		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY pin should be implemented to prevent overflow of the input data buffer.At boot the maximum speed is Fxtal/3.

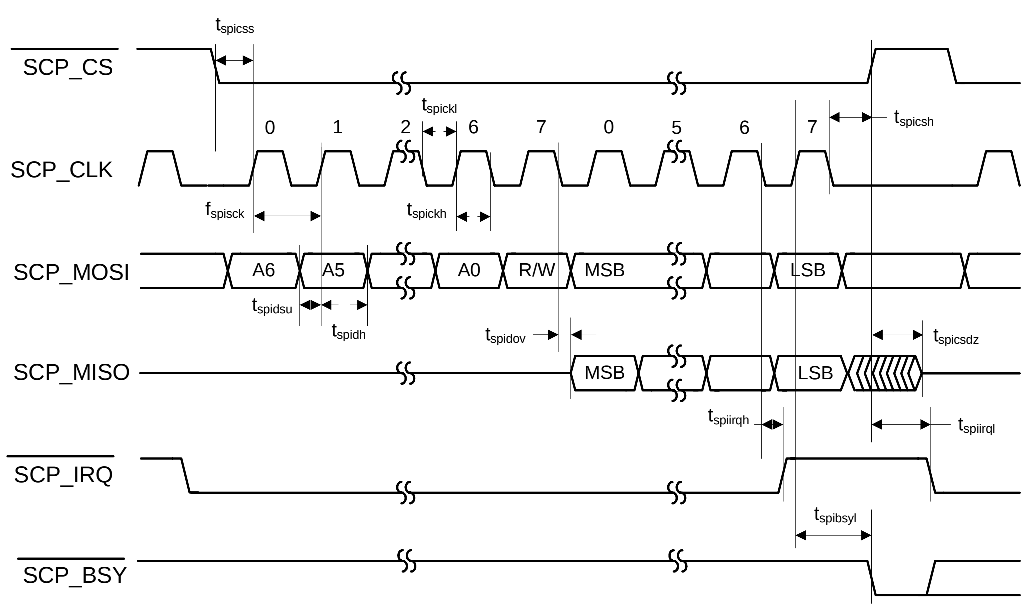


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		$F_{xtal}/2$ (See Footnote 2)	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising [3]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	18		-	ns
SCP_CLK high time	t_{spickh}	18		-	ns
Setup time SCP_MISO input	t_{spidsu}	11		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		11	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ falling	t_{spicsl}	7		-	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active $\overline{\text{SCP\_CS}}$	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter.

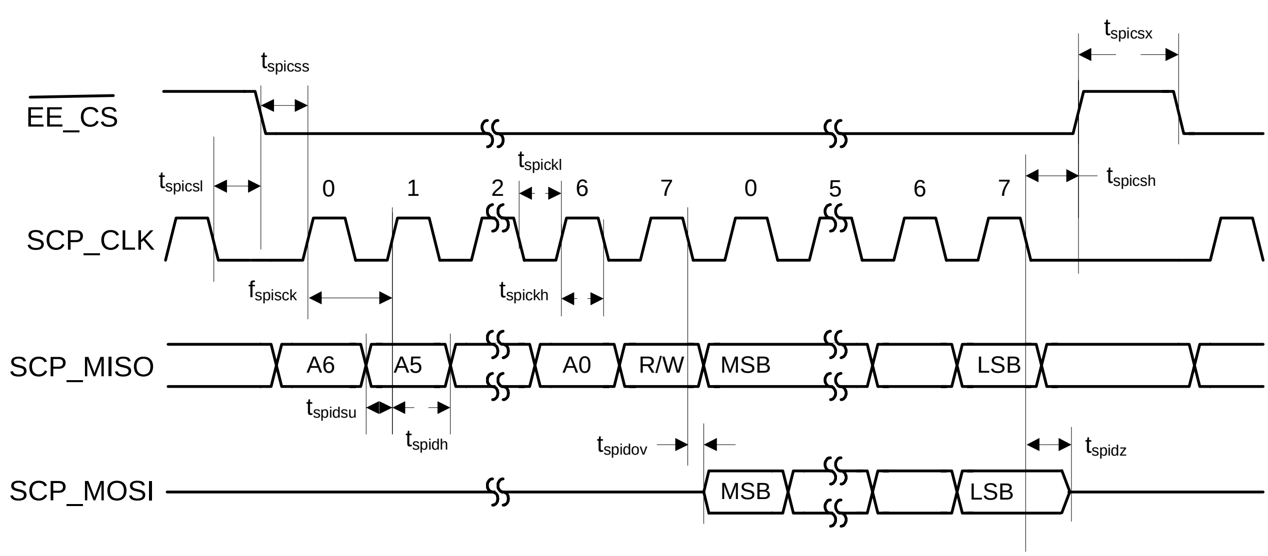


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	-		3∗DCLKP + 40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$		3∗DCLKP + 20		ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	-	3∗DCLKP + 20		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.

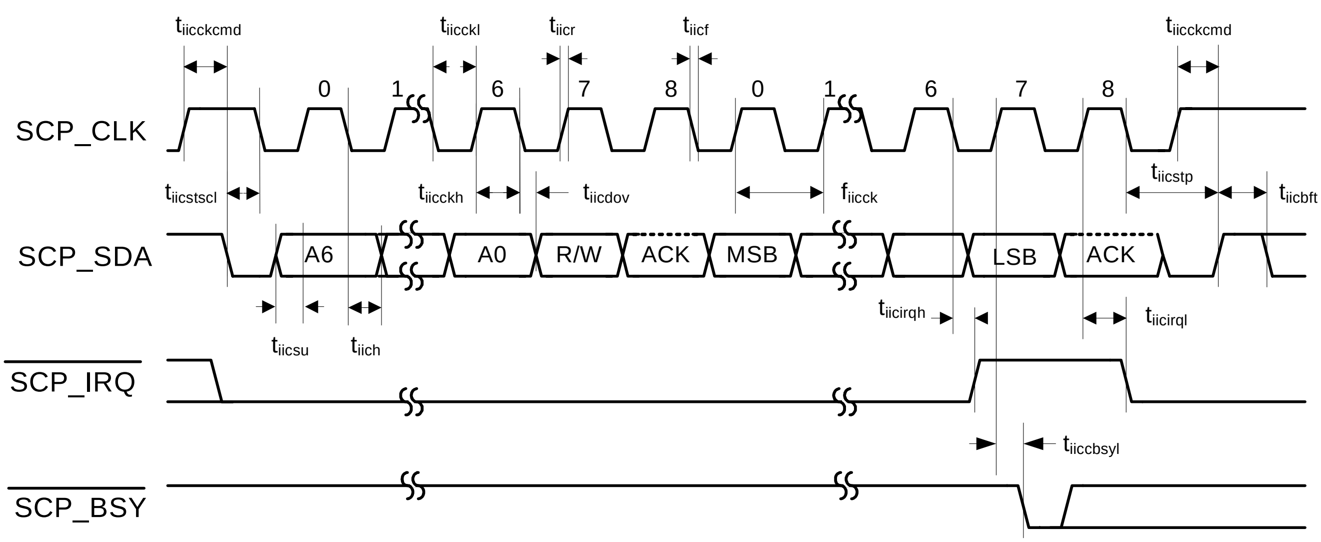


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

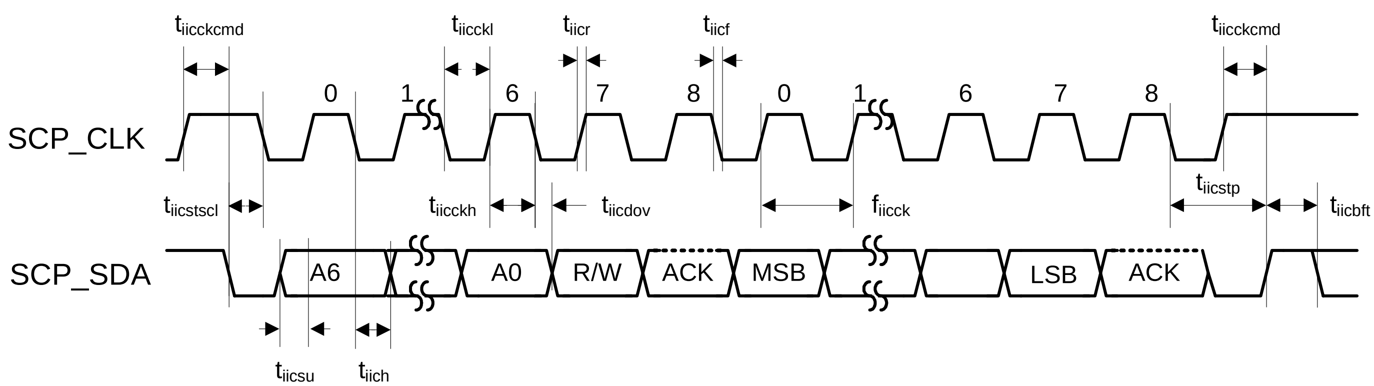


Figure 6. Serial Control Port - I²C Master Mode Timing

5.13 Switching Characteristics — UART

Parameter	Symbol	Min	Max	Unit
UART_CLK period[1]	t_{uclki}	266	-	ns
UART_CLK duty cycle	-	40	60	%
Setup time for UART_RXD	$t_{uckrxsu}$	5	-	
Hold time for UART_RXD	$t_{uckrxdv}$	5	-	ns
Delay from CLK transition to TXD transition	$t_{ucktxdv}$	-	29	ns

1. The minimum clock period is limited to DCLKP/32 or the minimum value, whichever is larger.

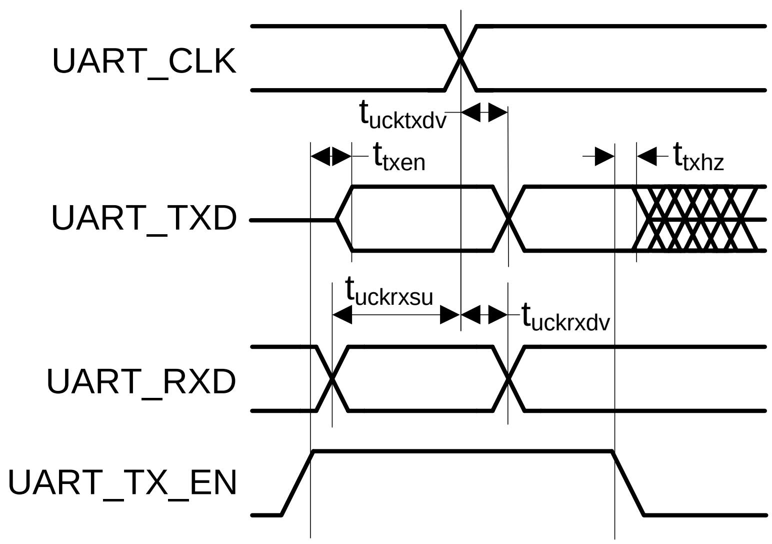


Figure 7. UART Timing

5.14 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

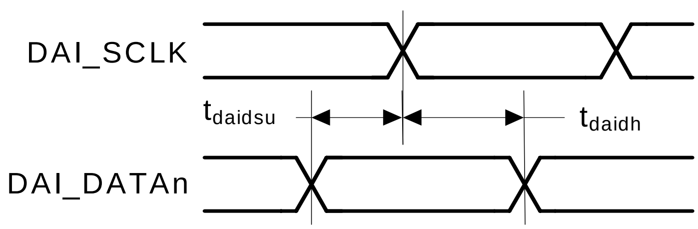
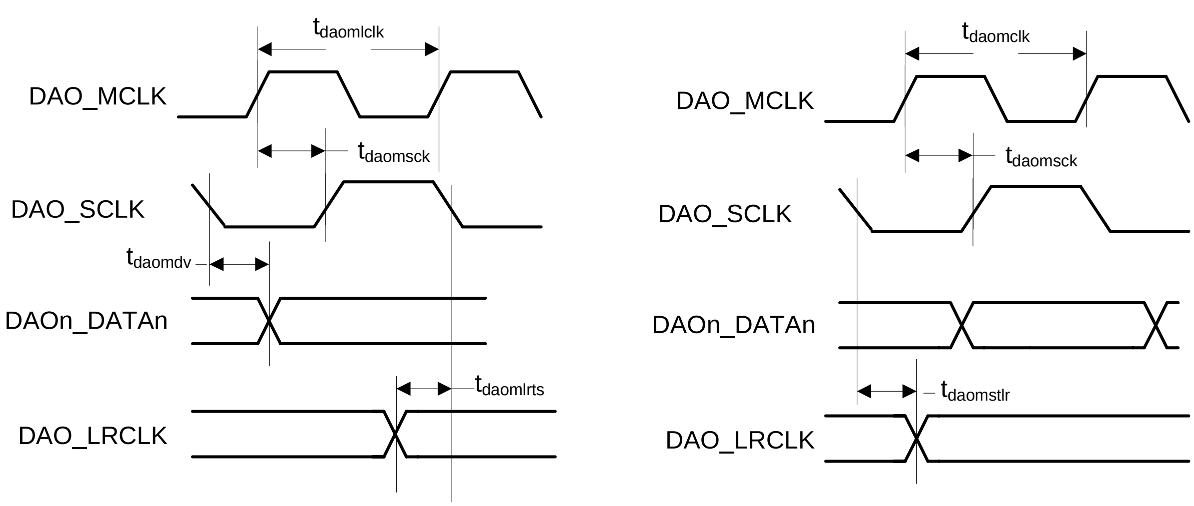


Figure 8. Digital Audio Input (DAI) Port Timing Diagram

5.15 Switching Characteristics — Digital Audio Output Port

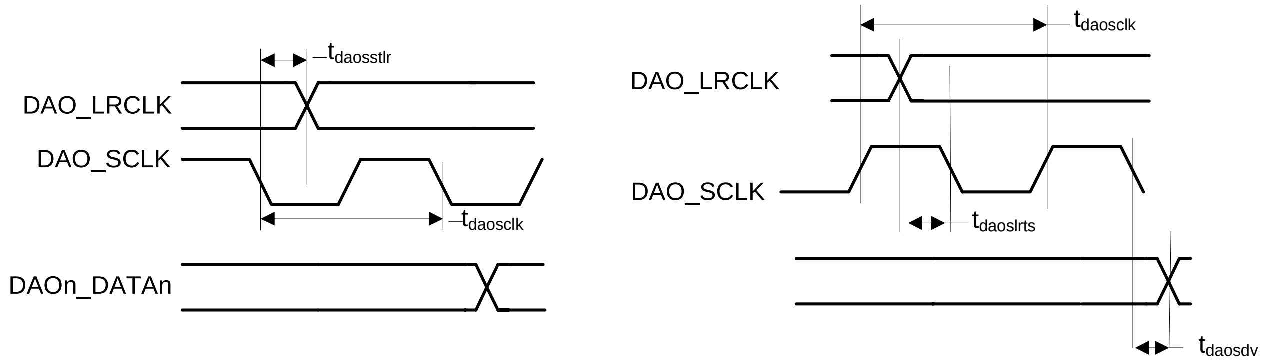
Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle	-	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	-	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daomstlr}$	-	8	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daomlrts}$	-	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daosdv}	-	15	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daosstlr}$	-	30	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daoslrts}$	-	15	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS49DVxx driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 9. Digital Audio Port Timing Master Mode



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 10. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

5.16 Switching Characteristics — SDRAM Interface

Refer to Figure 11 through Figure 14.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3		-	ns
SD_CLKIN low time	t_{sdclkl}	2.3		-	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	-		1	ns
SD_CLKOUT Frequency			150		MHz
SD_CLKOUT duty cycle	-	45		55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	-		3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}		1.1	-	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	-	3.8	-	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38		-	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3		-	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	1.38		-	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	-	3.8	-	ns

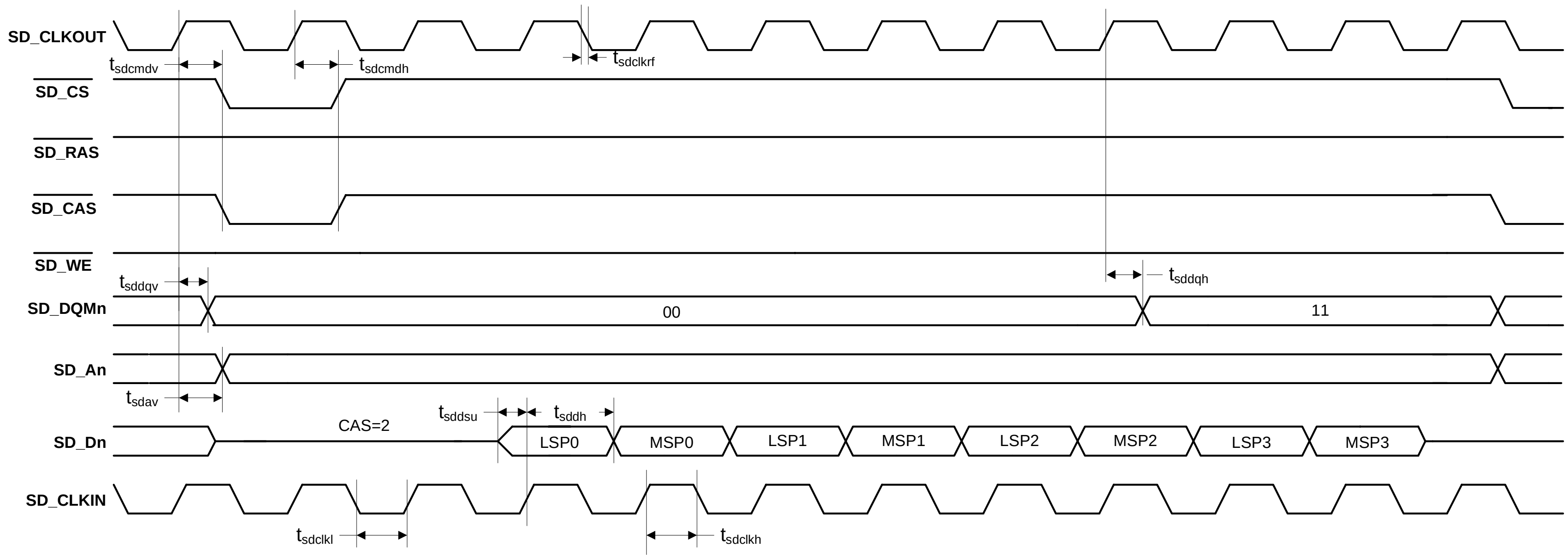


Figure 11. External Memory Interface - SDRAM Burst Read Cycle

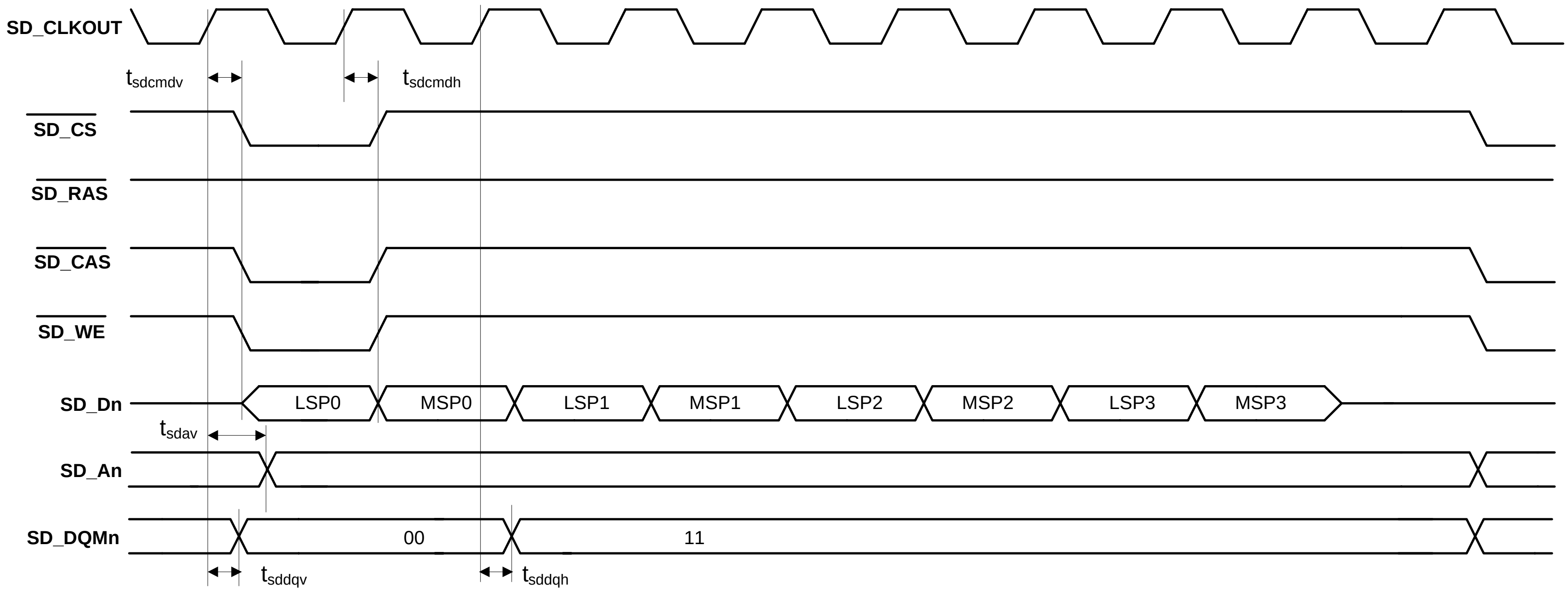


Figure 12. External Memory Interface - SDRAM Burst Write Cycle

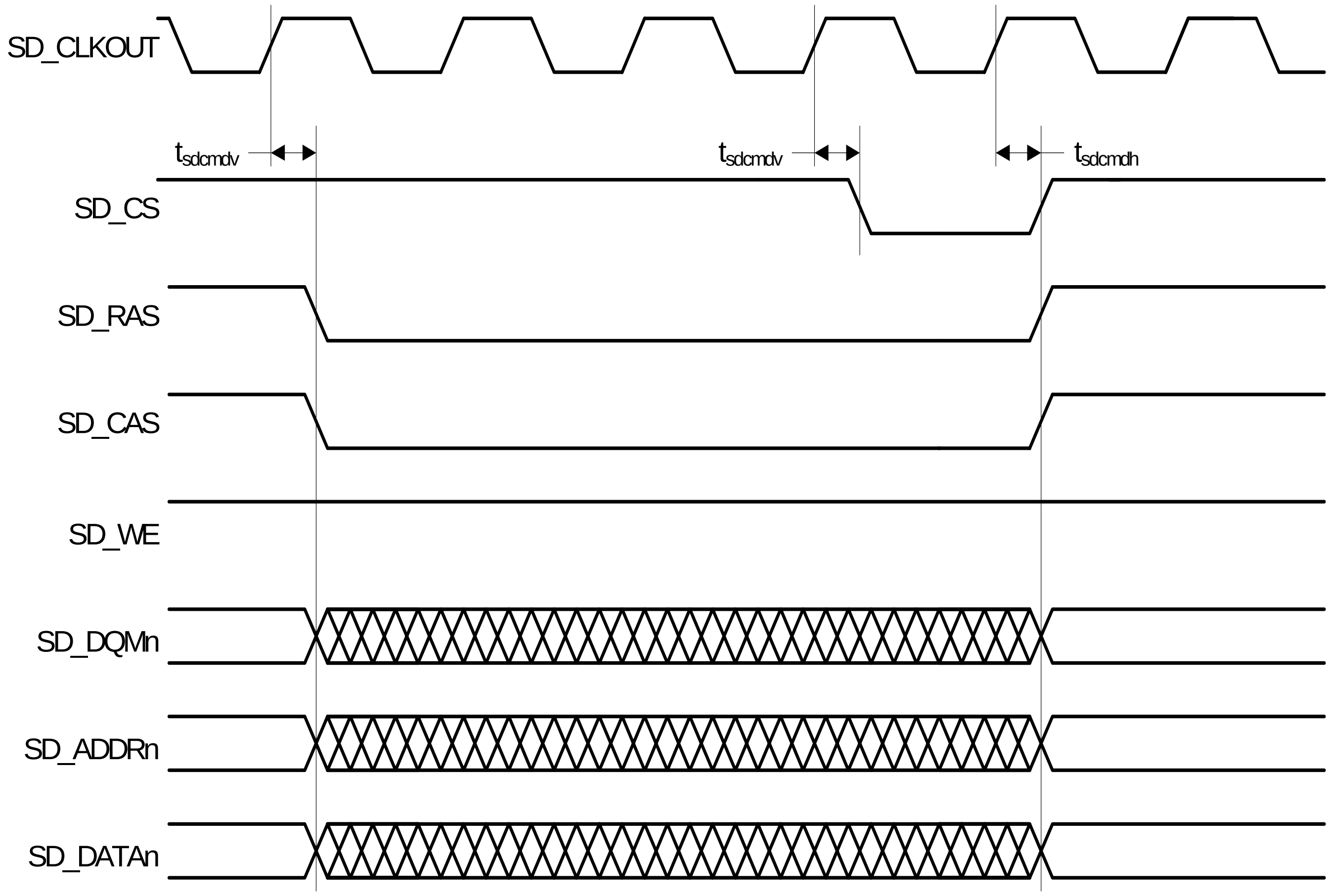


Figure 13. External Memory Interface - SDRAM Auto Refresh Cycle

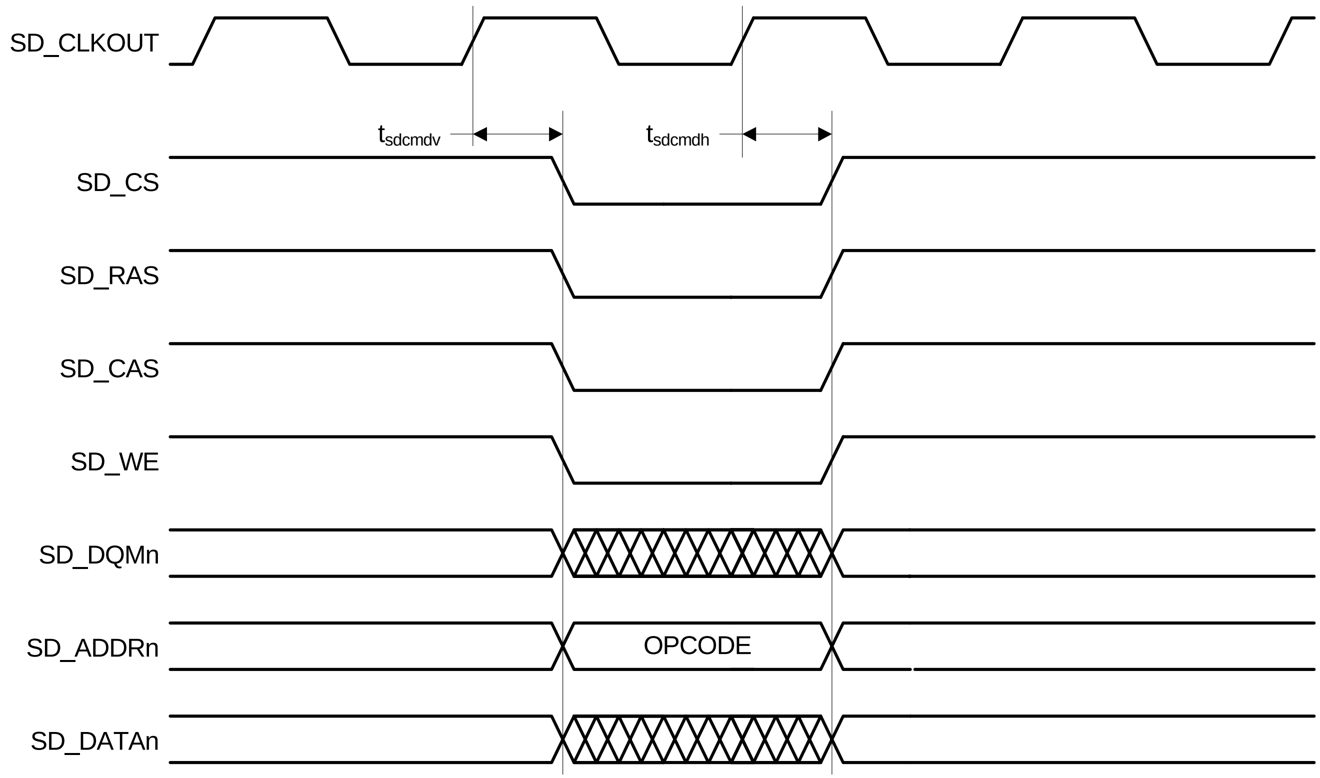


Figure 14. External Memory Interface - SDRAM Load Mode Register Cycle

6. Ordering Information

The CS49DV8C family part number is described as follows:

CS49DVNNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 4. Ordering Information

Part No.	Grade	Temp. Range	Container	Package
CS49DV8C-CVZ	Commercial	0 to +70 °C	Tray	128-pin LQFP
CS49DV8C-CVZR	Commercial	0 to +70 °C	Reel	

7. Environmental, Manufacturing, and Handling Information

Table 5. Environmental, Manufacturing, and Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS49DV8C-CVZ	260 °C	3	7 Days
CS49DV8C-CVZR	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

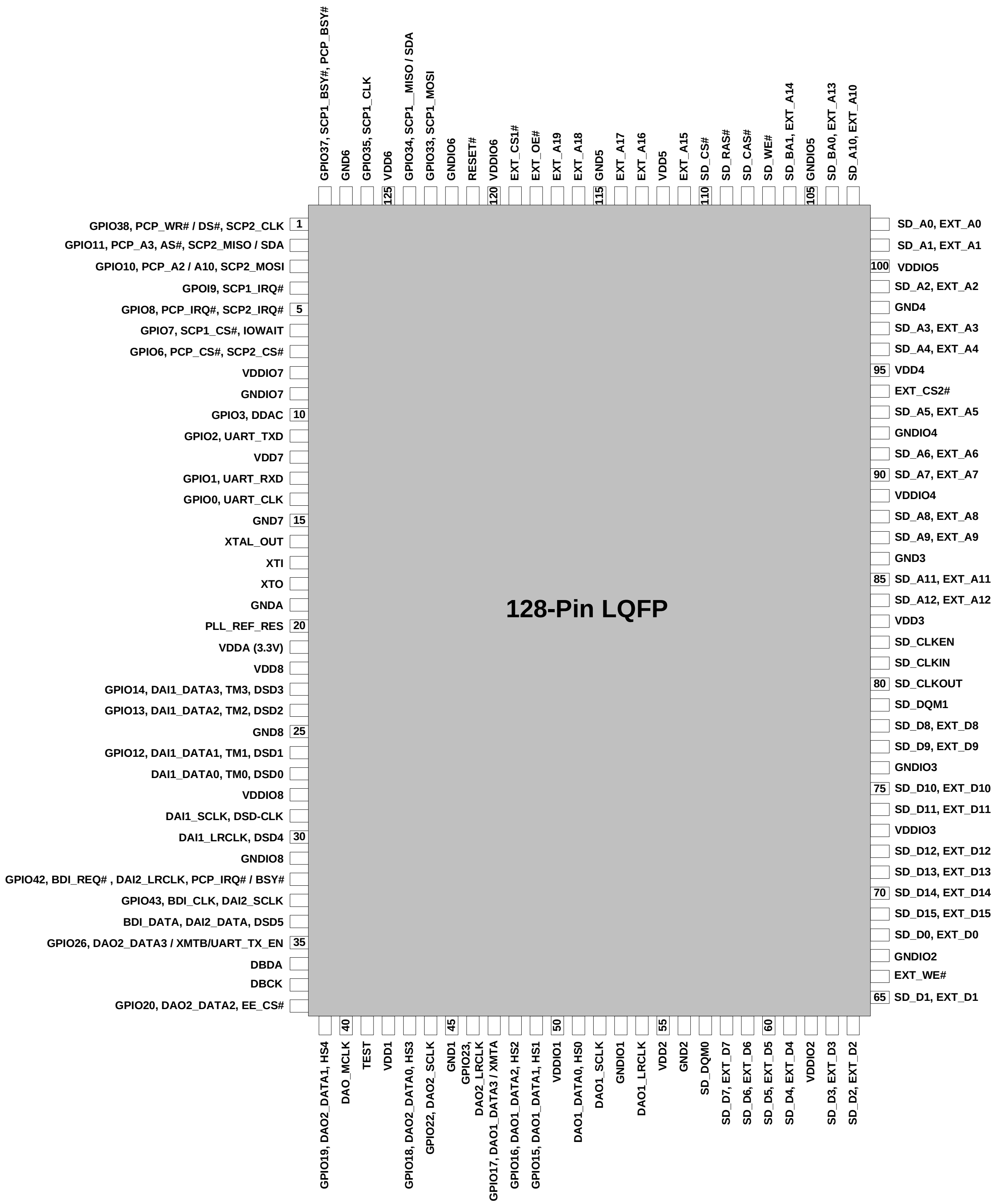


Figure 15. 128-Pin LQFP Pin-Out

9. Package Mechanical Drawings

9.1 128-Pin LQFP Package

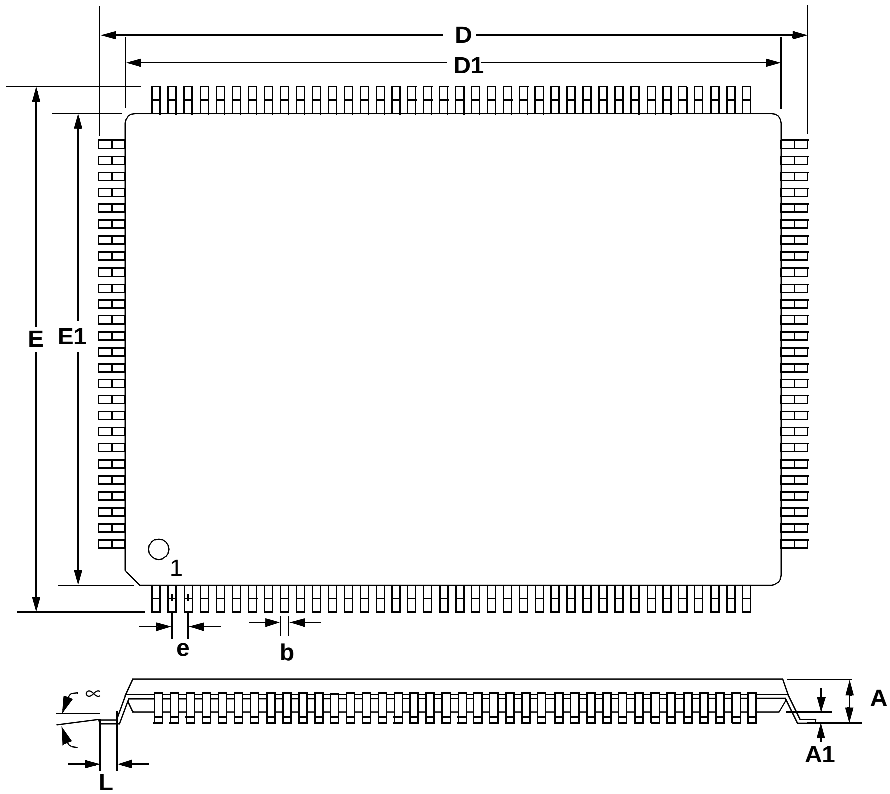


Figure 16. 128-Pin LQFP Package Drawing

Table 6. 128-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	.063”
A1	0.05	---	0.15	.002”	---	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

10. Revision History

Revision	Date	Changes
PP1	September 2, 2008	Initial Release.
PP2	September 25, 2008	Removed references to External Parallel Flash / SRAM Interface.