MAXIM

DisplayPort/PCIe Passive Switches

MAX4928A/MAX4928B

General Description

The MAX4928A/MAX4928B high-speed passive switches route PCI Express® (PCIe) data and/or DisplayPort™ signals between two possible destinations in desktop or laptop PCs. The MAX4928A is intended to be used with the ATX form factor desktop PCs, while the MAX4928B is expected to be used in the BTX form factor.

The MAX4928A/MAX4928B are hex double-pole/double-throw (6 x DPDT) switches. The MAX4928A/MAX4928B feature a single digital control input (SEL) to switch signal paths and a latch input (LE) that holds the switches in a given state.

The MAX4928A/MAX4928B are fully specified to operate from a single +3.3V (typ) power supply. The MAX4928A/MAX4928B are available in an industry standard 5mm x 11mm, 56-pin TQFN package. Both devices operate over the -40°C to +85°C extended temperature range.

Applications

Desktop PCs

Notebook PCs

PCI Express is a registered trademark of PCI-SIG.

DisplayPort is a trademark of Video Electronics Standards Association (VESA).

Features

♦ **Single +3.3V Power Supply Voltage**

♦ **Supports PCIe Gen I, Gen II, and DisplayPort Data Rates > 5Gbps**

♦ **Excellent Return Loss > 12dB at 2.5GHz**

♦ **Six Bidirectional Pairs of Switches All Switching in One Device**

♦ **Low 850µA (max) Supply Current**

♦ **Small 5mm x 11mm, 56-Pin TQFN Package**
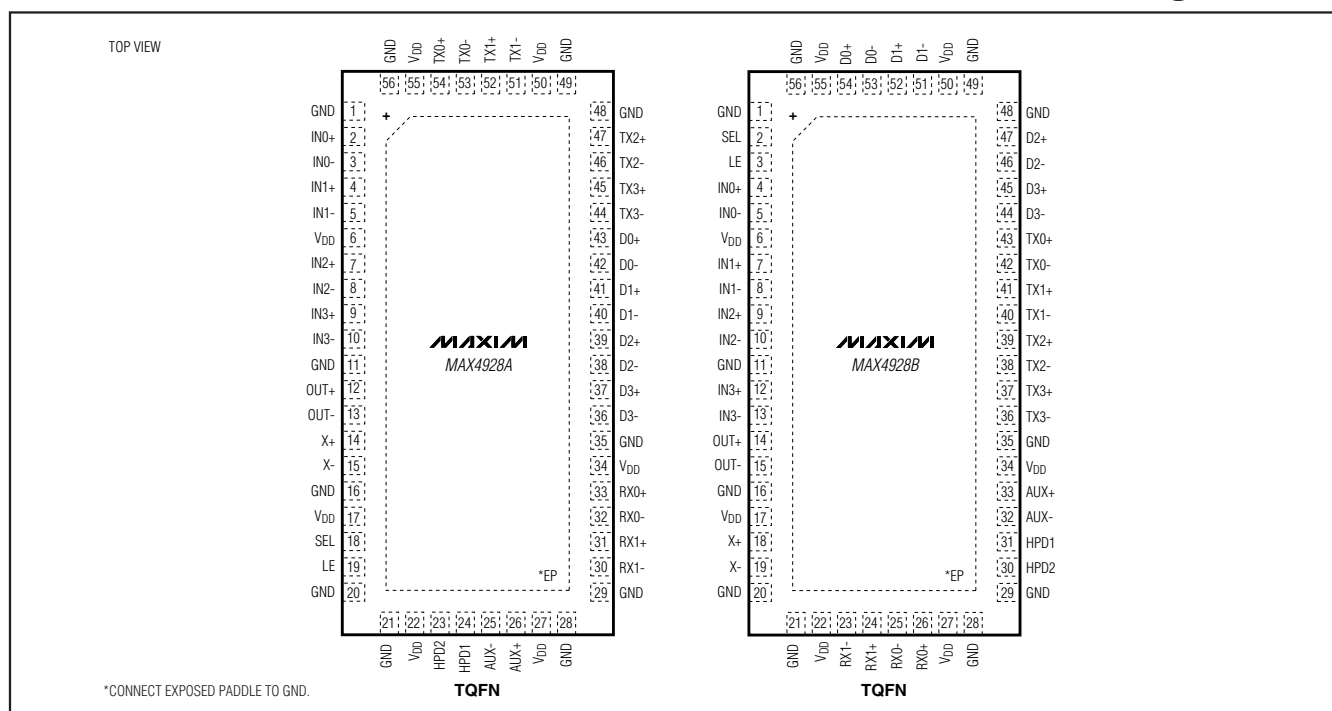
♦ **Industry-Standard Pinouts**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4928AETN+	-40°C to +85°F	56 TQFN-EP
MAX4928BETN+	-40°C to +85°F	56 TQFN-EP

+Denotes a lead-free package/RoHS-Compliant package.
EP = Exposed paddle.

Typical Operating Circuit appears at end of data sheet.

Pin Configurations

CONNECT EXPOSED PADDLE TO GND.

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DisplayPort/PCIe Passive Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V_{DD} ....-0.3V to +4V
LE, SEL, IN_, X_, OUT_, D_, TX_, HPD_, RX_, AUX_
   (Note 1) ....-0.3V to + (V_{DD} + 0.3V)
$|V_{IN\_} - V_{TX\_}|$, $|V_{IN\_} - V_{D\_}|$, $|V_{X\_} - V_{HPD\_}|$, $|V_{X\_} - V_{RX1\_}|$,
   $|V_{OUT\_} - V_{AUX\_}|$, $|V_{OUT\_} - V_{RX0\_}|$ (Note 1) ....0 to +2V
Continuous Current (IN_ to D_/TX_, X_ to HPD_/RX1_,
   OUT_ to AUX_/RX0_ ....±70mA
Peak Current (IN_ to D_/TX_, X_ to HPD_/RX1_, OUT_ to
   AUX_/RX0_) (pulsed at 1ms, 10% duty cycle) ....±70mA
Continuous Current (LE, SEL)...±30mA

Peak Current (LE, SEL)
   (pulsed at 1ms, 10% duty cycle)..................................±70mA
Continuous Power Dissipation (T_A = +70°C) for Multilayer Board
   56-Pin TQFN (derate 41.0mW/°C above +70°C) 3279mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Package Junction-to-Ambient Thermal Resistance (θ_{JA})
   (Note 2) ....24.4°C/W
Package Junction-to-Case Thermal Resistance (θ_{JC})
   (Note 2) ....1.5°C/W
Lead Temperature (soldering) ....+300°C

Note 1: Signals on IN_, X_, OUT_, D_, TX_, HPD_, RX_, or AUX_, LE, SEL exceeding V_{DD} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, see www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V ±10%, T_A =T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog Signal Range	IN_, X_, OUT_, D_, TX_, HPD_, RX_, AUX_		-0.1		(V_{DD} - 1.8)	V
Voltage Between IN and D/TX, X and HPD/RX1, and OUT and AUX/RX0	$|V_{IN\_} - V_{TX\_}|$, $|V_{IN\_} - V_{D\_}|$, $|V_{X\_} - V_{HPD\_}|$, $|V_{X\_} - V_{RX1\_}|$, $|V_{OUT\_} - V_{AUX\_}|$, $|V_{OUT\_} - V_{RX0\_}|$		0		1.8	V
On-Resistance	R_{ON}	$I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$ = 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V, +1.2V		8		Ω
On-Resistance Match Between Pairs of Same Channel	ΔR_{ON}	V_{DD} = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$= 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V (Notes 4, 5)		0.1	2	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{DD} = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$= 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V (Notes 4, 5)		1.5	4	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{DD} = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$= 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V, +1.2V (Notes 5, 6)		0.3	1.5	Ω

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DisplayPort/PCIe Passive Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D_ or TX_/ HPD_ or RX1_/ AUX_ or RX0_ Off-Leakage Current	$I_{D\_}$ (OFF) $I_{TX\_}$ (OFF) $I_{HPD\_}$ (OFF) $I_{RX1\_}$ (OFF) $I_{AUX\_}$ (OFF) $I_{RX0\_}$ (OFF)	V_{DD} = +3.6V , $V_{IN\_}$ = $V_{X\_}$ = $V_{OUT\_}$ = 0V, +1.2V; $V_{D\_}$ or $V_{TX\_}$, $V_{HPD\_}$ or $V_{RX1\_}$, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.2V, 0V	-1		+1	µA
IN_/X_/OUT_ On-Leakage Current	$I_{IN\_}$ (ON) $I_{X\_}$ (ON) $I_{OUT\_}$ (ON)	V_{DD} = +3.6V , $V_{IN\_}$ = $V_{X\_}$ = $V_{OUT\_}$ = 0V, +1.2V; $V_{D\_}$ or $V_{TX\_}$ = $V_{IN\_}$ or unconnected, $V_{HPD\_}$ or $V_{RX1\_}$ = $V_{X\_}$ or unconnected, $V_{AUX\_}$ or $V_{RX0\_}$ = $V_{OUT\_}$ or unconnected	-1		+1	
DIGITAL SIGNALS						
SEL to Switch Turn-On Time	t_{ON_SEL}	$V_{D\_}$ or $V_{TX\_}$ = +1.0V, R_L = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, R_L = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, R_L = 50Ω, LE = V_{DD}, C_L = 100pf (Figure 1)		55	120	ns
SEL to Switch Turn-Off Time	t_{OFF_SEL}	$V_{D\_}$ or $V_{TX\_}$ = +1.0V, R_L = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, R_L = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, R_L = 50Ω, LE = V_{DD}, C_L = 100pf (Figure 1)		8	50	ns
LE Setup Time SEL to LE	t_{SU}	$V_{D\_}$ or $V_{TX\_}$ = +1.0V, R_L = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, R_L = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, R_L = 50Ω (Figure 1)		2		ns
LE Hold Time SEL to LE	t_{HOLD}	$V_{D\_}$ or $V_{TX\_}$ = +1.0V, R_L = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, R_L = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, R_L = 50Ω, (Figure 1)		2		ns
LE Minimum Pulse-Width Low	t_W	$V_{D\_}$ or $V_{TX\_}$ = +1.0V, R_L = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, R_L = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, R_L = 50Ω (Figure 1)	40			ns
Differential Insertion Loss (Figure 2)	S_{DD21}	f = 2.5GHz		-1.5		dB
		f = 5.0GHz		-3.3		
		f = 7.5GHz		-4.9		
Differential Crosstalk (Figure 2)	S_{DDCTK}	f = 2.5GHz		-40		dB
		f = 5.0GHz		-23		
		f = 7.5GHz		-28		
Differential Off-Isolation	S_{DD21_OFF}	f = 3.0GHz		-22		dB
Differential Return Loss (Figure 2)	S_{DD11}	f = 2.8GHz		-21		dB
		f = 5.0GHz		-8		
		f = 7.5GHz		-7		

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DisplayPort/PCIe Passive Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal Data Rate	BR	R_S = R_L = 100Ω balanced		10		Gbps
Differential -3dB Bandwidth	DBW	R_S = R_L = 100Ω balanced		5		GHz
LOGIC INPUT (LE, SEL)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.5	V
Input Logic Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}	-1		+1	µA
POWER SUPPLY						
Power Supply Range	V_{DD}		3.0		3.6	V
V_{DD} Supply Current	I_{DD}	V_{IN} = 0 or V_{DD}			850	µA

Note 3: All units are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

Note 4: ΔR_{ON} = $R_{ON\ (MAX)}$ - $R_{ON\ (MIN)}$.
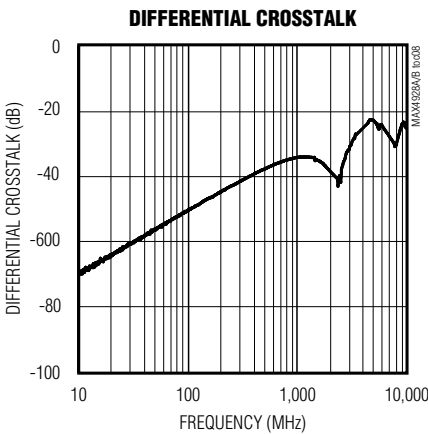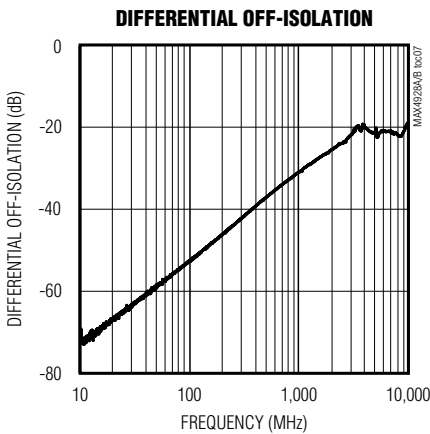
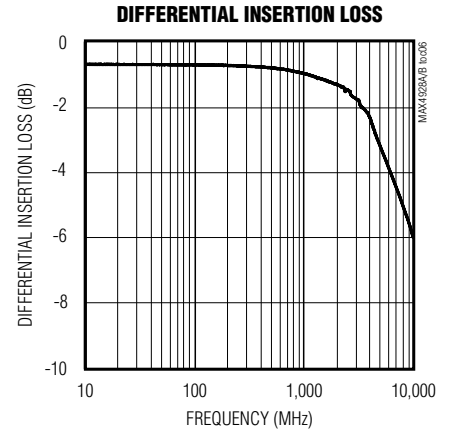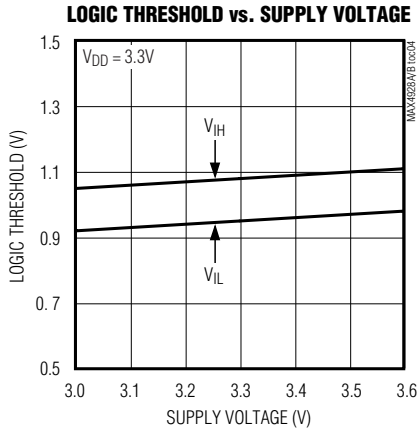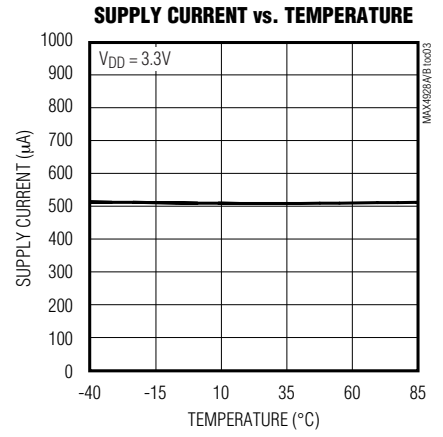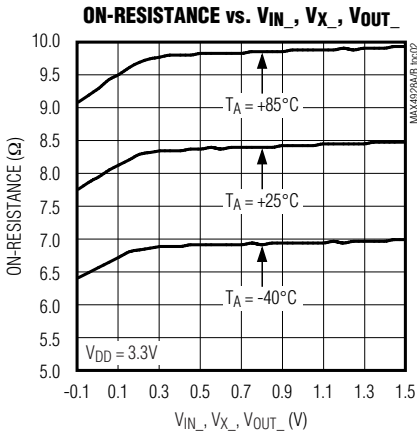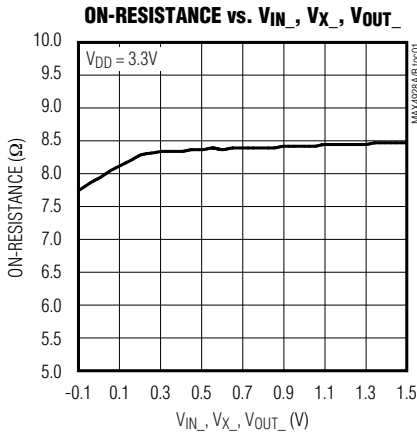**Note 5:** Guaranteed by design. Not production tested.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

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MAX4928A/MAX4928B

Typical Operating Characteristics

(T$_A$ = +25°C, unless otherwise noted.)

ON-RESISTANCE vs. V$_{IN\_}$, V$_{X\_}$, V$_{OUT\_}$

MAX4928A/B toc01

V$_{DD}$ = 3.3V

ON-RESISTANCE (Ω)

V$_{IN\_}$, V$_{X\_}$, V$_{OUT\_}$ (V)

ON-RESISTANCE vs. V$_{IN\_}$, V$_{X\_}$, V$_{OUT\_}$

MAX4928A/B toc02

T$_A$ = +85°C

T$_A$ = +25°C

T$_A$ = -40°C

V$_{DD}$ = 3.3V

ON-RESISTANCE (Ω)

V$_{IN\_}$, V$_{X\_}$, V$_{OUT\_}$ (V)

SUPPLY CURRENT vs. TEMPERATURE

MAX4928A/B toc03

V$_{DD}$ = 3.3V

SUPPLY CURRENT (µA)

TEMPERATURE (°C)

LOGIC THRESHOLD vs. SUPPLY VOLTAGE

MAX4928A/B toc04

V$_{DD}$ = 3.3V

V$_{IH}$

V$_{IL}$

LOGIC THRESHOLD (V)

SUPPLY VOLTAGE (V)

TURN-ON/OFF TIME vs. SUPPLY VOLTAGE

MAX4928A/B toc05

t$_{ON\_SEL}$

t$_{OFF\_SEL}$

TURN-ON/OFF TIME (ns)

SUPPLY VOLTAGE (V)

DIFFERENTIAL INSERTION LOSS

MAX4928A/B toc06

DIFFERENTIAL INSERTION LOSS (dB)

FREQUENCY (MHz)

DIFFERENTIAL OFF-ISOLATION

MAX4928A/B toc07

DIFFERENTIAL OFF-ISOLATION (dB)

FREQUENCY (MHz)

DIFFERENTIAL CROSSTALK

MAX4928A/B toc08

DIFFERENTIAL CROSSTALK (dB)

FREQUENCY (MHz)

DIFFERENTIAL RETURN LOSS

MAX4928A/B toc09

DIFFERENTIAL RETURN LOSS (dB)

FREQUENCY (MHz)

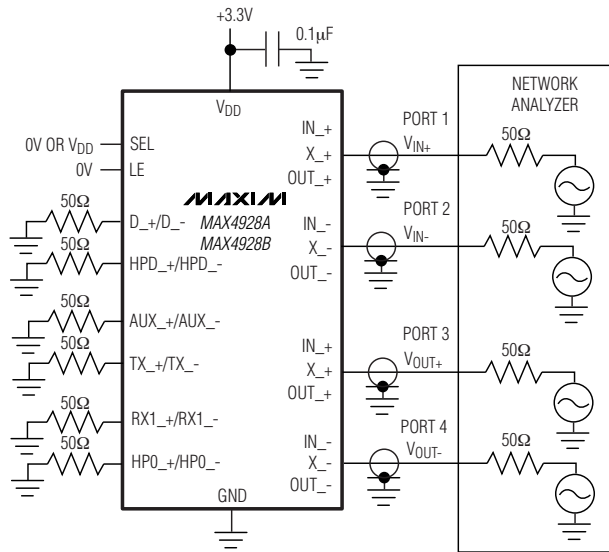# DisplayPort/PCIe Passive Switches

Figure 1. Switching Time
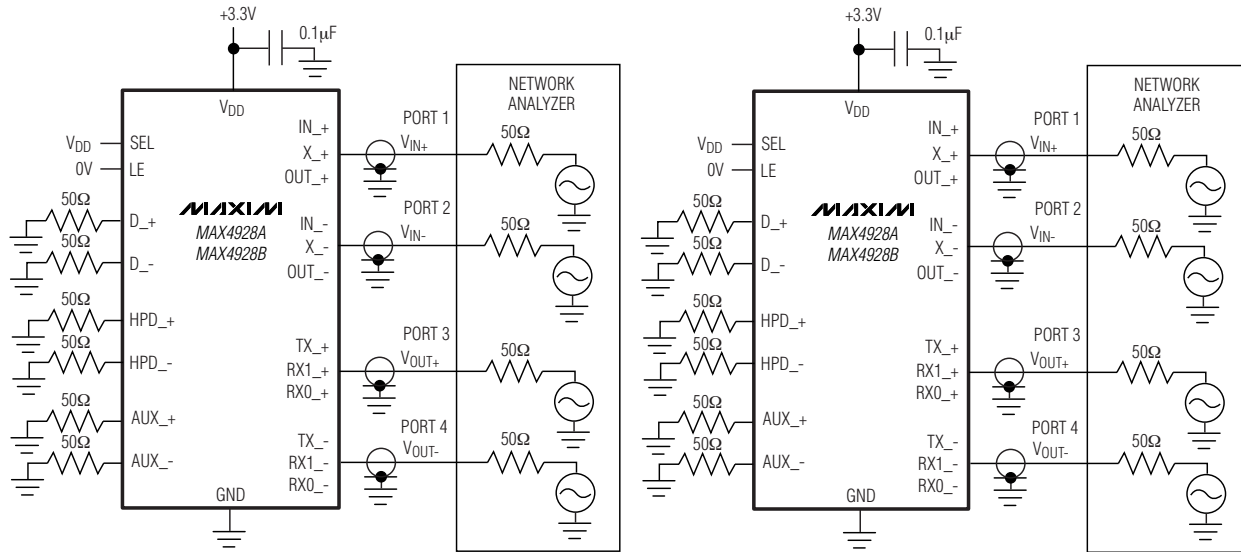
DIFFERENTIAL INSERTION-LOSS/DIFFERENTIAL RETURN LOSS

$$\text{DIFFERENTIAL INSERTION-LOSS} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

DIFFERENTIAL OFF-ISOLATION

$$\text{DIFFERENTIAL OFF-ISOLATION} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

DIFFERENTIAL CROSSTALK

$$\text{DIFFERENTIAL CROSSTALK} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

MEASUREMENTS ARE STANDARDIZED AGAINST SHORTS AT IC TERMINALS.
DIFFERENTIAL OFF-ISOLATION IS MEASURED BETWEEN IN_ AND "OFF" D_ OR TX_, X_ AND "OFF" HPD_ OR RX1_, OUT_ AND "OFF" AUX_ OR RX0_ TERMINAL ON EACH SWITCH.
DIFFERENTIAL ON-LOSS IS MEASURED BETWEEN IN_ AND "ON" D_ OR TX_, X_ AND "ON" HPD_ OR RX1_, OUT_ AND "ON" AUX_ OR RX0_ TERMINAL ON EACH SWITCH.
DIFFERENTIAL CROSSTALK IS MEASURED BETWEEN ANY TWO PAIRS.

Figure 2. Differential On-Loss, Differential Off-Isolation, and Differential Crosstalk

DisplayPort/PCIe Passive Switches

PIN		NAME	FUNCTION
MAX4928A	**MAX4928B**		
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Ground
2	4	IN0+	Analog Switch 1—Common Positive Terminal
3	5	IN0-	Analog Switch 1—Common Negative Terminal
4	7	IN1+	Analog Switch 2—Common Positive Terminal
5	8	IN1-	Analog Switch 2—Common Negative Terminal
6, 17, 22, 27, 34, 50, 55	6, 17, 22, 27, 34, 50, 55	V_{DD}	Positive Supply Voltage Input. Connect V_{DD} to a +3.0V to +3.6V supply voltage. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. See the *Board Layout* section.
7	9	IN2+	Analog Switch 3—Common Positive Terminal
8	10	IN2-	Analog Switch 3—Common Negative Terminal
9	12	IN3+	Analog Switch 4—Common Positive Terminal
10	13	IN3-	Analog Switch 4—Common Negative Terminal
12	14	OUT+	Analog Switch 5—Common Positive Terminal
13	15	OUT-	Analog Switch 5—Common Negative Terminal
14	18	X+	Analog Switch 6—Common Positive Terminal
15	19	X-	Analog Switch 6—Common Negative Terminal
18	2	SEL	Control Signal Input
19	3	LE	Latch Enable Input
23	30	HPD2	Analog Switch 6—Normally Open Negative Terminal
24	31	HPD1	Analog Switch 6—Normally Open Positive Terminal
25	32	AUX-	Analog Switch 5—Normally Open Negative Terminal
26	33	AUX+	Analog Switch 5—Normally Open Positive Terminal
30	23	RX1-	Analog Switch 6—Normally Closed Negative Terminal
31	24	RX1+	Analog Switch 6—Normally Closed Positive Terminal
32	25	RX0-	Analog Switch 5—Normally Closed Negative Terminal
33	26	RX0+	Analog Switch 5—Normally Closed Positive Terminal
36	44	D3-	Analog Switch 4—Normally Open Negative Terminal
37	45	D3+	Analog Switch 4—Normally Open Positive Terminal
38	46	D2-	Analog Switch 3—Normally Open Negative Terminal
39	47	D2+	Analog Switch 3—Normally Open Positive Terminal
40	51	D1-	Analog Switch 2—Normally Open Negative Terminal
41	52	D1+	Analog Switch 2—Normally Open Positive Terminal
42	53	D0-	Analog Switch 1—Normally Open Negative Terminal
43	54	D0+	Analog Switch 1—Normally Open Positive Terminal
44	36	TX3-	Analog Switch 4—Normally Closed Negative Terminal
45	37	TX3+	Analog Switch 4—Normally Closed Positive Terminal
46	38	TX2-	Analog Switch 3—Normally Closed Negative Terminal

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PIN		NAME	FUNCTION
MAX4928A	MAX4928B		
47	39	TX2+	Analog Switch 3—Normally Closed Positive Terminal
51	40	TX1-	Analog Switch 2—Normally Closed Negative Terminal
52	41	TX1+	Analog Switch 2—Normally Closed Positive Terminal
53	42	TX0-	Analog Switch 1—Normally Closed Negative Terminal
54	43	TX0+	Analog Switch 1—Normally Closed Positive Terminal
—	—	EP	Exposed Pad. Connect EP to GND. Exposed pad internally connected to GND.

Detailed Description

The MAX4928A/MAX4928B high-speed passive switches route PCI Express (PCIe) data and/or DisplayPort signals between two possible destinations. The MAX4928A/MAX4928B are ideal for routing signals between a graphics memory controller hub (GMCH) and either a DisplayPort or PCIe connector.

The MAX4928A/MAX4928B feature a single digital control input (SEL) to switch signal paths and a latch input (LE) that holds the switches in a given state.

Digital Control Input (SEL)

The MAX4928A/MAX4928B provide a single digital control input (SEL) to select the signal path between the IN_ and D_/TX_, X_ and HPD_/RX1_, and OUT_ and AUX_/RX0_ channels. The truth tables for the MAX4928A/MAX4928B are depicted in the *Functional Diagrams/Truth Table*. Drive SEL rail-to-rail to minimize power consumption.

Latch Control Input (LE)

The MAX4928A/MAX4928B provide a single digital control input (LE) to latch the signal paths between the IN_ and D_/TX_, X_ and HPD_/RX1_, and OUT_ and AUX_/RX0_ channels. When LE is driven high, the switches are held in their previous state, regardless of the input signal to SEL. Drive LE rail-to-rail to minimize power consumption.

Analog Signal Levels

The MAX4928A/MAX4928B accept standard PCIe signals to a maximum of (V_{DD} - 1.8V). Signals on the IN_+ channels are routed to either the D_+ or TX_+ channels, signals on the X+ channel are routed to either HPD1 or RX1+ channels, and signals on the OUT+ channel are routed to either AUX+ or RX0+ channels. Signals on the IN_- channels are routed to either the D_- or TX_- channels, signals on the X- channel are routed to either HPD2 or RX1- channels, and signals on the OUT- channel are routed to either AUX- or RX0- channels. The MAX4928A/MAX4928B are bidirectional switches, allowing IN_, X_, OUT_, D_, TX_, HPD_, RX_, and AUX_ to be used as either inputs or outputs.

Applications Information

DisplayPort/PCIe Switching

The MAX4928A/MAX4928B primary applications are aimed to switch between a GMCH and either a DisplayPort or PCIe connector. The MAX4928A/MAX4928B contain n-channel switches to permit differential signals to be selected between a PCIe Gen II socket or to a DisplayPort connector. Each device handles up to six pairs of signals. The DisplayPort signal is an AC-coupled 8b/10b encoded differential signal ranging up to 2.7 Gbps. The PCIe Gen I and Gen II signals are AC-coupled, 8b/10b encoded differential signals ranging up to 5.0Gbps.

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to large ground planes.
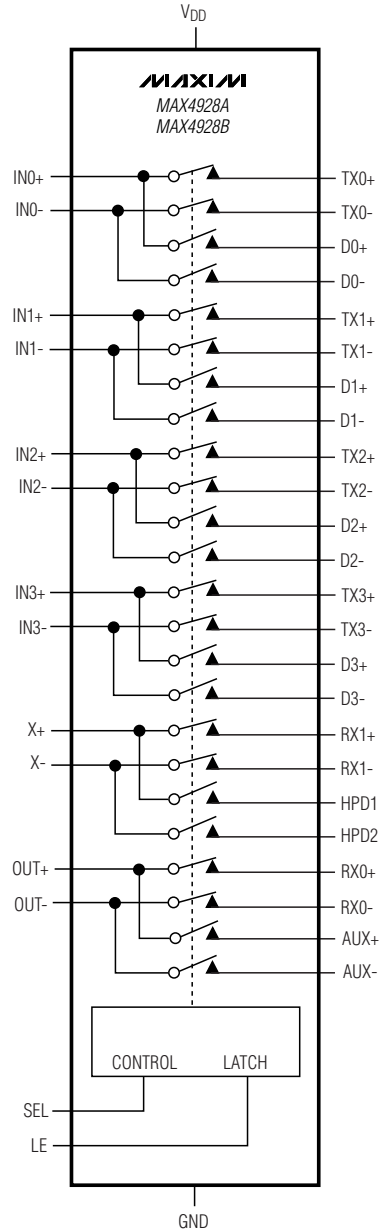
Chip Information

PROCESS: CMOS

MAX4928A/MAX4928B

Functional Diagram/Truth Table

LE	SEL	IN_ TO TX_, X_ TO RX1_, OUT_ TO RX0_	IN_ TO D0_, X_ TO HPD_, OUT_ TO AUX_
1	X	NO CHANGE	NO CHANGE
0	0	ON	OFF
0	1	OFF	ON

X = DON'T CARE.

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Typical Operating Circuit

MAX4928A/MAX4928B

MAX4928A/MAX4928B
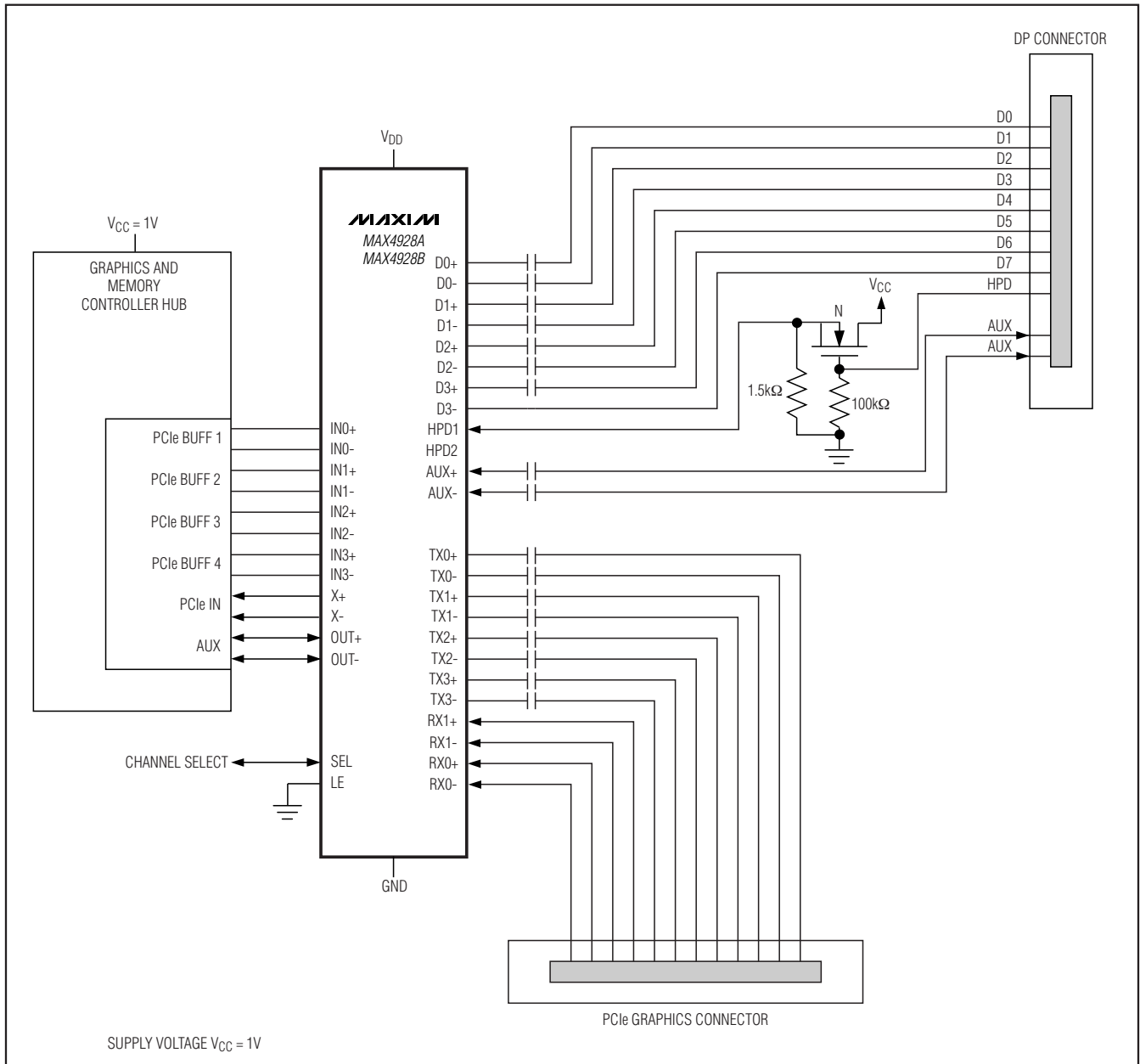
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T56511-1	**21-0187**

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DisplayPort/PCIe Passive Switches

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	8/08	Changed functional diagram and limits	1, 2, 11

MAX4928A/MAX4928B