

## ISOLATED MONITORING ADC

### Features

- ADC
  - 3 input channels
  - 10-bit resolution
  - 2  $\mu$ s conversion time
- Isolated serial I/O port
  - UART (Si8900)
  - I<sup>2</sup>C/SMbus (Si8901)
  - 2.5 MHz SPI port (Si8902)
- Transient immunity: 45 kV/ $\mu$ s (typ)
- Temperature range: -40 to +85 °C
- >60-year life at rated working voltage
- CSA component notice 5A approval
- IEC 60950, 61010, 60601
- VDE/IEC 60747-5-2
- UL1577 recognized
  - Up to 5 kVrms for 1 minute

### Applications

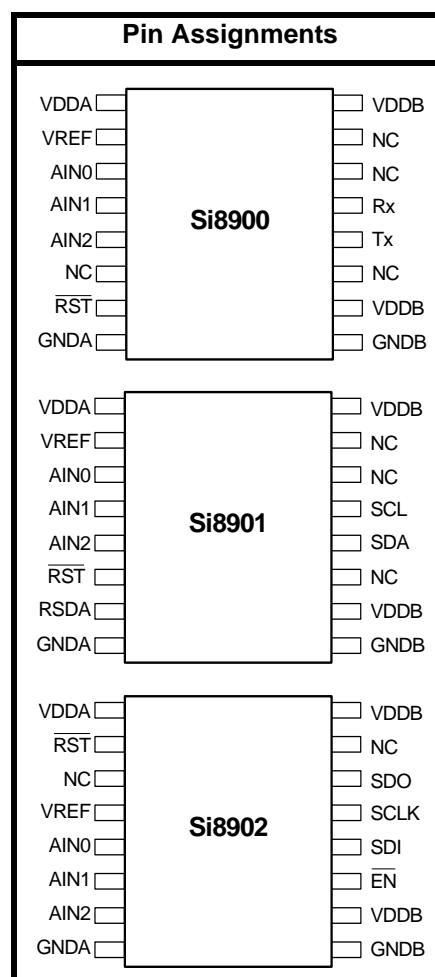
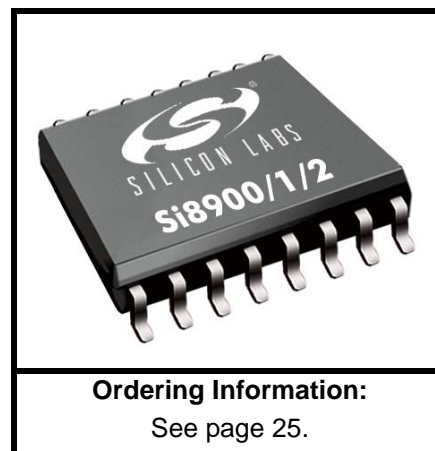
- Isolated data acquisition
- AC mains monitor
- Solar inverters
- Isolated temp/humidity sensing
- Switch mode power systems
- Telemetry

### Description

The Si8900/1/2 series of isolated monitoring ADCs are useful as linear signal galvanic isolators, level shifters, and/or ground loop eliminators in many applications including power-delivery systems and solar inverters. These devices integrate a 10-bit SAR ADC subsystem, supervisory state machine and isolated UART (Si8900), I<sup>2</sup>C/SMbus port (Si8901), or SPI Port (Si8902) in a single package. Based on Silicon Labs' proprietary CMOS isolation technology, ordering options include a choice of 2.5 or 5 kV isolation ratings. All products are safety certified by UL, CSA, and VDE. The Si8900/1/2 devices offer a typical common-mode transient immunity performance of 45 kV/ $\mu$ s for robust performance in noisy and high-voltage environments. Devices in this family are available in 16-pin SOIC wide-body packages.

### Safety Approval

- UL 1577 recognized
  - Upto 5 kVrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010, 60601
- VDE certification conformity
- IED 60747-5-2 (VDE 0884 Part 2)





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# Si8900/1/2

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

| Parameter                  | Symbol    | Condition                                 | Min | Typ | Max  | Unit |
|----------------------------|-----------|---|-----|-----|------|------|
| Input Side Supply Voltage  | $V_{DDA}$ | With respect to GND1                      | 2.7 | —   | 3.6  | V    |
| Input Side Supply Current  | $I_{DDA}$ | $V_{DDA} = 3.3$ V, Si890x active          | —   | 10  | 13.3 | mA   |
|                            |           | $V_{DDA} = 3.3$ V, Si890x idle            | —   | 8.6 | 11.4 |      |
| Output Side Supply Voltage | $V_{DDB}$ | With respect to GND2                      | 2.7 | —   | 5.5  | V    |
| Output Side Supply Current | $I_{DDB}$ | $V_{DDB} = 3.3$ V to 5.5 V, Si890x active | —   | 4.4 | 5.8  | mA   |
|                            |           | $V_{DDB} = 3.3$ V to 5.5 V, Si890x idle   | —   | 3.3 | 3.9  |      |
| Operating Temperature      | $T_A$     |   | -40 | —   | +85  | °C   |

**Table 2. Electrical Specifications**

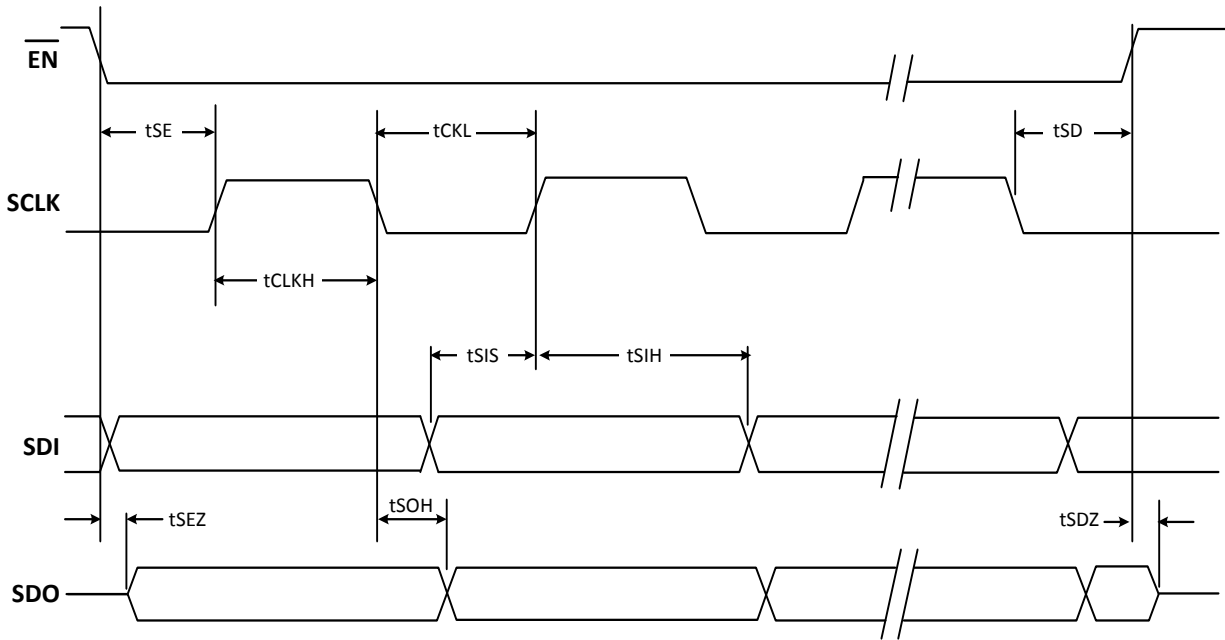
| Parameter                 | Symbol     | Test Condition                             | Min | Typ  | Max       | Unit   |
|---------------------------|------------|--|-----|------|-----------|--------|
| <b>ADC</b>                |            |  |     |      |           |        |
| Resolution                | R          |  | 10  |      |           | bits   |
| Integral Nonlinearity     | INL        | $V_{REF} = 2.4$ V                          | —   | ±0.5 | ±1        | LSB    |
| Differential Nonlinearity | DNL        | $V_{REF} = 2.4$ V,<br>Guaranteed Monotonic | —   | ±0.5 | ±1        | LSB    |
| Offset Error              | OFS        |  | -2  | 0    | +2        | LSB    |
| Full Scale Error          | FSE        |  | -2  | 0    | +2        | LSB    |
| Offset Tempco             | $T_{OS}$   |  | —   | 45   | —         | ppm/°C |
| Input Voltage Range       | $V_{IN}$   |  | 0   |      | $V_{REF}$ | V      |
| Sampling Capacitance      | $C_{IN}$   |  | —   | 5    | —         | pF     |
| Input MUX Impedance       | $R_{MUX}$  |  | —   | 5    | —         | kΩ     |
| Power Supply Rejection    | PSRR       |  | —   | -70  | —         | dB     |
| Reference Voltage         | $V_{REF}$  | Default $V_{REF} = V_{DDA}$                | 0   | —    | $V_{DDA}$ | V      |
| VREF Supply Current       | $I_{VREF}$ |  | —   | 12   | —         | μA     |
| ADC Conversion Time       | $t_{CONV}$ |  |     | 2    |           | μs     |

Table 2. Electrical Specifications (Continued)

| Parameter                             | Symbol           | Test Condition   | Min                    | Typ | Max | Unit |
|---------------------------------------|------------------|--|------------------------|-----|-----|------|
| <b>Reset and Undervoltage Lockout</b> |                  |  |                        |     |     |      |
| Power-on RESET Voltage Threshold High | VRSTH            |  | —                      | —   | 1.8 | V    |
| Power-on RESET Voltage Threshold Low  | VRSTL            |  | 1.7                    | —   | —   | V    |
| VDDA Power-On Reset Ramp Time         | tRAMP            | Time from VDDA = 0 V to VDDA ≥ VRST                      | —                      | —   | 1   | ms   |
| Power-On Reset Delay Time             | tPOR             | tRAMP < 1 ms   |                        |     | 0.3 | ms   |
| Output Side UVLO Threshold            | UVLO             |  | —                      | 2.3 | —   | V    |
| Output side UVLO Hysteresis           | H                |  | —                      | 100 | —   | mV   |
| <b>Digital Inputs</b>                 |                  |  |                        |     |     |      |
| Logic High Level Input Voltage        | V <sub>IH</sub>  |  | 0.7 × V <sub>DDB</sub> | —   | —   | V    |
| Logic Low Level Input Voltage         | V <sub>IL</sub>  |  | —                      | —   | 0.6 | V    |
| Logic Input Current                   | I <sub>IN</sub>  | V <sub>IN</sub> = 0 V or V <sub>DD</sub>                 | −10                    |     | +10 | μA   |
| Input Capacitance                     | C <sub>IN</sub>  |  | —                      | 15  | —   | pF   |
| <b>Digital Outputs</b>                |                  |  |                        |     |     |      |
| Logic High Level Output Voltage       | V <sub>OH</sub>  | V <sub>DDB</sub> = 5 V,<br>I <sub>OH</sub> = −4 mA       | V <sub>DDB</sub> −0.4  | 4.8 | —   | V    |
|                                       |                  | V <sub>DDB</sub> = 3.3 V,<br>I <sub>OH</sub> = −4 mA     | 3.1                    | —   | —   | V    |
| Logic Low Level Output Voltage        | V <sub>OL</sub>  | V <sub>DDB</sub> = 3.3 to 5 V,<br>I <sub>OL</sub> = 4 mA | —                      | 0.2 | 0.4 | V    |
| Digital Output Series Impedance       | R <sub>OUT</sub> |  | —                      | 85  | —   | Ω    |
| <b>Serial Ports</b>                   |                  |  |                        |     |     |      |
| UART Bit Rate                         |                  |  | 60                     | —   | 234 | kbps |
| SMBus/I <sup>2</sup> C Bit Rate       |                  | Slave Address = 1111000x                                 | —                      | —   | 240 | kbps |
| SPI Port                              |                  |  | —                      | —   | 2.5 | Mbps |

**Table 2. Electrical Specifications (Continued)**

| Parameter   | Symbol           | Test Condition | Min | Typ | Max | Unit |
|---|------------------|----------------|-----|-----|-----|------|
| <b>SPI Port Timing</b>                                  |                  |                |     |     |     |      |
| $\overline{\text{EN}}$ Falling Edge to SCLK Rising Edge | $t_{\text{SE}}$  |                | 80  | —   | —   | ns   |
| Last Clock Edge to $\overline{\text{EN}}$ Rising        | $t_{\text{SD}}$  |                | 80  | —   | —   | ns   |
| $\overline{\text{EN}}$ Falling to SDO Valid             | $t_{\text{SEZ}}$ |                | —   | —   | 160 | ns   |
| $\overline{\text{EN}}$ Rising to SDO High-Z             | $t_{\text{SDZ}}$ |                | —   | —   | 160 | ns   |
| SCLK High Time  | $t_{\text{CKH}}$ |                | 200 | —   | —   | ns   |
| SCLK Low Time   | $t_{\text{CKL}}$ |                | 200 | —   | —   | ns   |
| SDI Valid to SCLK Sample Edge                           | $t_{\text{SIS}}$ |                | 80  | —   | —   | ns   |
| SCLK Sample Edge to SDI Change                          | $t_{\text{SIH}}$ |                | 80  | —   | —   | ns   |
| SCLK Shift Edge to SDO Change                           | $t_{\text{SOH}}$ |                | —   | —   | 160 | ns   |



**Figure 1. SPI Port Timing Characteristics**

Table 3. Thermal Characteristics

| Parameter                             | Symbol        | Test Condition | WB SOIC-16 | NB SOIC-16 | Unit                        |
|---------------------------------------|---------------|----------------|------------|------------|-----------------------------|
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ |                | 100        | 105        | $^{\circ}\text{C}/\text{W}$ |

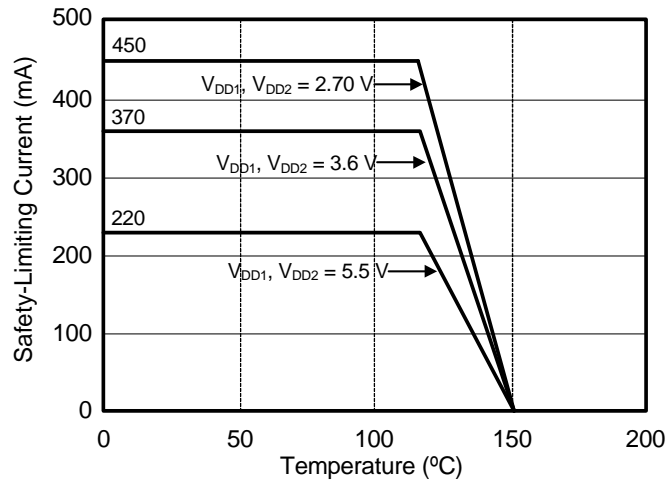


Figure 2. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

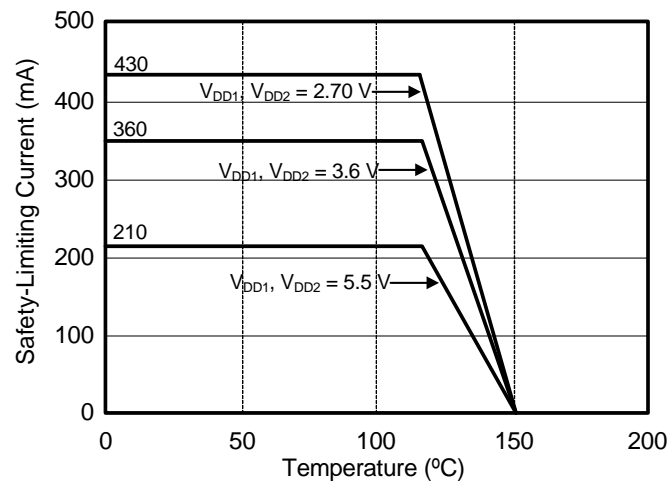


Figure 3. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

**Table 4. Absolute Maximum Ratings**

| Parameter                      | Symbol    | Min  | Typ | Max      | Unit      |
|--------------------------------|-----------|------|-----|----------|-----------|
| Storage Temperature            | $T_{STG}$ | -65  | —   | 150      | °C        |
| Ambient Temperature under Bias | $T_A$     | -40  | —   | 85       | °C        |
| Input-Side Supply Voltage      | $V_{DDA}$ | -0.5 | —   | 6.0      | V         |
| Output-Side Supply Voltage     | $V_{DDB}$ | -0.5 | —   | 6.0      | V         |
| Input/Output Voltage           | $V_I$     | -0.5 | —   | VDD +0.5 | V         |
| Output Current Drive           | $I_O$     | —    | —   | 10       | mA        |
| Lead Solder Temperature (10 s) |           | —    | —   | 260      | °C        |
| Maximum Isolation Voltage      |           | —    | —   | 6500     | $V_{RMS}$ |

**\*Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## 2. Regulatory Information

The Si8900/1/2 family is certified by Underwriters Laboratories, CSA International, and VDE. Table 5 summarizes the certification levels supported.

**Table 5. Regulatory Information**

|  |
|--|
| <p><b>CSA</b></p> <p>The Si89xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.<br/>61010-1: Up to 600 VRMS reinforced insulation working voltage; up to 600 VRMS basic insulation working voltage.<br/>60950-1: Up to 600 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage.<br/>60601-1: Up to 125 VRMS reinforced insulation working voltage; up to 380 VRMS basic insulation working voltage.</p> |
| <p><b>VDE</b></p> <p>The Si89xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.<br/>60747-5-2: Up to 1200 Vpeak for basic insulation working voltage.<br/>60950-1: Up to 600 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage.</p>  |
| <p><b>UL</b></p> <p>The Si89xx is certified under UL1577 component recognition program. For more details, see File E257455.<br/>Rated up to 5000 VRMS isolation voltage for basic protection.</p>  |

## 3. Functional Description

The Si8900/1/2 (Figure 4) are isolated monitoring ADCs that convert linear input signals into digital format and transmit the resulting data through an on-chip isolated serial port to an external master processor (typically a microcontroller). The Si890x access protocol is simple: The master configures and controls the start of ADC conversion by writing a configuration register (CNFG\_0) Command Byte to the Si890x. The master then acquires ADC conversion data by reading the Si890x serial port. Devices in this series differ only in the type of serial port. Options include a UART with on-chip baud rate generator that operates at 234 kbps max (Si8900), an SMBus/I<sup>2</sup>C port that operates at 240 kbps max (Si8901), and an SPI Port that operates at 2.5 MHz max (Si8902).

The integrated ADC subsystem consists of a three-channel analog input multiplexer (MUX) followed by a series gain amplifier (selectable 1x or 0.5x gain) and 10-bit SAR ADC. Serial-port-accessible ADC options allow the user to select an internal or external voltage reference, set the programmable gain amplifier (PGA), and select the ADC MUX address. The master can configure the Si890x to return ADC data on-demand (Demand Mode) or continuously (Burst Mode). For more information, see "CNFG\_0 Command Byte" on page 18.

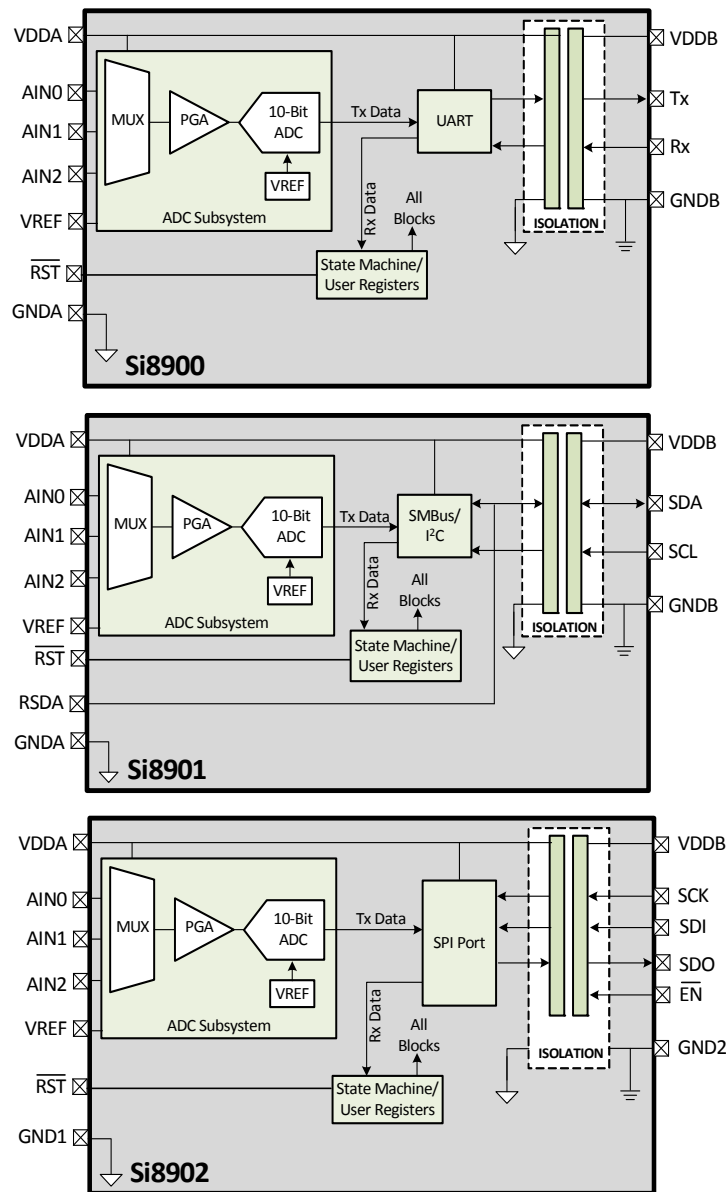
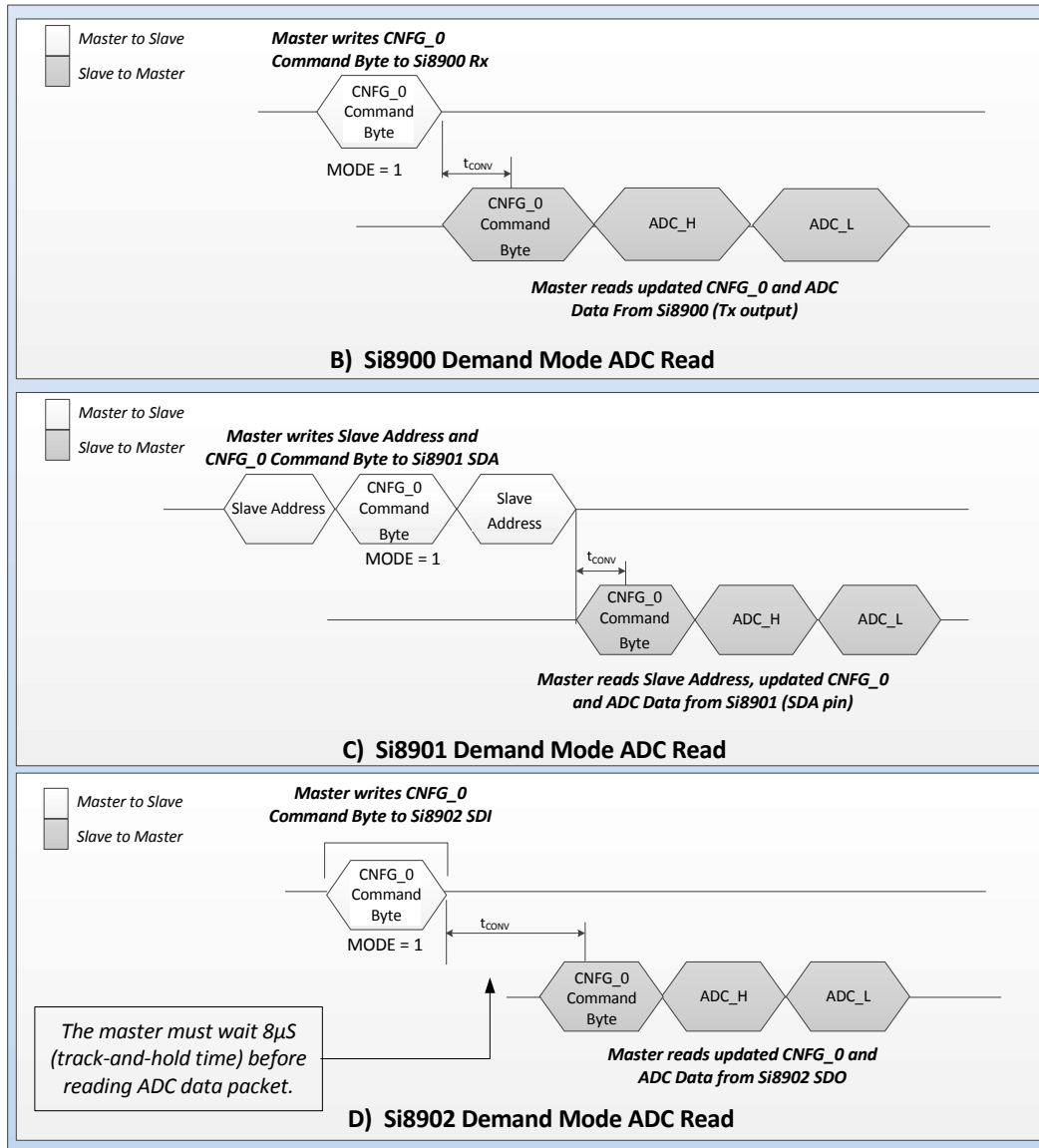


Figure 4. Si8900/1/2 Block Diagrams

## 4. ADC Data Transmission Modes

The master can access ADC read-only registers ADC\_H and ADC\_L using either Demand Mode or Burst Mode. In Demand Mode (MODE = 1), the master triggers individual A/D conversions “on-demand”. In Burst Mode (MODE = 0), the Si890x performs ADC conversions continuously.



**Figure 5. ADC Demand Mode Operation**

Referring to Figure 5A, a Demand Mode ADC read is initiated when the master writes a Command Byte to the Si8900. (The Command Byte is a copy of the CNFG\_0 register that has been properly configured by the master.) Upon receipt of the Command Byte, the Si8900 updates its CNFG\_0 register and triggers the start of an ADC conversion, at which time the master may immediately begin reading ADC conversion data from the Si8900 UART. The ADC conversion data packet contains a copy of the Command Byte for verification and two-bytes of ADC conversion data. The Si8901 (Figure 5B) ADC read transaction is identical to that of the Si8900 with the exception of the added I<sup>2</sup>C/SMBus Slave Address byte (Si8901 Slave Address is 0xF0). The Si8902 Demand Mode ADC read transaction (Figure 5C) is the same as that of the Si8900, except the master must wait 8 μs after the transmission of the Command Byte before reading the Si8902 SPI port because byte transmission time is two times shorter versus the Si8900/01.

# Si8900/1/2

The Burst Mode ADC transactions for the Si8900 (Figure 6A) and Si8901 (Figure 6B) are substantially the same. A Burst Mode ADC read is initiated when the master writes a CNFG\_0 (MODE = 0) Command Byte to the Si8900/1, which updates the CNFG\_0 register and triggers the ADC continuously. Like the Demand Mode example, the Si8901 has a Slave Address byte prior to the CNFG\_0 Command Byte. When using the Si8901, the master must write the I<sup>2</sup>C port address prior to reading the serial port. The Si8902 Burst Mode (Figure 6C) is similar to that of the Si8900/1, except the master must wait 8 μs before reading the first Burst Mode ADC data packet. After reading the first Burst Mode ADC data packet, the master may read all ADC data packets that follow without delay.

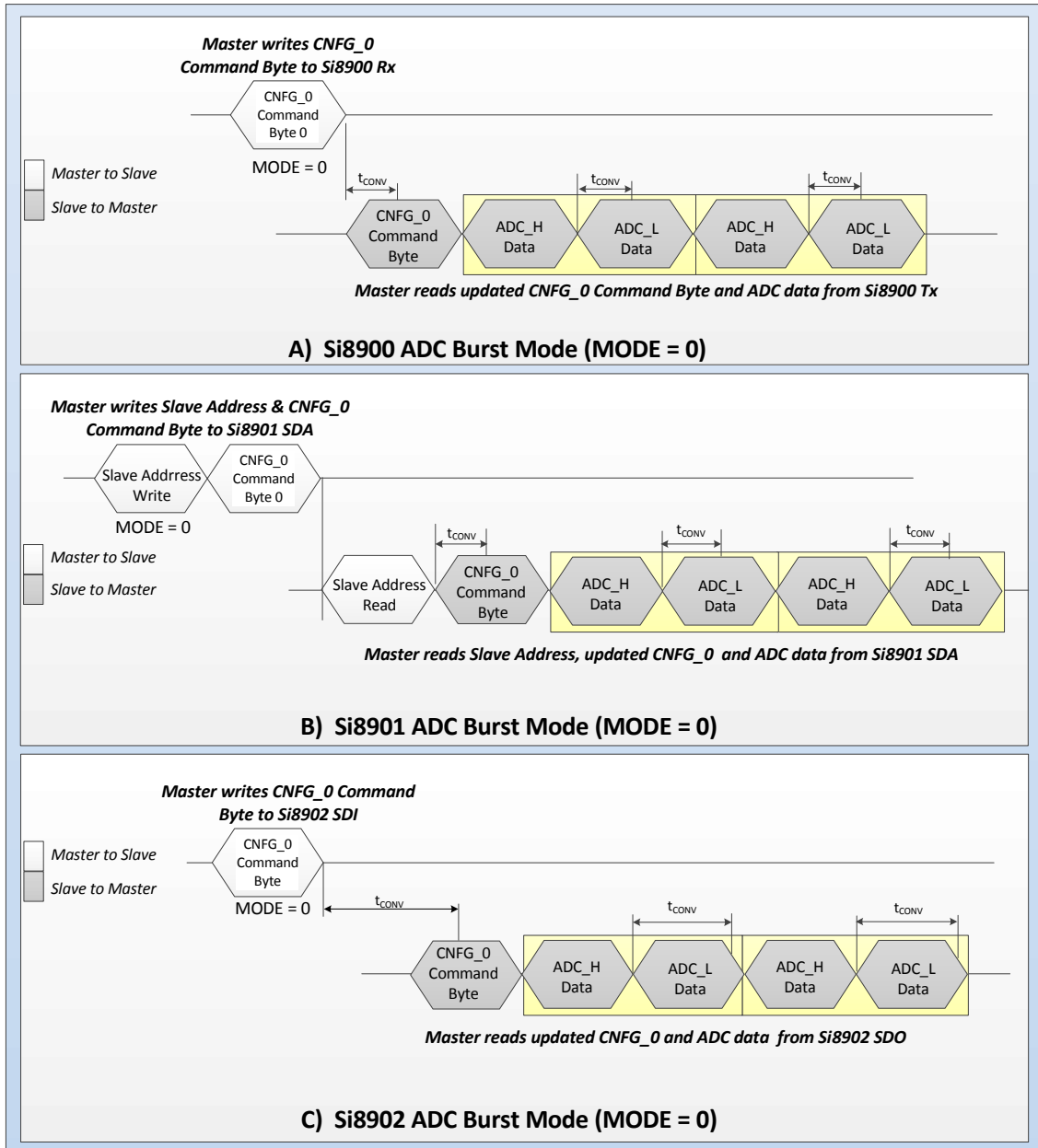


Figure 6. ADC Burst Mode Operation

## 4.1. UART (Si8900)

The UART is a two-wire interface (Tx, Rx) and operates as an asynchronous, full-duplex serial port with internal auto baud rate generator that measures the period of incoming data stream and automatically adjusts the internal baud rate generator to match. The auto baud rate detection and matching optimizes UART timing for minimum bit error rate. For more information, see “AN635: AC Line Monitoring Using the Si890x Family of Isolated ADCs”.

There are a total of 10 bits per data read/write: One start bit, eight data bits (LSB first), and one stop bit with data transmitted LSB first as shown in Figure 7. Figure 8A and Figure 8B show master/Si8900 ADC read transactions for Demand Mode and Burst Mode, respectively.

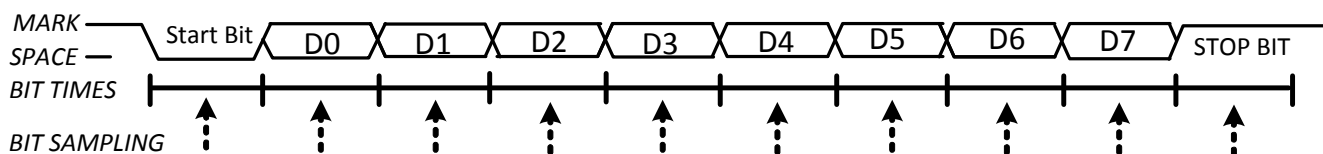


Figure 7. UART Data Byte

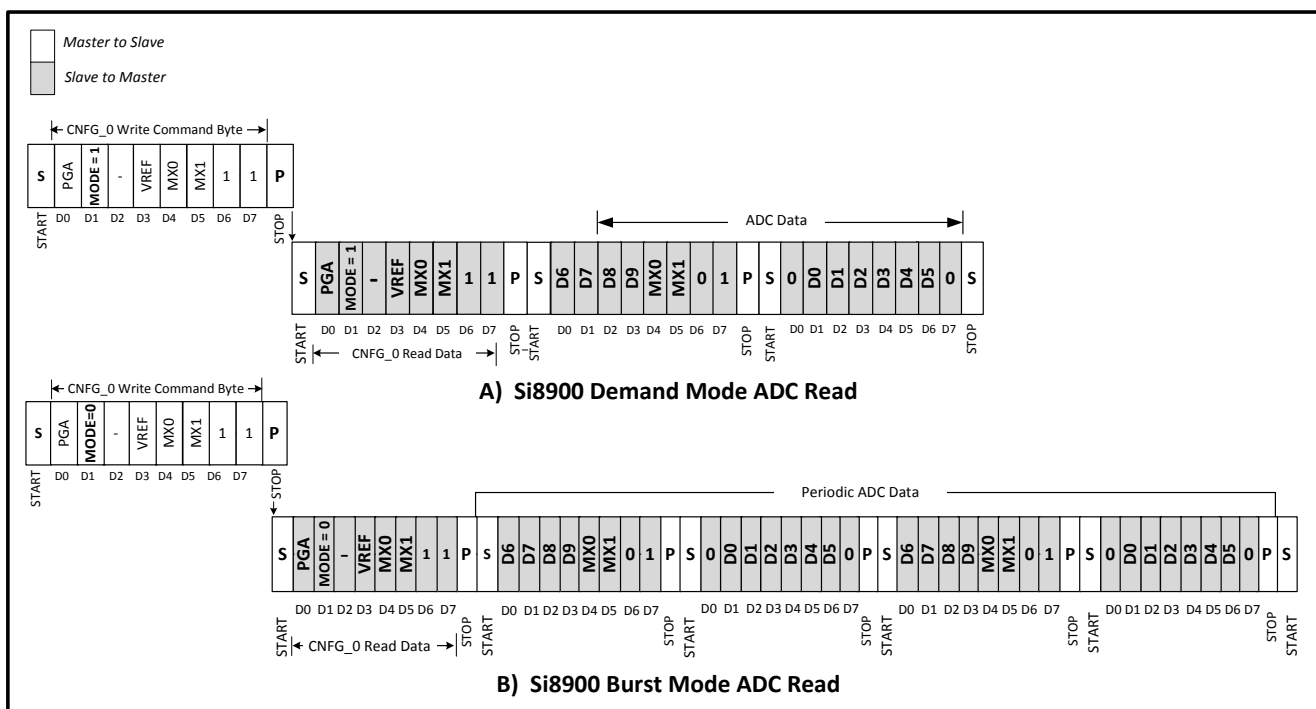


Figure 8. Si8900 ADC Read Operation

## 4.2. I<sup>2</sup>C/SMBus (Si8901)

The I<sup>2</sup>C/SMBus serial port is a two-wire serial bus where data line SDA is bidirectional and clock line SCL is unidirectional. Reads and writes to this interface by the master are byte-oriented, with the I<sup>2</sup>C/SMBus master controlling the serial data rates up to 240 kbps. The SDA and SCL lines must be pulled high through pull-up resistors of 5 kΩ or less. An Si8901 ADC read transaction begins with a START condition (“S” or Repeated START condition “SR”), which is defined as a high-to-low transition on SDA while SCL is high (Figure 9). The master terminates a transmission with a STOP condition (P), defined as a low-to-high transition on SDA while SCL is high. The data on SDA must remain stable during the high period of the SCL clock pulse because such changes in either line will be interpreted as a control command (e.g., S, P SR). SDA and SCL idle in the high state when the bus is not busy. Acknowledge bits (Figure 10) provide detection of successful data transfers, whereas unsuccessful transfers conclude with a not-acknowledge bit (NACK). Both the master and the Si8901 generate ACK and NACK bits. An ACK bit is generated when the receiving device pulls SDA low before the rising edge of the acknowledged related (ninth) SCL pulse and maintains it low during the high period of the clock pulse. A NACK bit is generated when the receiver allows SDA to be pulled high before the rising edge of the acknowledged related SCL pulse and maintains it high during the high period of the clock pulse. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master attempts communication at a later time. Figure 11A shows the I<sup>2</sup>C Slave Address Byte and CNFG\_0 byte for the Si8901. Figure 11B and Figure 11C show master/Si8901 ADC read transactions for Demand Mode and Burst Mode, respectively.

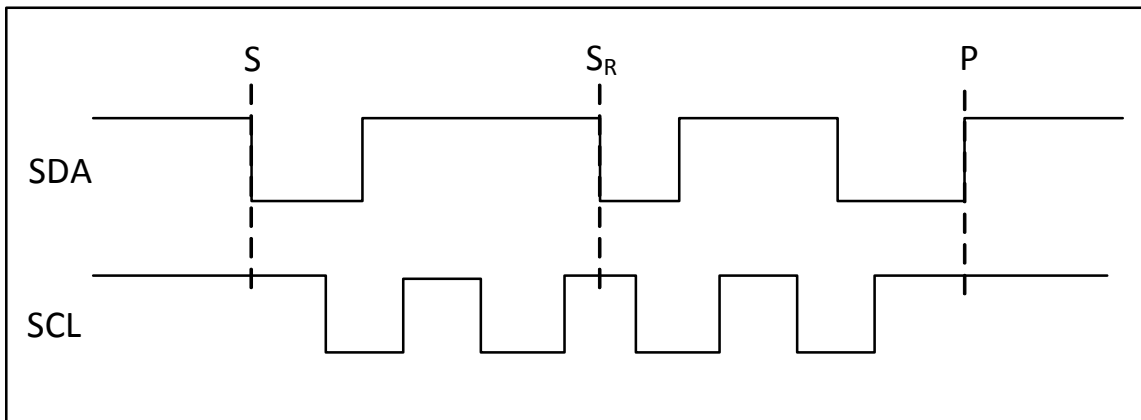


Figure 9. Start and Stop Conditions

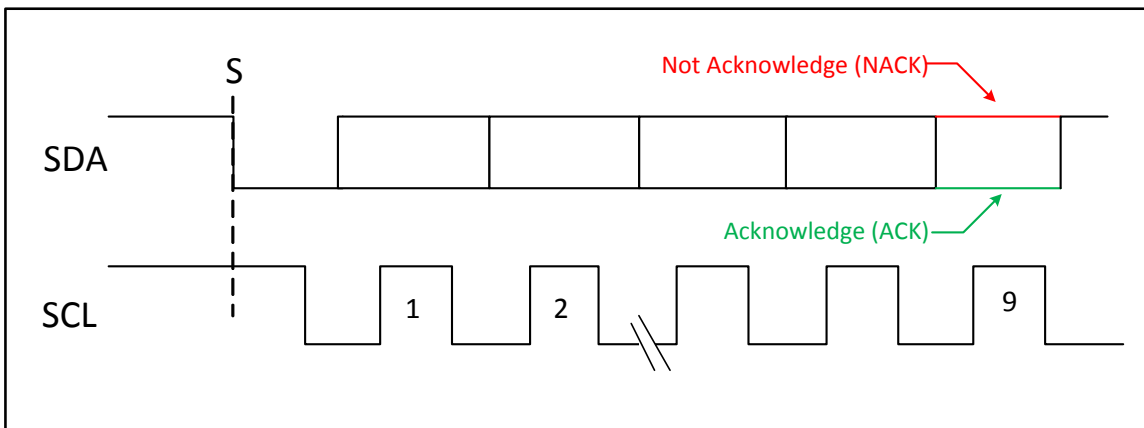


Figure 10. Acknowledge Cycle

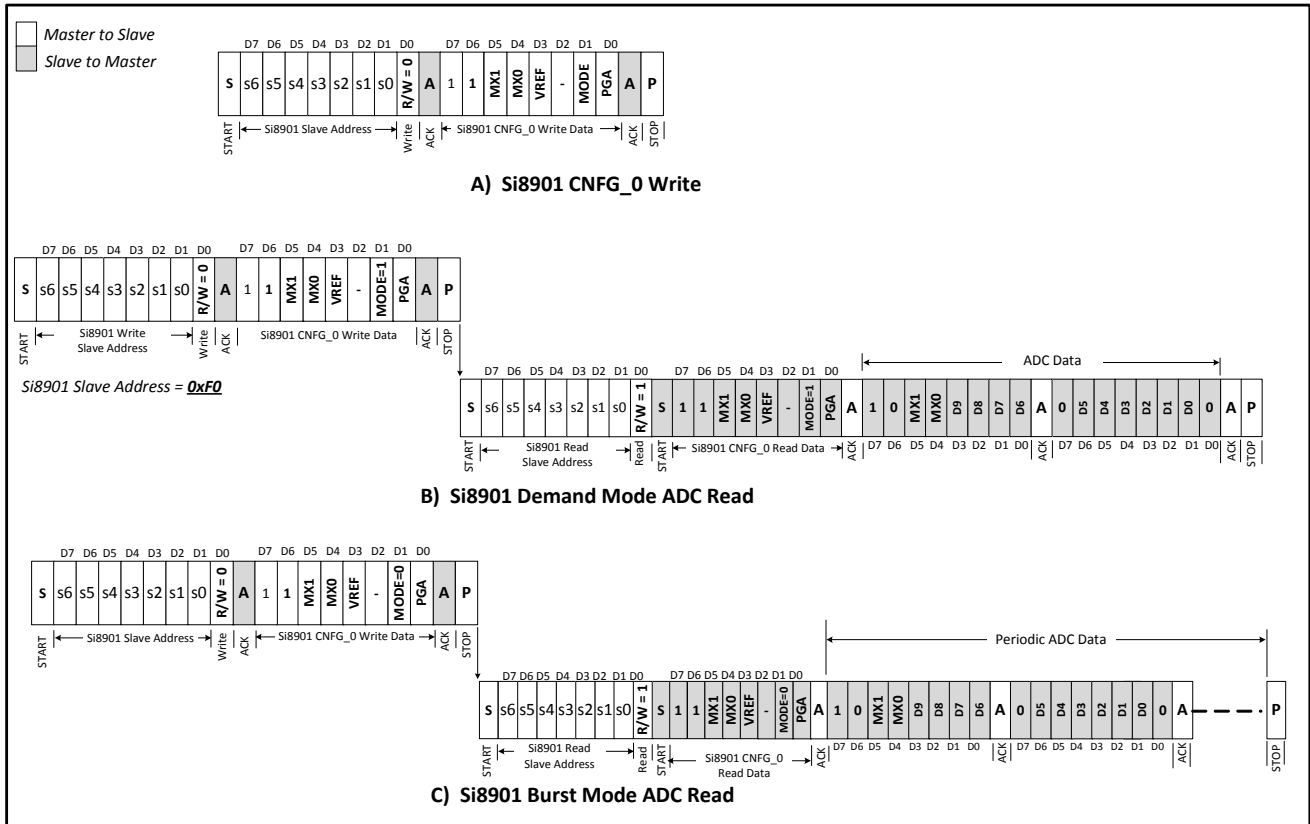


Figure 11. Si8901 ADC Read Operation

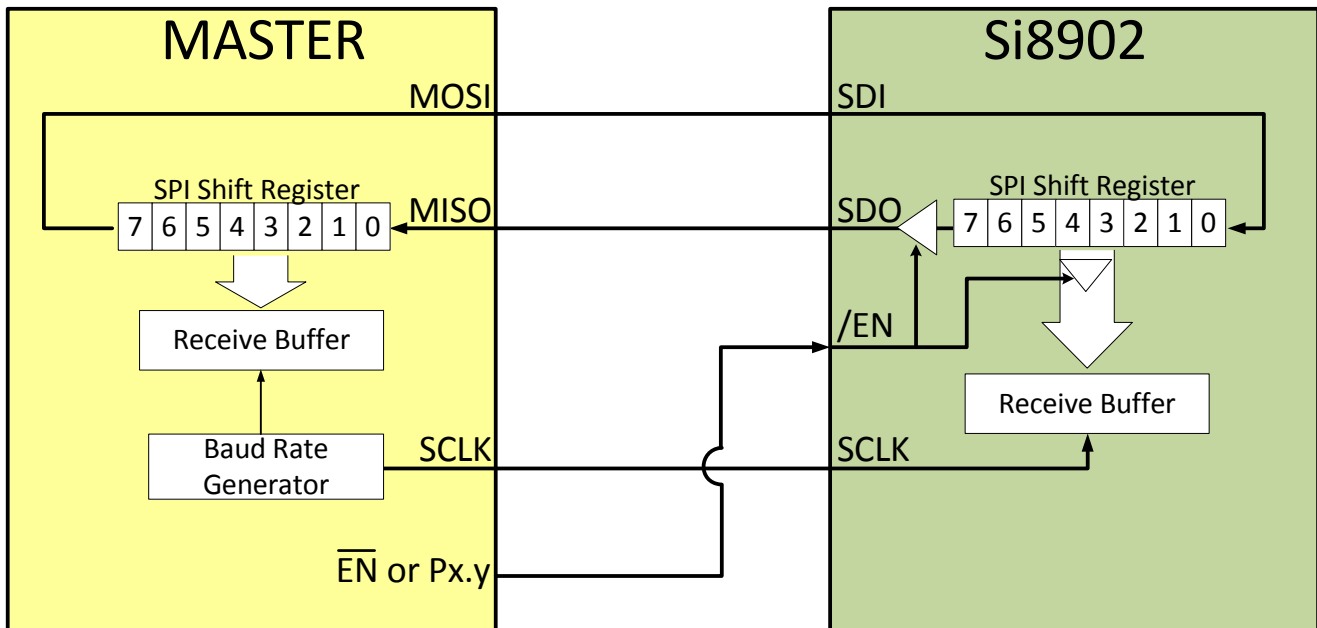
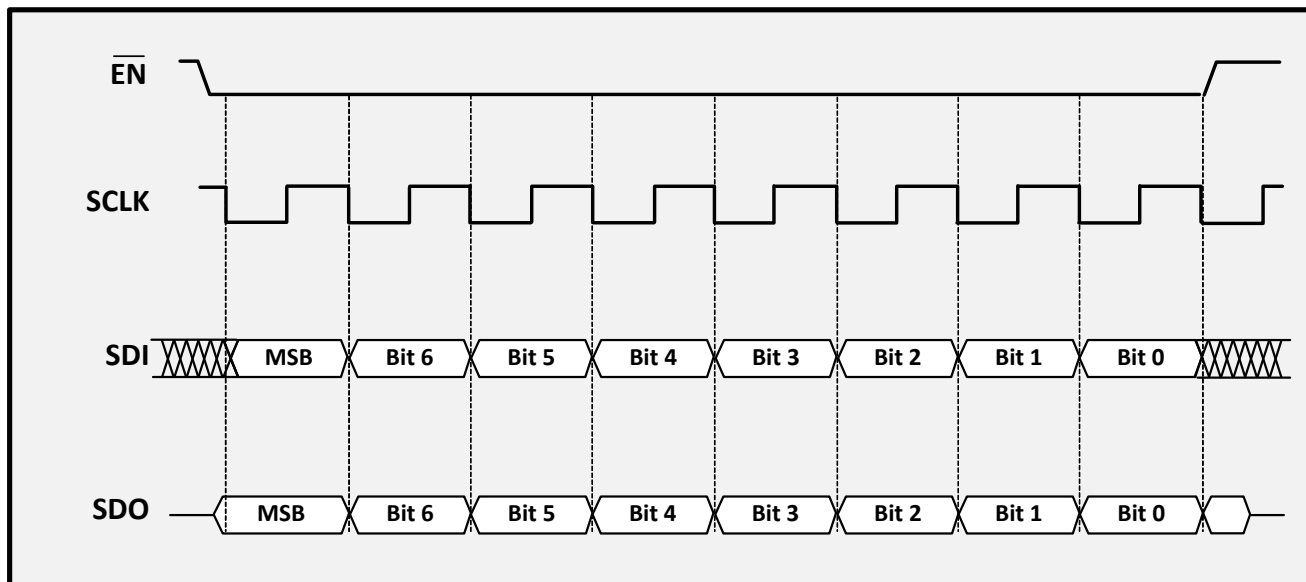


Figure 12. Master Connection to Si8902

## 4.3. SPI Port (Si8902)



**Figure 13. Si8902 Data/Clock Timing**

The Serial Peripheral Interface (SPI port) is a slave mode, full-duplex, synchronous, 4-wire serial bus that connects to the master as shown in Figure 12. The master's clock and data timing must match the Si8902 timing shown Figure 12 (for more information about clock and data timing, please see the "SPI Port" section of Table 2 on page 6).

As shown in Figure 13, an SPI bus transaction begins with the master driving  $\overline{EN}$  low and maintaining this state for the duration of the read transaction(s). The master transmits data from its master-out/slave-in terminal (MOSI) to the Si8902 serial read/write input terminal (SDI). The Si8902 transmits data to the master from its serial data-out terminal (SDO) to the master-in/slave-out terminal (MISO), and data transfer ends when the master returns  $\overline{EN}$  to the high state. Figure 14A shows the Si8902 CNFG\_0 Command Byte format, while Figures 14B and 14C show Si8902 Demand Mode and Burst Mode ADC reads.



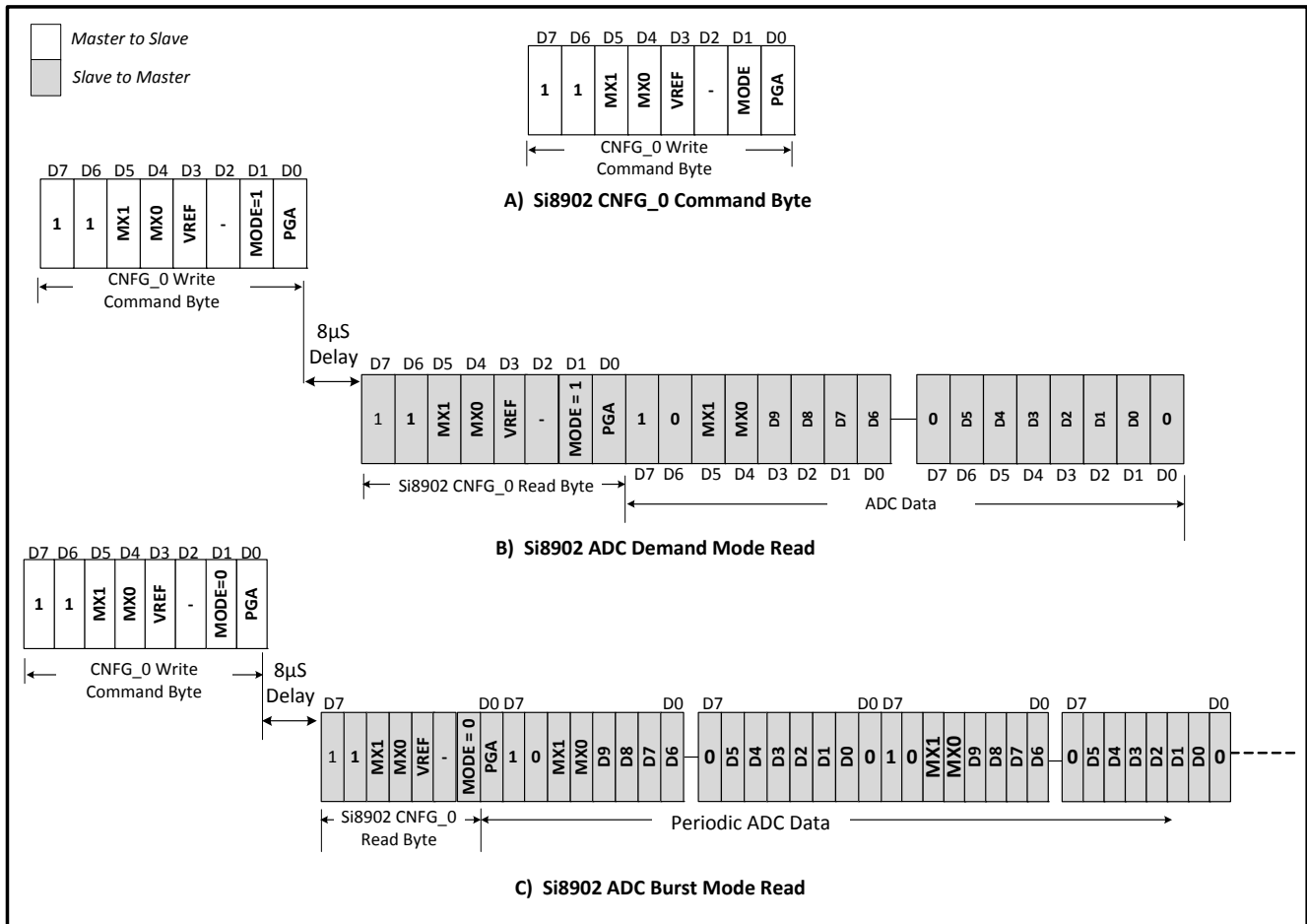


Figure 14. Si8902 ADC Read Operation

#### 4.4. Master Controller Firmware

The user's master controller must include firmware to manage the Si890x Demand and Burst operating modes and serial port control. In some cases, the master controller may also require a firmware moving average function to reduce noise. For more information on master controller firmware, see "AN637: Si890x Master Controller Recommendations", available for download at [www.silabs.com/isolation](http://www.silabs.com/isolation).

## 5. Si8900/1/2 Configuration Registers

### CNFG\_0 Command Byte

| Bit            | D7  | D6  | D5  | D4  | D3   | D2  | D1   | D0  |
|----------------|-----|-----|-----|-----|------|-----|------|-----|
| <b>Name</b>    | 1   | 1   | MX1 | MX0 | VREF | —   | MODE | PGA |
| <b>Type</b>    | R/W | R/W | R/W | R/W | R/W  | R/W | R/W  | R/W |
| <b>Default</b> | 1   | 1   | 1   | 1   | 1    | 1   | 1    | 1   |

| Bit | Name     | Function  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
|-----|----------|---|-----|-----|--------------------------|---|---|----------|---|---|------|---|---|------|---|---|------|
| 7:6 | 1,1      | Internal use. These bits are always set to 1.   |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 5:4 | MX1, MX0 | <p><b>ADC MUX Address.</b><br/>ADC MUX address selection is controlled by MX1, MX0 as follows:</p> <table border="1"> <thead> <tr> <th>MX1</th> <th>MX0</th> <th>Selected ADC MUX Channel</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Not Used</td> </tr> <tr> <td>1</td> <td>0</td> <td>AIN2</td> </tr> <tr> <td>0</td> <td>1</td> <td>AIN1</td> </tr> <tr> <td>0</td> <td>0</td> <td>AIN0</td> </tr> </tbody> </table> | MX1 | MX0 | Selected ADC MUX Channel | 1 | 1 | Not Used | 1 | 0 | AIN2 | 0 | 1 | AIN1 | 0 | 0 | AIN0 |
| MX1 | MX0      | Selected ADC MUX Channel  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 1   | 1        | Not Used  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 1   | 0        | AIN2  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 0   | 1        | AIN1  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 0   | 0        | AIN0  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 3   | VREF     | <p><b>ADC Voltage Reference Source</b><br/>VDD is selected as the reference voltage when this bit is set to 1. An externally connected voltage reference generator is selected when this bit is reset to 0.</p>   |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 2   | —        | Not used.   |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 1   | MODE     | <p><b>ADC Read Mode</b><br/>ADC Demand Mode read is enabled when this bit is 1, and Burst Mode is enabled when this bit is 0. For more information on Demand and Burst mode operation, please see "ADC Data Transmission Modes" on page 11.</p>   |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |
| 0   | PGA      | <p><b>PGA Gain Set</b><br/>PGA gain is 1 when this bit is set to 1. PGA gain is 0.5 when this bit is reset to 0.</p>  |     |     |                          |   |   |          |   |   |      |   |   |      |   |   |      |

**ADC\_H Byte**

| Bit            | D7 | D6 | D5  | D4  | D3 | D2 | D1 | D0 |
|----------------|----|----|-----|-----|----|----|----|----|
| <b>Name</b>    | 1  | 0  | MX1 | MX0 | D9 | D8 | D7 | D6 |
| <b>Type</b>    | R  | R  | R   | R   | R  | R  | R  | R  |
| <b>Default</b> | —  | —  | —   | —   | —  | —  | —  | —  |

| Bit | Name     | Function   |
|-----|----------|--|
| 7:6 | 1,0      | Internal use. These bits are always set to 1,0.  |
| 5:4 | MX1, MX0 | <b>ADC MUX Address</b><br>ADC input MUX address for the converted data in ADC_H, ADC_L.  |
| 3:0 | D9: D6   | <b>ADC conversion data bits D9:D6</b><br>Most significant 4 bits of ADC conversion data. |

**ADC\_L Byte**

| Bit            | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------|----|----|----|----|----|----|----|----|
| <b>Name</b>    | 0  | D5 | D4 | D3 | D2 | D1 | D0 | 0  |
| <b>Type</b>    | R  | R  | R  | R  | R  | R  | R  | R  |
| <b>Default</b> | —  | —  | —  | —  | —  | —  | —  | —  |

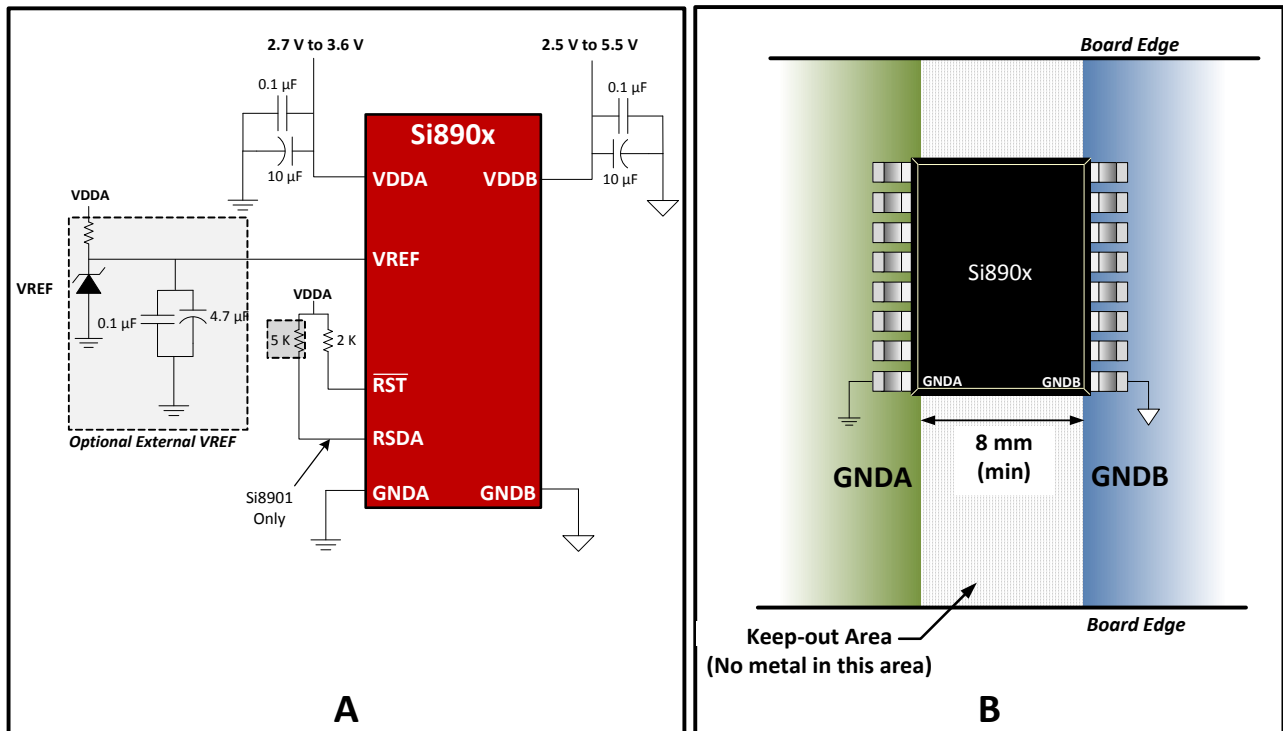
| Bit | Name  | Function  |
|-----|-------|---|
| 7   | 0     | Internal use. This bit is always set to 0.  |
| 6:1 | D5:D0 | <b>ADC Conversion Data Bits D5:D0</b><br>Least significant 6 bits of ADC conversion data. |
| 0   | 0     | Internal use. This bit is always set to 0.  |

## 6. Applications

### 6.1. Isolated Outputs

The Si890x serial outputs are internally isolated from the device input side. To ensure safety in the end-user application, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (i.e., circuits with <30 VAC) by a certain distance (creepage/clearance). If a component straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Tables published in the component standards (UL1577, IEC60747, CSA 5A) are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any circuit design that uses galvanic isolation. To enhance the robustness of a design, it is further recommended that the user also include 100 Ω resistors in series with the Si890x inputs and outputs if the system is excessively noisy. The nominal impedance of an isolated Si890x output channel is approximately 50 Ω and is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects are a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

The Si890x supply inputs must be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors at VDDA and VDDB as shown in Figure 15A. The capacitors should be placed as close to the package as possible. The Si890x uses the VDDA supply as its internal ADC voltage reference by default. A precision external reference can be installed as shown in Figure 15A and must be bypassed with a parallel combination of 0.1 μF and 4.7 μF capacitors. (Note that the CNFG\_0 VREF bit must be set to 0 when using the external reference.) The Si890x has an on-chip power on reset circuit (POR) that maintains the device in its reset state until VDDA has stabilized. A 2 kΩ pull-up resistor on RST is strongly recommended to reduce the possibility of external noise coupling into the reset input. The Si8901 will also require a 5 kΩ pull-up resistor to VDDA on the RSDA input. The Si8901 will also require a 5 kΩ pull-up resistor to VDDA on the RSDA input.



**Figure 15. Si890x Installation**

Figure 15B shows the required PCB ground configuration, where an 8 mm (min) “keep-out area” is provided to ensure adequate creepage and clearance distances between the two grounds. PCB metal traces *cannot* be present or cross through the keep-out area on the PCB top, bottom, or internal layer.

## 6.2. Device Reset

During power-up, the Si890x is held in the reset state by the internal power-on reset signal (POR) until VDDA settles above VRST. When this condition is met, a delay is initiated that maintains the Si890x in the reset state for time period tPOR, after which the reset signal is driven high allowing the Si890x to start-up. Note the maximum allowable VDD ramp time (i.e. time from 0 V to VDDA settled above VRST) is 1 ms. Slower ramp times may cause the Si890x to be released from reset before VDDA reaches the VRST level.

Figure 16 shows typical VDDA monitor reset timing where the internal reset is driven low (Si890x in reset) when VDDA falls below VRST (e.g., during a power down or VDDA brownout). The internal reset is released to its high state when VDDA again settles above VRST. External circuitry can also be used to force a reset event by driving the external  $\overline{\text{RST}}$  input low. A 2 k $\Omega$  pull-up resistor on  $\overline{\text{RST}}$  is recommended to avoid erroneous reset events from external noise coupling to the  $\overline{\text{RST}}$  input.

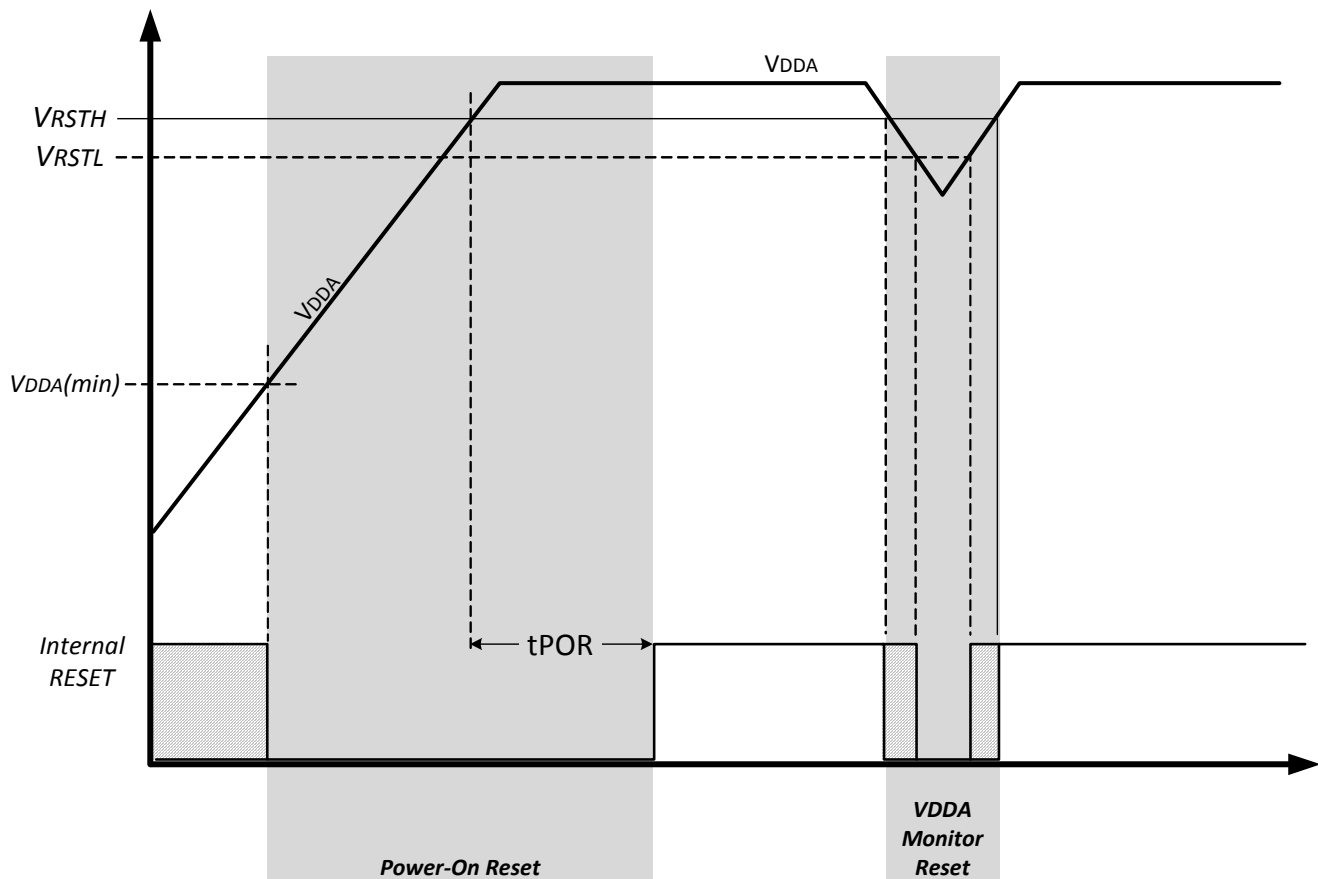


Figure 16. Si890x Power-on and Monitor Reset

## 6.3. Application Example

Figure 17 shows the Si8900 operating as a single-phase ac line voltage and current monitor. The VDDA dc bias circuit uses a low-cost 3.3 V linear regulator referenced to the neutral (white wire). The ac current is measured on ADC input AIN0. The ac line voltage is scaled by resistors R17 and R18 and level-shifted by the 1.5 V VREF. AC line current is measured using differential amplifier U1 connected across shunt resistor R1. Data is transferred to the external controller or processor via the isolated UART.

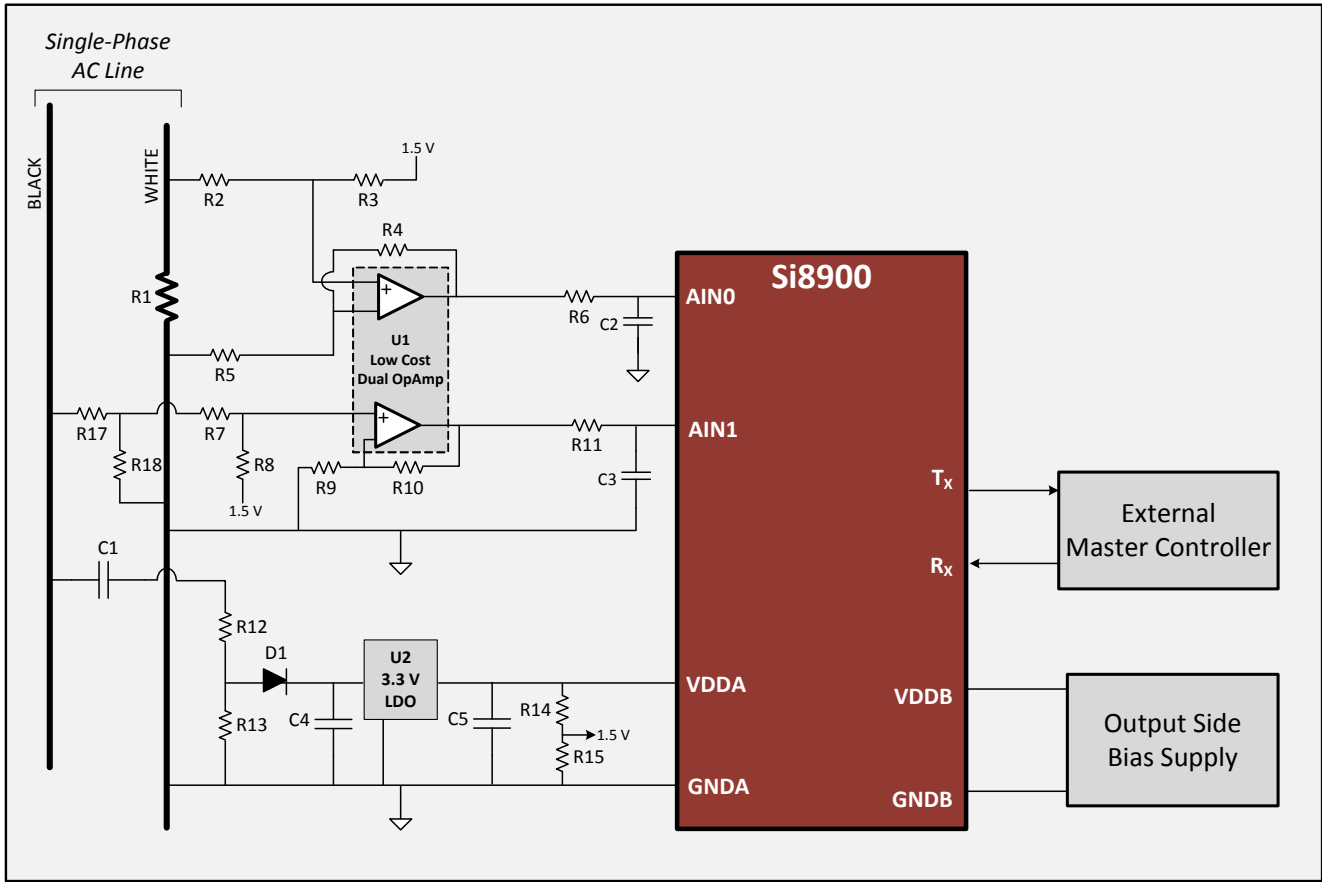


Figure 17. AC Line Monitor Application Example

## 7. Device Pin Assignments

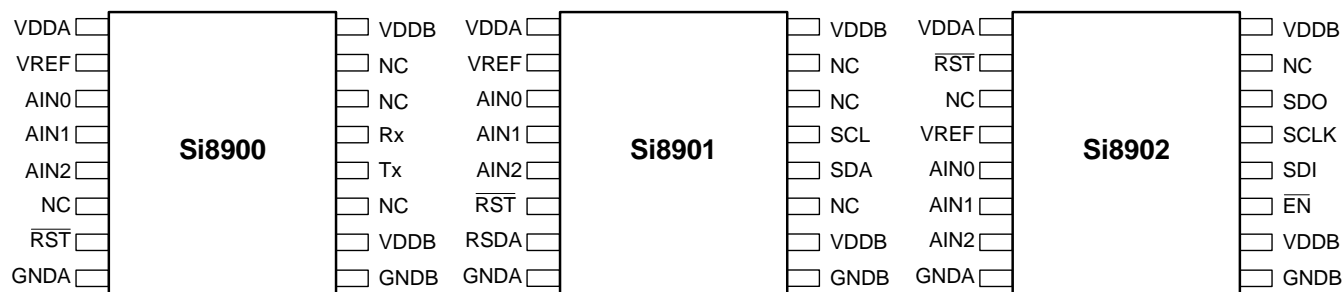


Figure 18. Si8900/1/2 Pinout (16SOW)

Table 6. Si8900/1/2 Pin Assignments

| Pin | Si8900 Pin              | Si8901 Pin              | Si8902 Pin              | Description   |
|-----|-------------------------|-------------------------|-------------------------|---|
| 1   | VDDA                    |                         |                         | Input side VDD bias voltage (typically 3.3 V)   |
| 2   | VREF                    |                         | $\overline{\text{RST}}$ | Si8900/1: External voltage reference input.<br>Si8902: Active low reset.  |
| 3   | AIN0                    | AIN0                    | NC                      | Si8900: ADC analog input channel 0.<br>Si8901: ADC analog input channel 0.<br>Si8902: No connection   |
| 4   | AIN1                    | AIN1                    | VREF                    | Si8900: ADC analog input channel 1.<br>Si8901: ADC analog input channel 1.<br>Si8902: External VREF in.                                       |
| 5   | AIN2                    | AIN2                    | AIN0                    | Si8900: ADC analog input channel 2.<br>Si8901: ADC analog input channel 2.<br>Si8902: ADC analog input channel 0.                             |
| 6   | NC                      | $\overline{\text{RST}}$ | AIN1                    | Si8900: No Connection.<br>Si8901: Active low reset.<br>Si8902: ADC analog input channel 1.  |
| 7   | $\overline{\text{RST}}$ | RSDA                    | AIN2                    | Si8900: Active low reset.<br>Si8901: RSDA bias resistor (typically 5 k $\Omega$ ).<br>Si8902: ADC analog input channel 2.                     |
| 8   | GNDA                    |                         |                         | Input side ground   |
| 9   | GNDB                    |                         |                         | Output side ground  |
| 10  | VDDB                    |                         |                         | Output side VDD bias voltage (2.7 V to 5.5 V)   |
| 11  | NC                      |                         | $\overline{\text{EN}}$  | Si8900/1: No connection. Si8902: SPI Port Enable.   |
| 12  | Tx                      | SDA                     | SDI                     | Si8900: UART unidirectional transmit output.<br>Si8901: I <sup>2</sup> C Bidirectional data input/output.<br>Si8902: SPI port Serial data in. |

# Si8900/1/2

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**Table 6. Si8900/1/2 Pin Assignments (Continued)**

| Pin | Si8900 Pin | Si8901 Pin | Si8902 Pin | Description   |
|-----|------------|------------|------------|---|
| 13  | Rx         | SCL        | SCLK       | Si8900: UART unidirectional receive input.<br>Si8901: I <sup>2</sup> C port unidirectional serial clock input.<br>Si8902: SPI port unidirectional serial clock input. |
| 14  | NC         |            | SDO        | Si8900/1: No connection.<br>Si8902: SPI port Serial data out (SDO)  |
| 15  | NC         |            |            | No connection   |
| 16  | VDDB       |            |            | Si8900/1/2: Output side VDD bias voltage (2.7 V to 5.5 V).  |



## 8. Ordering Guide

**Table 7. Product Ordering Information<sup>1,2,3</sup>**

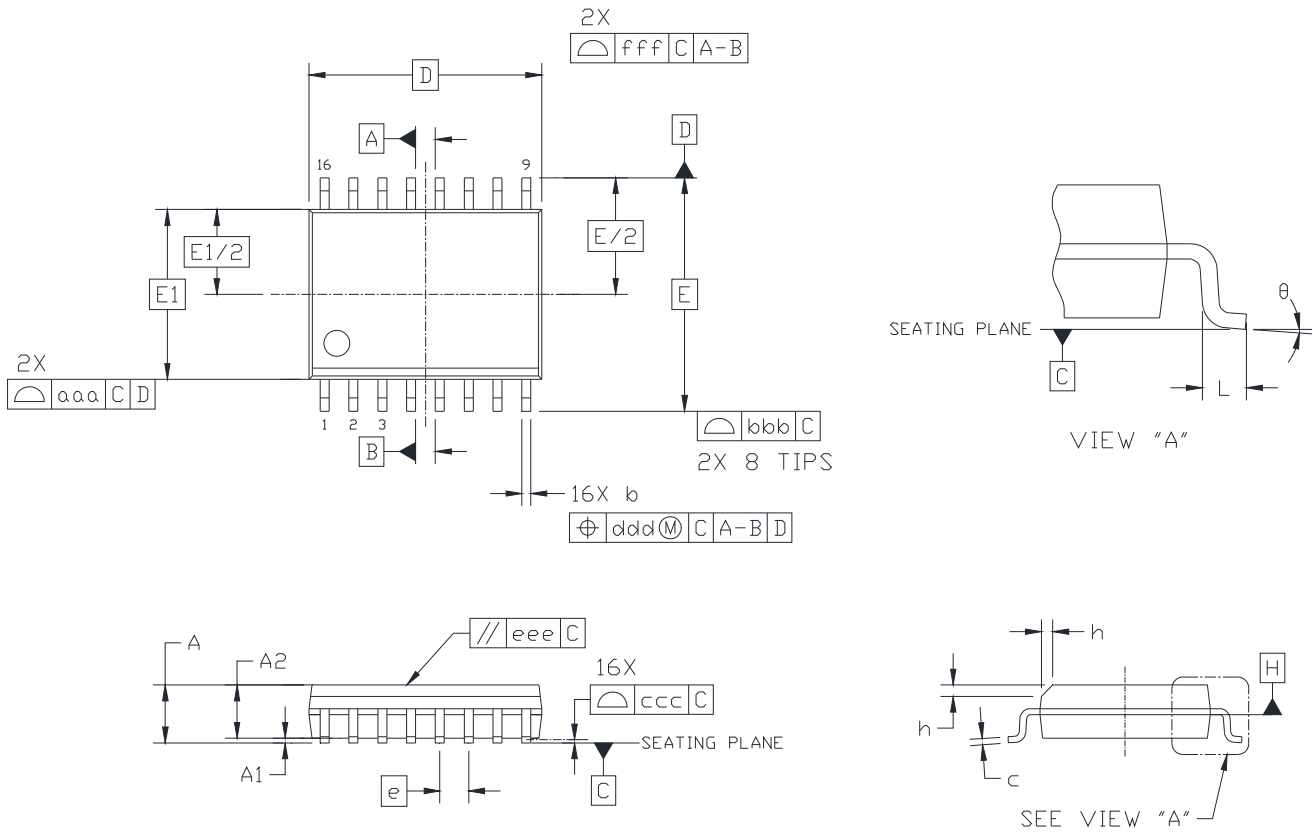
| Part Number (OPN) | Serial Port            | Package | Isolation Rating | Temp Range    |
|-------------------|------------------------|---------|------------------|---------------|
| Si8900B-A01-GS    | UART                   | WB SOIC | 2.5 kV           | -40 to +85 °C |
| Si8900D-A01-GS    | UART                   | WB SOIC | 5.0 kV           | -40 to +85 °C |
| Si8901B-A01-GS    | I <sup>2</sup> C/SMBus | WB SOIC | 2.5 kV           | -40 to +85 °C |
| Si8901D-A01-GS    | I <sup>2</sup> C/SMBus | WB SOIC | 5.0 kV           | -40 to +85 °C |
| Si8902B-A01-GS    | SPI Port               | WB SOIC | 2.5 kV           | -40 to +85 °C |
| Si8902D-A01-GS    | SPI Port               | WB SOIC | 5.0 kV           | -40 to +85 °C |

**Notes:**

1. Add an "R" suffix to the part number to specify the tape and reel option. Example: "Si8900AB-A-ISR".
2. All packages are RoHS-compliant.
3. Moisture sensitivity level is MSL3 for wide-body SOIC-16 package with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

## 9. Package Outline: 16-Pin Wide Body SOIC

Figure 19 illustrates the package details for the Si8900/1/2 Digital Isolator. Table 8 lists the values for the dimensions shown in the illustration.



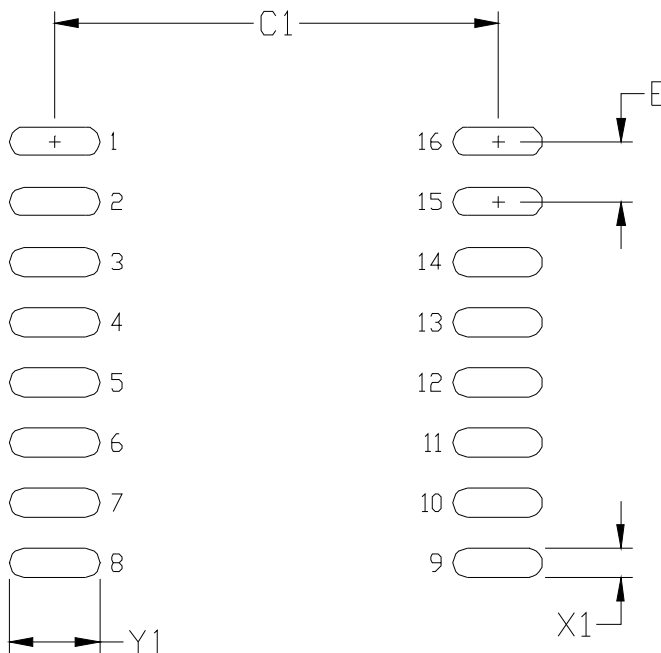
**Figure 19. 16-Pin Wide Body SOIC**

Table 8. Package Diagram Dimensions

| Symbol  | Millimeters |      |
|---|-------------|------|
|   | Min         | Max  |
| A   | —           | 2.65 |
| A1  | 0.10        | 0.30 |
| A2  | 2.05        | —    |
| b   | 0.31        | 0.51 |
| c   | 0.20        | 0.33 |
| D   | 10.30 BSC   |      |
| E   | 10.30 BSC   |      |
| E1  | 7.50 BSC    |      |
| e   | 1.27 BSC    |      |
| L   | 0.40        | 1.27 |
| h   | 0.25        | 0.75 |
| $\theta$  | 0°          | 8°   |
| aaa   | —           | 0.10 |
| bbb   | —           | 0.33 |
| ccc   | —           | 0.10 |
| ddd   | —           | 0.25 |
| eee   | —           | 0.10 |
| fff   | —           | 0.20 |
| <b>Notes:</b>   |             |      |
| <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li> <li>3. This drawing conforms to JEDEC Outline MS-013, Variation AA.</li> <li>4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.</li> </ol> |             |      |

## 10. Land Pattern: 16-Pin Wide-Body SOIC

Figure 20 illustrates the recommended land pattern details for the Si8900/1/2 in a 16-pin wide-body SOIC. Table 9 lists the values for the dimensions shown in the illustration.



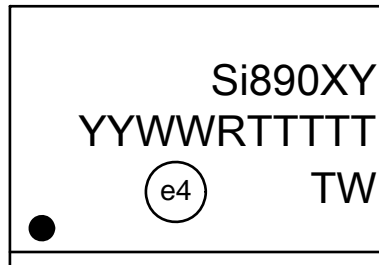
**Figure 20. 16-Pin SOIC Land Pattern**

**Table 9. 16-Pin Wide Body SOIC Land Pattern Dimensions**

| Dimension  | Feature            | (mm) |
|--|--------------------|------|
| C1   | Pad Column Spacing | 9.40 |
| E  | Pad Row Pitch      | 1.27 |
| X1   | Pad Width          | 0.60 |
| Y1   | Pad Length         | 1.90 |
| <b>Notes:</b>  |                    |      |
| <ol style="list-style-type: none"> <li>1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).</li> <li>2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.</li> </ol> |                    |      |

## 11. Top Marking: 16-Pin Wide Body SOIC

### 11.1. Si8900/1/2 Top Marking



### 11.2. Top Marking Explanation

|                        |  |  |
|------------------------|--|--|
| <b>Line 1 Marking:</b> | Base Part Number<br>Ordering Options<br><br>(See Ordering Guide for more information).     | Si890 = Isolator product series<br>X = Serial Port<br>0 = UART<br>1 = I <sup>2</sup> C<br>2 = SPI<br>Y = Insulation rating<br>B = 2.5 kV; D = 5.0 kV |
|                        | <b>Line 2 Marking:</b>   | YY = Year<br>WW = Workweek<br><br>RTTTTT = Mfg Code  |
| <b>Line 3 Marking:</b> | Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date. | Manufacturing code from assembly house<br>"R" indicates revision   |
|                        | Circle = 1.7 mm Diameter<br>(Center-Justified)   | "e4" Pb-Free Symbol  |
|                        | Country of Origin ISO Code<br>Abbreviation   | TW = Taiwan  |

## DOCUMENT CHANGE LIST

### Revision 0.5 to Revision 1.0

- No changes.

### Revision 1.0 to Revision 1.1

- Removed "pending" throughout.
- Changed AN638 reference to AN637.
- Updated "Top Marking: 16-Pin Wide Body SOIC" on page 29.

NOTES:

## CONTACT INFORMATION

### Silicon Laboratories Inc.

400 West Cesar Chavez  
Austin, TX 78701  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:  
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