# 5 kV LED Emulator Input, Open Collector Output Isolators

## Features

- Pin-compatible, drop-in upgrades for popular high-speed digital optocouplers
- Performance and reliability advantages vs. optocouplers
  - Resistant to temperature, age and forward current effects
  - 10x lower FIT rate for longer service life
  - Higher common-mode transient immunity: >50 kV/µs typical
  - Lower power and forward input diode current
- PCB footprint compatible with optocoupler packaging
- Wide range of product options
- 1 channel diode emulator input
- 3 to 30 V open collector output
- Propagation delay 30 ns
- Data rates dc to 15 Mbps
- 3.75 and 5 kV reinforced isolation
  - UL, CSA, VDE
- Wide operating temperature range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-8
  - DIP8
  - SDIP6
  - LGA8

## Applications

- Industrial automation
- Motor controls and drives
- Isolated switch mode power supplies
- Isolated data acquisition
- Test and measurement equipment

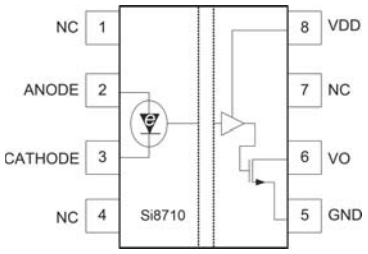
## Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE 0884 Part 2) (reinforced insulation)
- CQC certification approval
  - GB4943.1

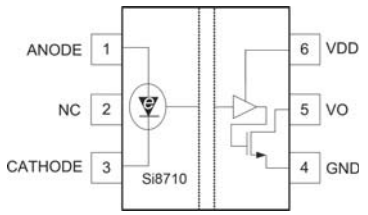
## Description

The Si87xx isolators are pin-compatible, one-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. These devices isolate high-speed digital signals and offer performance, reliability, and flexibility advantages not available with optocoupler solutions. The Si87xx series is based on Silicon Labs' proprietary CMOS isolation technology for low-power and high-speed operation and are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. As a result, the Si87xx series offer longer service life and dramatically higher reliability compared to optocouplers. Ordering options include open collector output with and without integrated pull-up resistor and output enable options.

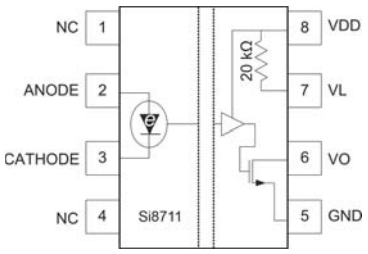
**Pin Assignments:**
**See page 18**



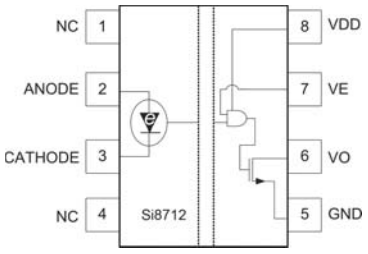

**SOIC-8, DIP8, LGA8**
**Open Collector Output**




**SDIP6**
**Open Collector Output**



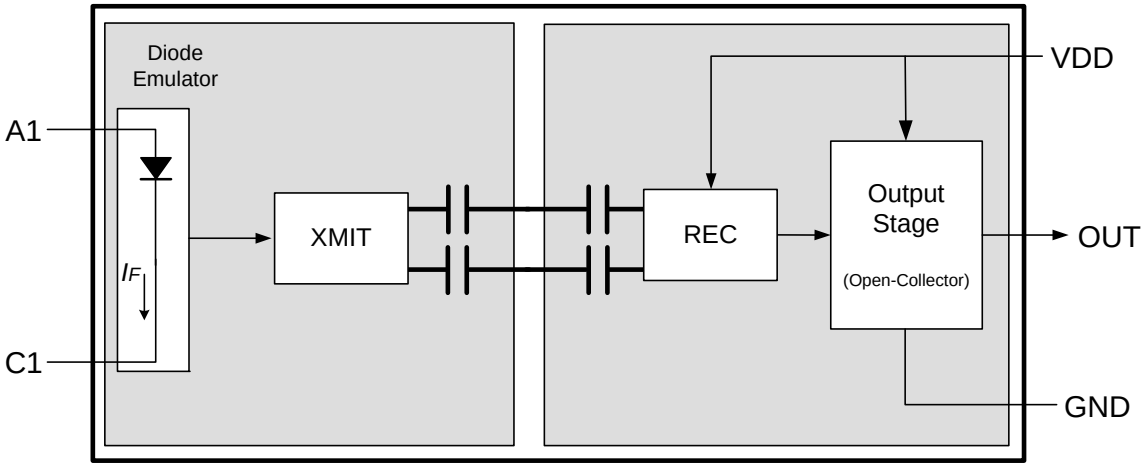

**SOIC-8, DIP8, LGA8**
**Open Collector Output**
**with 20 kΩ Pull-up Resistor**




**SOIC-8, DIP8, LGA8**
**Open Collector Output**
**with Output Enable**

Patent pending

## Functional Block Diagram



# TABLE OF CONTENTS

**Section** **Page**

**1. Electrical Specifications . . . . . 4**
**2. Application Information . . . . . 12**
2.1. Theory of Operation . . . . . 12
**3. Technical Description . . . . . 13**
3.1. Device Behavior . . . . . 13
3.2. Device Startup . . . . . 13
**4. Applications . . . . . 14**
4.1. Input Circuit Design . . . . . 14
4.2. Output Circuit Design and Power Supply Connections . . . . . 15
**5. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector . . . . . 16**
**6. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable . . . . . 17**
**7. Pin Descriptions (SDIP6) Open Collector . . . . . 18**
**8. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 kΩ Pull-Up Resistor . . . . . 19**
**9. Ordering Guide . . . . . 20**
**10. Package Outline: 8-Pin Narrow Body SOIC . . . . . 23**
**11. Land Pattern: 8-Pin Narrow Body SOIC . . . . . 24**
**12. Package Outline: DIP8 . . . . . 25**
**13. Land Pattern: DIP8 . . . . . 26**
**14. Package Outline: SDIP6 . . . . . 27**
**15. Land Pattern: SDIP6 . . . . . 29**
**16. Package Outline: LGA8 . . . . . 30**
**17. Land Pattern: LGA8 . . . . . 31**
**18. Top Marking: 8-Pin Narrow Body SOIC . . . . . 32**
**19. Top Marking: DIP8 . . . . . 33**
**20. Top Marking: SDIP6 . . . . . 34**
**21. Top Marking: LGA8 . . . . . 35**
**Contact Information . . . . . 36**

# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ Supply Voltage (Open Collector Output) | $V_{DD}$ | 3 | — | 30 | V |
| Input Current | $I_{F(ON)}$ | | | | |
| Si87xxA Devices | | 3 | — | 15 | mA |
| Si87xxB Devices | | 6 | — | 30 | mA |
| Si87xxC Devices | | 3 | — | 15 | mA |
| Operating Temperature (Ambient) | $T_A$ | –40 | — | 125 | °C |

### Table 2. Electrical Characteristics

$V_{DD}$ = 5 V; GND = 0 V; $T_A$ = –40 to +125 °C; typical specs at 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC Parameters** | | | | | | |
| Supply Voltage | $V_{DD}$ | Open collector output | 3 | — | 30 | V |
| Supply Current | $I_{DD}$ | Output high or low ($V_{DD}$ = 5 to 30 V) | — | — | 1.7 | mA |
| Input Current Threshold | $I_{F(TH)}$ | Si87xxA devices | 3 | — | — | mA |
| | | Si87xxB devices | 6 | — | — | mA |
| | | Si87xxC devices | 3 | — | — | mA |
| Input Current Rising Edge Hysteresis | $I_{HYS}$ | Si87xxA devices | — | 0.17 | — | mA |
| | | Si87xxB devices | — | 0.34 | — | mA |
| | | Si87xxC devices | — | 0.17 | — | mA |
| Input Forward Voltage (OFF) | $V_{F(OFF)}$ | Measured at ANODE with respect to CATHODE. | — | — | 1 | V |
| Input Forward Voltage (ON) | $V_{F(ON)}$ | Measured at ANODE with respect to CATHODE. | 1.7 | — | 2.8 | V |
| Input Reverse Breakdown Voltage | BVR | Ensures that reverse current is limited to a safe level. | –0.3 | — | — | V |
| Input Capacitance | $C_I$ | f = 100 kHz, | | | | |
| | | $V_F$ = 0 V, | — | 15 | — | pF |
| | | $V_F$ = 2 V | — | 15 | — | pF |
| Logic Low Output Voltage | $V_{OL}$ | $I_{OL}$ = 3 mA, $V_{DD}$ = 3.3 or 5 V | — | — | 0.4 | V |
| | | $I_{OL}$ = 13 mA, $V_{DD}$ = 5.5 V | — | — | 0.7 | V |
| Logic High Output Current | $I_{OH}$ | $V_{DD}$ = $V_{OUT}$ = 5.5 V | — | — | 0.5 | µA |
| | | $V_{DD}$ = $V_{OUT}$ = 24 V | — | — | 1 | µA |
| Peak Output Current | $I_{OPK}$ | Peak DC collector current drive ($V_{DD}$ = 5 V) | — | 50 | — | mA |
| Output Low Impedance | $R_{OL}$ | | — | — | 54 | Ω |
| Pull-up Resistor | $R_{PU}$ | Using internal pull-up | — | 20 | — | kΩ |
| Enable High Min | $V_{EH}$ | | 2 | — | 30 | V |
| Enable Low Max | $V_{EL}$ | | — | — | 0.8 | V |
| Enable High Current Draw | $I_{EH}$ | $V_{DD}$ = $V_{EH}$ = 5 V | — | 20 | — | µA |
| Enable Low Current Draw | $I_{EL}$ | $V_{DD}$ = 5 V, $V_{EL}$ = 0 V | — | –10 | 0 | µA |

**Table 2. Electrical Characteristics (Continued)**

$V_{DD}$ = 5 V; GND = 0 V; $T_A$ = –40 to +125 °C; typical specs at 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **AC Switching Parameters ($V_{DD}$ = 5 V, $R_L$ = 350 Ω, $C_L$ = 15 pF)** | | | | | | |
| Maximum Data Rate | $F_{DATA}$ | Si87xxA devices<br>Si87xxB devices<br>Si87xxC devices | DC<br>DC<br>DC | —<br>—<br>— | 15<br>15<br>1 | $M_{BPS}$<br>$M_{BPS}$<br>$M_{BPS}$ |
| Minimum Pulse Width | MPW | Si87xxA devices<br>Si87xxB devices<br>Si87xxC devices | 66<br>66<br>1 | —<br>—<br>— | —<br>—<br>— | ns<br>ns<br>µs |
| Propagation Delay (Low-to-High) | $t_{PLH}$ | $C_L$ = 15 pF using 350 Ω pull-up | — | — | 60 | ns |
| Propagation Delay (High-to-Low) | $t_{PHL}$ | $C_L$ = 15 pF using 350 Ω pull-up | — | — | 60 | ns |
| Pulse Width Distortion | PWD | $\lvert t_{PLH} - t_{PHL} \rvert$ | — | — | 20 | ns |
| Propagation Delay Skew | $t_{PSK(p-p)}$ | $t_{PSK(P-P)}$ is the magnitude of the difference in prop delays between different units operating at same supply voltage, load, and ambient temp. | — | — | 20 | ns |
| Rise Time | $t_R$ | $C_L$ = 15 pF using 350 Ω pull-up | — | 15 | — | ns |
| Fall Time | $t_F$ | $C_L$ = 15 pF using 350 Ω pull-up | — | 5 | — | ns |
| Device Startup Time | $t_{START}$ | | — | — | 40 | µs |
| Common Mode Transient Immunity | CMTI | Output = low or high<br>$I_F$ = 3 mA for Si87xxA devices<br>$I_F$ = 6 mA for Si87xxB devices<br>$I_F$ = 3 mA for Si87xxC devices | <br>20<br>35<br>20 | <br>35<br>50<br>35 | <br>—<br>—<br>— | <br>kV/µs<br>kV/µs<br>kV/µs |

**Table 3. Regulatory Information (Pending)***

| |
|---|
| **CSA** |
| The Si87xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873. |
| 61010-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 600 $V_{RMS}$ basic insulation working voltage. |
| 60950-1: Up to 1000 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| 60601-1: Up to 250 $V_{RMS}$ reinforced insulation working voltage; up to 500 $V_{RMS}$ basic insulation working voltage. |
| **VDE** |
| The Si87xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001. |
| 60747-5-2: Up to 1414 $V_{peak}$ for reinforced insulation working voltage. |
| **UL** |
| The Si87xx is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 $V_{RMS}$ isolation voltage for basic protection. |
| **CQC** |
| The Si87xx is certified under GB4943.1-2011. For more details, see File number pending. |
| Rated up to 1000 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| ***Note:** Regulatory Certifications apply to 3.75 $kV_{RMS}$ rated devices which are production tested to 4.5 $kV_{RMS}$ for 1 sec. Regulatory Certifications apply to 5.0 $kV_{RMS}$ rated devices which are production tested to 6.0 $kV_{RMS}$ for 1 sec. For more information, see "9.Ordering Guide" on page 20. |

**Table 4. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Nominal Air Gap (Clearance) | L(IO1) | | 4.9 min | 7.4 min | 8.0 min | 9.6 min | mm |
| Nominal External Tracking (Creepage) | L(IO2) | | 4.8 min | 8.0 min | 8.0 min | 10.0 min | mm |
| Minimum Internal Gap (Internal Clearance) | | | 0.016 | 0.016 | 0.016 | 0.016 | mm |
| Tracking Resistance (Proof Tracking Index) | PTI | IEC60112 | 600 | 600 | 600 | 600 | V |
| Erosion Depth | ED | | 0.031 | 0.031 | Pending | 0.021 | mm |
| Resistance (Input-Output)* | $R_{IO}$ | | $10^{12}$ | $10^{12}$ | $10^{12}$ | $10^{12}$ | Ω |
| Capacitance (Input-Output)* | $C_{IO}$ | f = 1 MHz | 1 | 1 | 1 | 1 | pF |

***Note:** To determine resistance and capacitance, the Si87xx is converted into a 2-terminal device. Pins 1–4 (1–3, SDIP6) are shorted together to form the first terminal, and pins 5–8 (4–6, SDIP6) are shorted together to form the second terminal. The parameters are then measured between these two terminals.

**Table 5. IEC 60664-1 (VDE 0844 Part 2) Ratings**

| Parameter | Test Condition | Specification | | | |
|---|---|---|---|---|---|
| | | SOIC-8 | DIP8 | SDIP6 | LGA8 |
| Basic Isolation Group | Material Group | I | I | I | I |
| Installation Classification | Rated Mains Voltages ≤ 150 $V_{RMS}$ | I-IV | I-IV | I-IV | I-IV |
| | Rated Mains Voltages ≤ 300 $V_{RMS}$ | I-IV | I-IV | I-IV | I-IV |
| | Rated Mains Voltages ≤ 450 $V_{RMS}$ | I-III | I-III | I-IV | I-IV |
| | Rated Mains Voltages ≤ 600 $V_{RMS}$ | I-III | I-III | I-IV | I-IV |
| | Rated Mains Voltages ≤ 1000 $V_{RMS}$ | — | — | — | I-III |

**Table 6. IEC 60747-5-2 Insulation Characteristics***

| Parameter | Symbol | Test Condition | Characteristic | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | | 630 | 891 | 1140 | 1414 | V peak |
| Input to Output Test Voltage | $V_{PR}$ | Method b1 ($V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test, $t_m$ = 1 sec, Partial Discharge < 5 pC) | 1181 | 1671 | 2138 | 2652 | V peak |
| Transient Overvoltage | $V_{IOTM}$ | t = 60 sec | 6000 | 6000 | 8000 | 8000 | V peak |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | 2 | 2 | 2 | |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | | $>10^9$ | $>10^9$ | $>10^9$ | $>10^9$ | Ω |

***Note:** This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si87xx provides a climate classification of 40/125/21.

**Table 7. IEC Safety Limiting Values**

| Parameter | Symbol | Test Condition | Max | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Case Temperature | $T_S$ | | 140 | 140 | 140 | 140 | °C |
| Input Current | $I_S$ | $\theta_{JA}$ = 110 °C/W (SOIC-8), 110 °C/W (DIP8), 105 °C/W (SDIP6), 220 °C (LGA8), $V_F$ = 2.8 V, $T_J$ = 140 °C, $T_A$ = 25 °C | 370 | 370 | 390 | 185 | mA |
| Output Power | $P_S$ | | 1 | 1 | 1 | 0.5 | W |
| **Note:** Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 1, 2, 3, and 4. | | | | | | | |

**Table 8. Thermal Characteristics**

| Parameter | Symbol | Typ | | | | Unit |
|---|---|---|---|---|---|---|
| | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 110 | 110 | 105 | 220 | ºC/W |

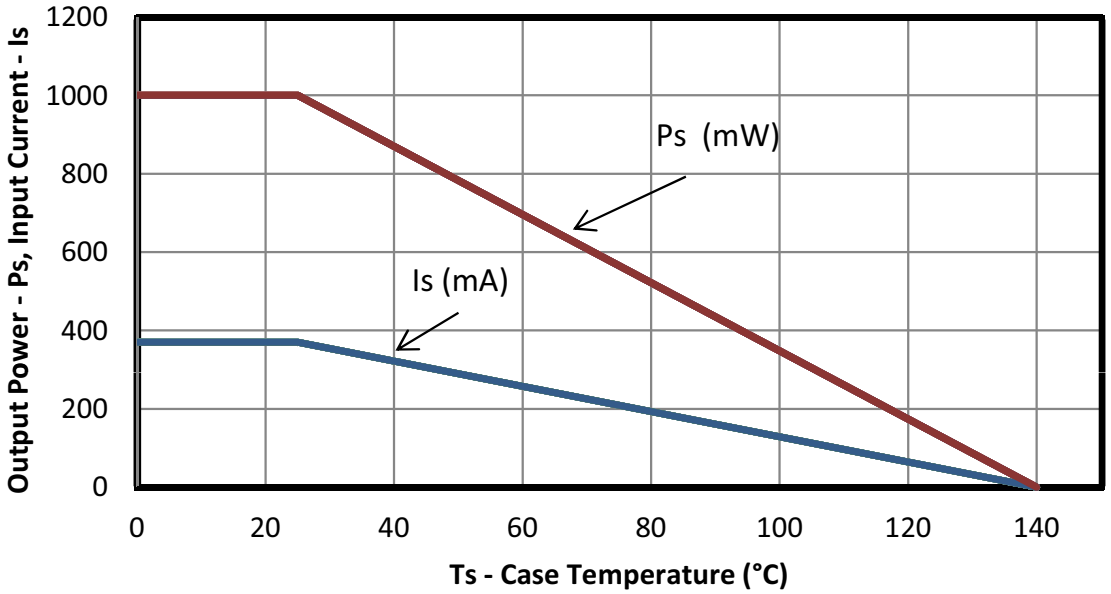



**Figure 1. (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

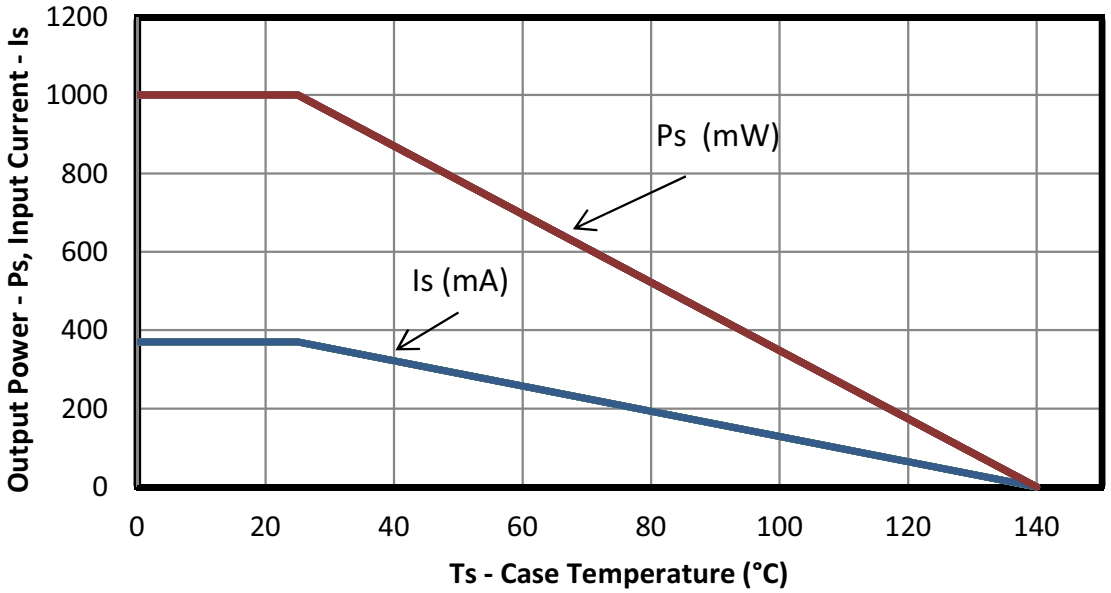



**Figure 2. (DIP8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

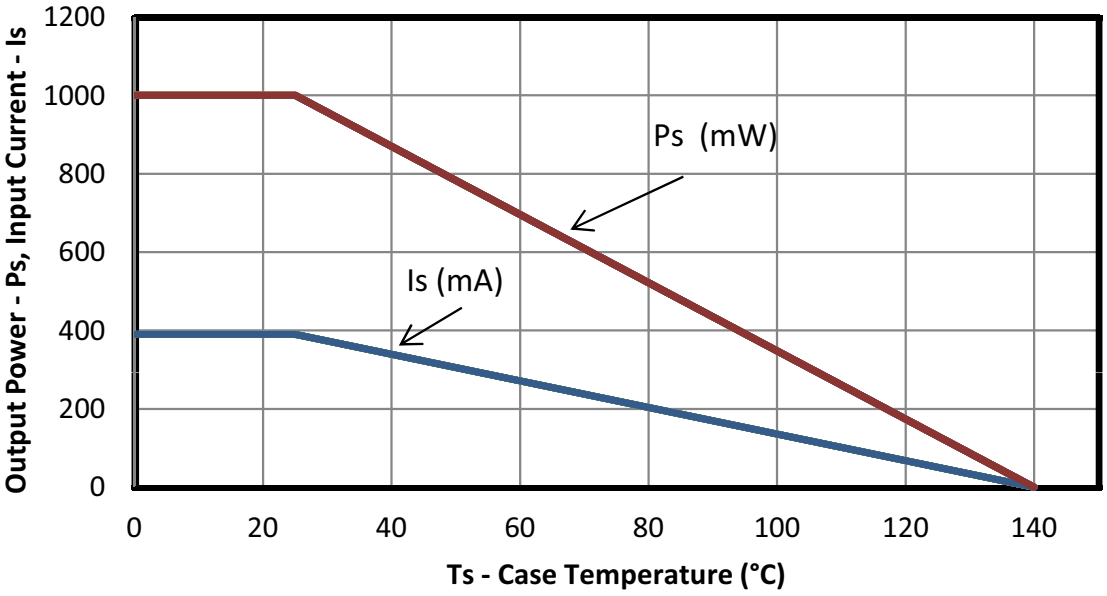



**Figure 3. (SDIP6) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

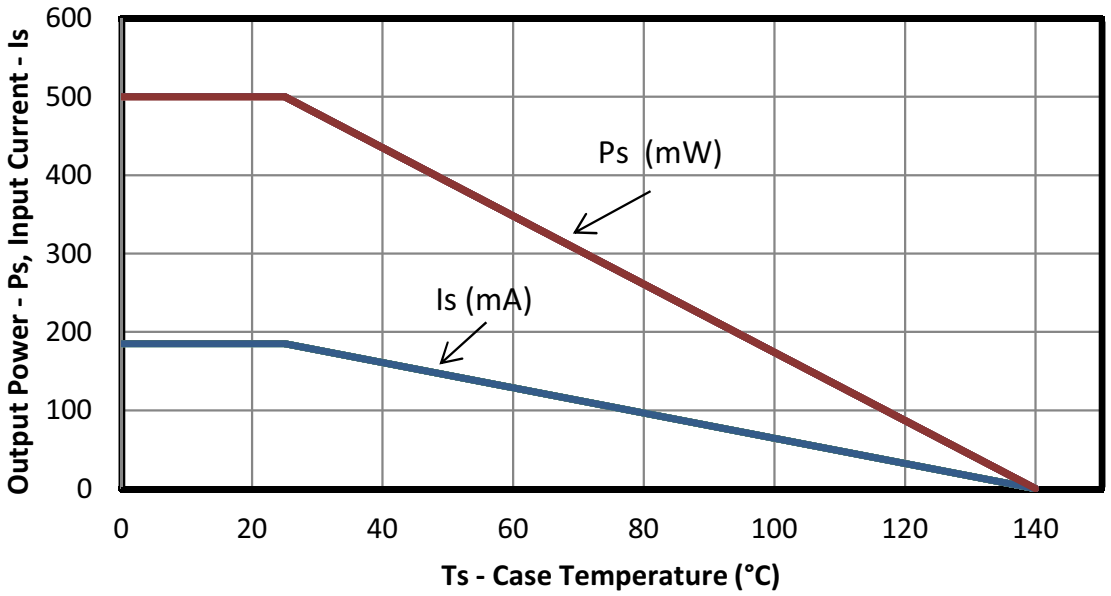



**Figure 4. (LGA8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2**

**Table 9. Absolute Maximum Ratings***

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_{STG}$ | –65 | +150 | °C |
| Operating Temperature | $T_A$ | –40 | +125 | °C |
| Junction Temperature | $T_J$ | — | +140 | °C |
| Average Forward Input Current<br>Si87xxA Devices<br>Si87xxB Devices<br>Si87xxC Devices | $I_{F(AVG)}$ | <br>—<br>—<br>— | <br>15<br>30<br>15 | <br>mA<br>mA<br>mA |
| Peak Transient Input Current<br>(< 1 µs pulse width, 300 ps) | $I_{FTR}$ | — | 1 | A |
| Reverse Input Voltage | $V_R$ | –0.3 | | V |
| Supply Voltage | $V_{DD}$ | –0.5 | 36 | V |
| Output Voltage | $V_{OUT}$ | –0.5 | 36 | V |
| Enable Voltage | $V_{OUT}$ | –0.5 | $V_{DD}$+0.5 | V |
| Output Sink Current | $I_{SINK}$ | — | 15 | mA |
| Average Output Current | $I_{O(AVG)}$ | — | 8 | mA |
| Peak Output Current ($V_{DD}$ = 5 V) | $I_{OPK}$ | — | 75 | mA |
| Input Power Dissipation | $P_I$ | — | 90 | mW |
| Output Power Dissipation | $P_O$ | — | 50 | mW |
| Total Power Dissipation | $P_T$ | — | 140 | mW |
| Lead Solder Temperature (10 s) | | — | 260 | °C |
| HBM Rating ESD | | 3 | — | kV |
| Machine Model ESD | | 200 | — | V |
| CDM | | 500 | — | V |
| Maximum Isolation Voltage (1 s) SOIC-8 | | — | 4500 | $V_{RMS}$ |
| Maximum Isolation Voltage (1 s) DIP8 | | — | 4500 | $V_{RMS}$ |
| Maximum Isolation Voltage (1 s) SDIP6 | | — | 6500 | $V_{RMS}$ |
| Maximum Isolation Voltage (1 s) LGA8 | | — | 6500 | $V_{RMS}$ |

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

# 2. Application Information

## 2.1. Theory of Operation

The Si87xx are pin-compatible, one-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. The operation of an Si87xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si87xx is shown in Figure 5.

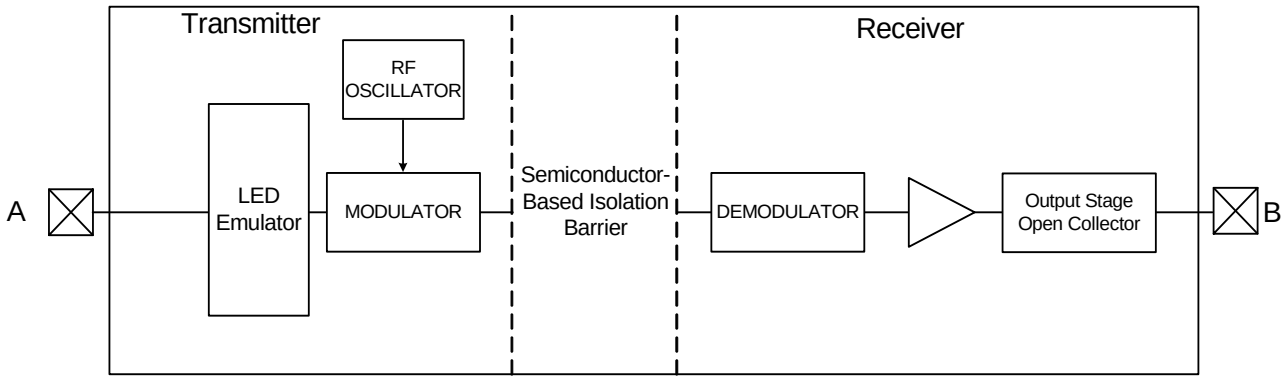



**Figure 5. Simplified Channel Diagram**

# 3. Technical Description

## 3.1. Device Behavior

Truth tables for the Si87xx are summarized in Table 10.

**Table 10. Si87xx Truth Table Summary[1]**

| Input | $V_{DD}$ | EN[2] | $V_O$[3] |
|---|---|---|---|
| OFF | > UVLO | H | HIGH |
| OFF | > UVLO | L | HIGH |
| OFF | < UVLO | H | HIGH |
| OFF | < UVLO | L | HIGH |
| ON | > UVLO | H | LOW |
| ON | > UVLO | L | HIGH |
| ON | < UVLO | H | HIGH |
| ON | < UVLO | L | HIGH |

**Notes:**
1. This truth table assumes $V_{DD}$ is powered. UVLO is typically 2.8 V.
2. Si8712 only.
3. The output voltage level is determined by the external pull-up supply.

## 3.2. Device Startup

Output $V_O$ is held low during power-up until $V_{DD}$ rises above the UVLO+ threshold for a minimum time period of $t_{START}$. Following this, the output is high when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shutdown behavior is shown in Figure 6.

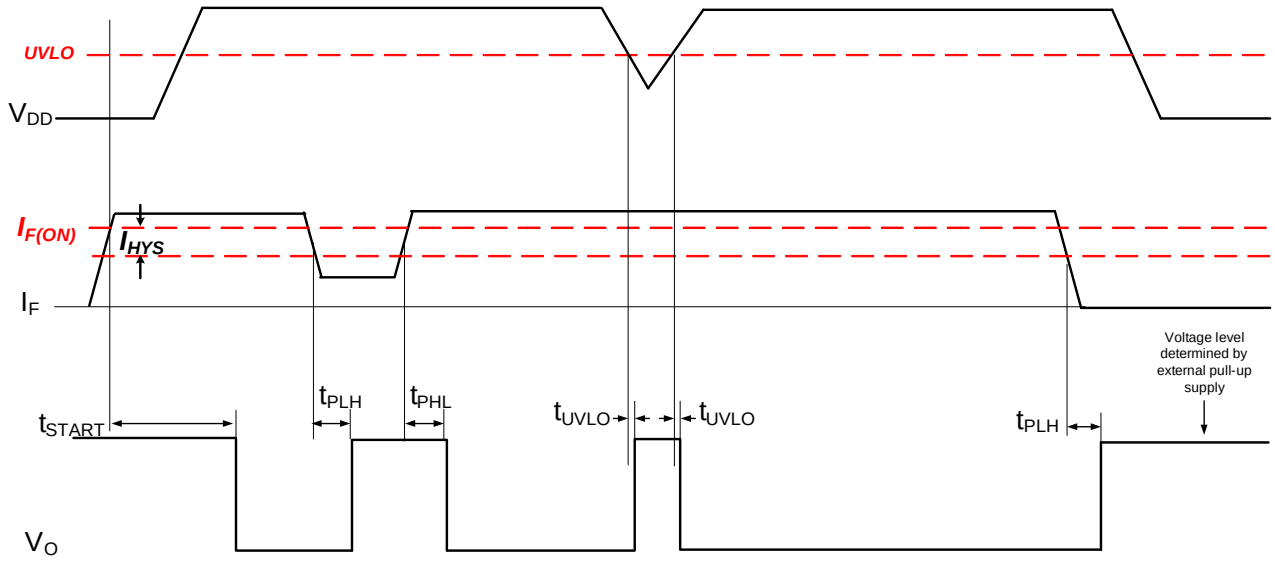



**Figure 6. Si87xx Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)**

# 4. Applications

The following sections detail the input and output circuits necessary for proper operation of the Si87xx family.

## 4.1. Input Circuit Design

Opto coupler manufacturers typically recommend the circuits shown in Figures 7 and 8. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

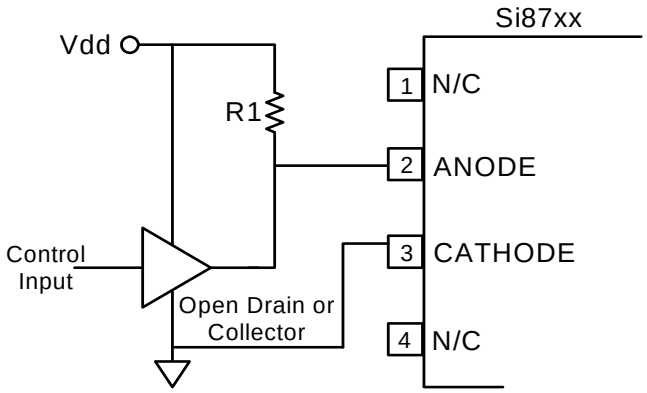



**Figure 7. Si87xx Input Circuit**

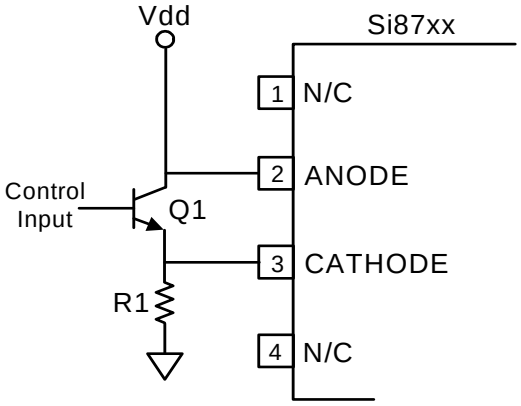



**Figure 8. High CMR Si87xx Input Circuit**

The optically-coupled circuit of Figure 7 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 8 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity.

Some opto coupler applications recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED. The Si87xx input circuit requires less current and has twice the off-state noise margin compared to opto couplers. However, high CMR opto coupler designs that overdrive the LED (see Figure 8) may require increasing the value of R1 to limit input current $I_F$ to its maximum rating when using the Si87xx. In addition, there is no benefit in driving the Si87xx input diode into reverse bias when in the off state. Consequently, opto coupler circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g., add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si87xx is no more than –0.3 V with respect to the cathode when reverse-biased.

New designs should consider the input circuit configurations of Figure 9, which are more efficient than those of Figures 7 and 8. As shown, S1 and S2 represent any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si87xx input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 6 mA (see Figure 9B). Additionally, note that the Si87xx propagation delay and output drive do not significantly change for values of $I_F$ between $I_{F(MIN)}$ and $I_{F(MAX)}$.

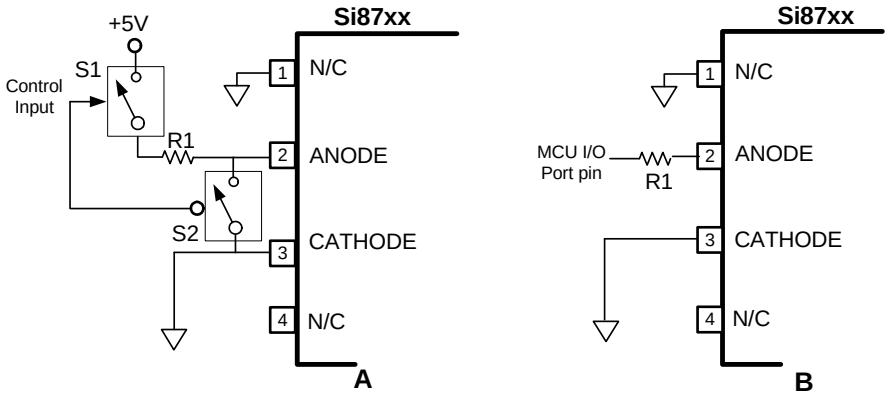



**Figure 9. Si87xx Other Input Circuit Configurations**

## 4.2. Output Circuit Design and Power Supply Connections

The speed of the open collector circuit is dependent upon the supply, VCC, the pullup resistor, $R_L$, and the load modeled by $C_L$. Figure 10 illustrates three common circuit output configurations. For $V_{DD}$ = 5 V operation, $R_L$>350 Ω is recommended to ensure proper $V_{OL}$ levels. For $V_{DD}$ = 30 V operation, $R_L$ > 2.1 kΩ is recommended to ensure proper $V_{OL}$ levels. If the enable pin is used (see Figure 10B) and two separate supplies power $V_{DD}$ and the $V_O$ pullup resistor, the enable pin should be referenced to the $V_{DD}$ pin because $V_O$ cannot exceed $V_{DD}$ by more than 0.5 V. Figure 10C illustrates a circuit using the internal 20 kΩ resistor.

Note that GND can be biased at, above, or below ground as long as the voltage on $V_{DD}$ with respect to GND is a maximum of 30 V. $V_{DD}$ decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 1 µF bypass capacitors be used to reduce high-frequency noise and maximize performance. Opto replacement applications should limit their supply voltages to 30 V or less.

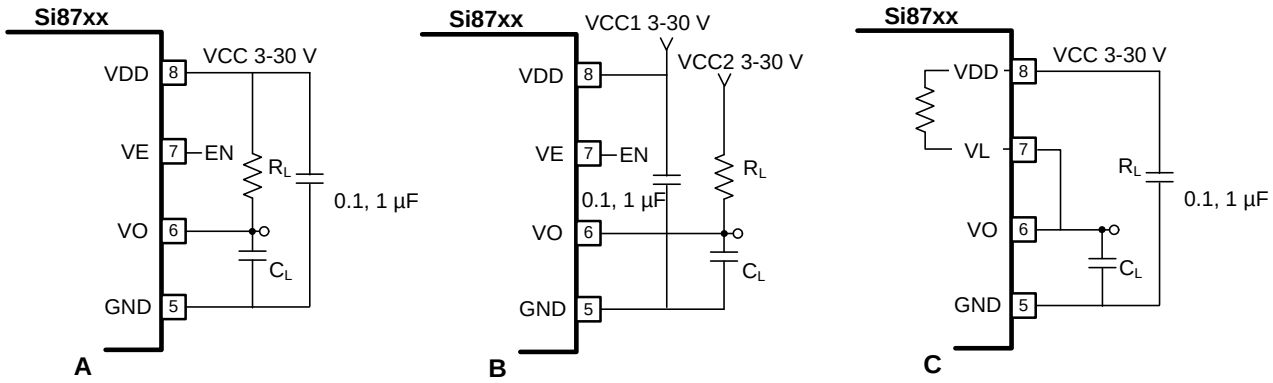



**Figure 10. Si87xx Output Circuit Configurations**

## 5. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector

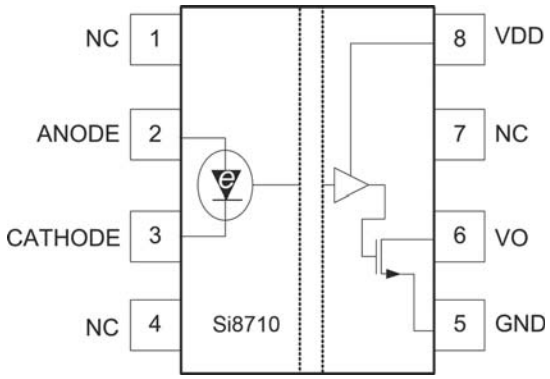



**Figure 11. Pin Configuration**

**Table 11. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector**

| Pin | Name | Description |
|---|---|---|
| 1 | NC | No connect. |
| 2 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 4 | NC | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | $V_O$ | Output signal. |
| 7 | NC | No connect. |
| 8 | $V_{DD}$ | Output-side power supply input referenced to GND (30 V max). |
| ***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane. | | |

## 6. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable

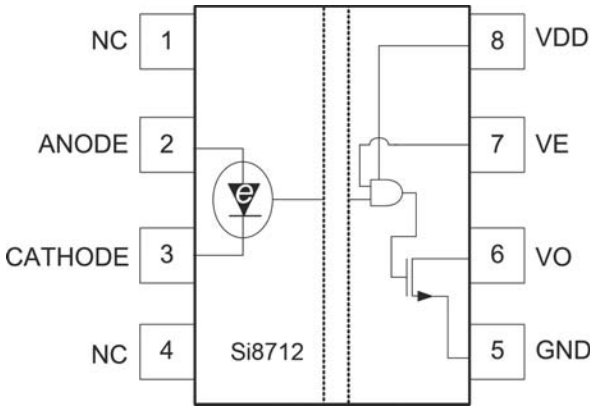



**Figure 12. Pin Configuration**

**Table 12. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable**

| Pin | Name | Description |
|---|---|---|
| 1 | NC | No connect. |
| 2 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 4 | NC | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | $V_O$ | Output signal. |
| 7 | $V_E$ | Output enable. |
| 8 | $V_{DD}$ | Output-side power supply input referenced to GND (30 V max). |
| ***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane. | | |

## 7. Pin Descriptions (SDIP6) Open Collector

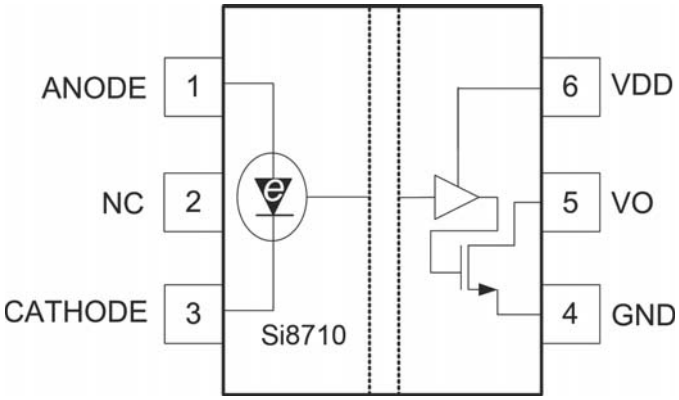



**Figure 13. Pin Configuration**

**Table 13. Pin Descriptions (SDIP6) Open Collector**

| Pin | Name | Description |
|---|---|---|
| 1 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 2 | NC | No connect. |
| 3 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 4 | GND | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 5 | $V_O$ | Output signal. |
| 6 | $V_{DD}$ | Output-side power supply input referenced to GND (30 V max). |
| ***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane. | | |

## 8. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 kΩ Pull-Up Resistor

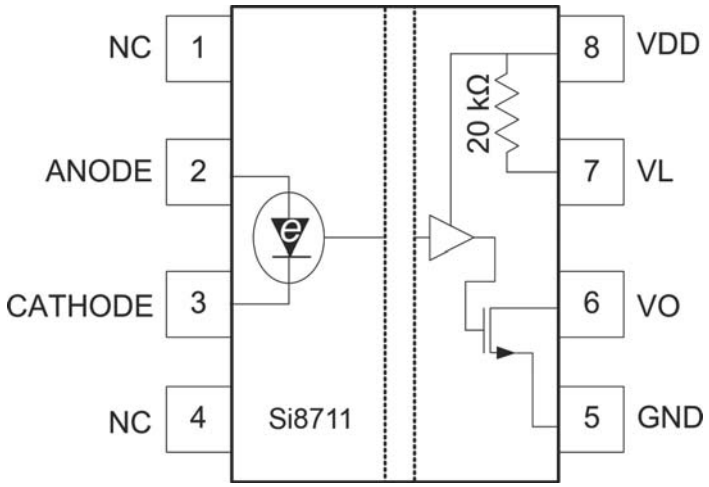



**Figure 14. Pin Configuration**

**Table 14. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 kΩ Pull-Up Resistor**

| Pin | Name | Description |
|---|---|---|
| 1 | NC | No connect. |
| 2 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 4 | NC | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | $V_O$ | Output signal. |
| 7 | $V_L$ | Output Pull-Up Load |
| 8 | $V_{DD}$ | Output-side power supply input referenced to GND (30 V max). |
| ***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane. | | |

## 9. Ordering Guide

**Table 15. Si87xx Ordering Guide***

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|---|---|---|---|---|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| **Open Collector Output (Available in SOIC-8, DIP8, and SDIP6)** | | | | | |
| Si8710AC-B-IS (In Production) | LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8710BC-B-IS (In Production) | High CMTI LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8710CC-B-IS (In Production) | LED input Open collector output | 1 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8710AC-B-IP (In Production) | LED input Open collector output | 15 Mbps HCPL-4502 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8710BC-B-IP (In Production) | High CMTI LED input Open collector output | 15 Mbps HCPL-4502 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8710CC-B-IP (In Production) | LED input Open collector output | 1 Mbps HCPL-4502 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8710AD-B-IS (Sampling) | LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | –40 to +125 °C | SDIP6 |
| Si8710BD-B-IS (Sampling) | High CMTI LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | –40 to +125 °C | SDIP6 |
| Si8710CD-B-IS (Sampling) | LED input Open collector output | 1 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | –40 to +125 °C | SDIP6 |

***Note:** All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

**Table 15. Si87xx Ordering Guide* (Continued)**

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|---|---|---|---|---|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| **Open Collector Output with 20 kΩ Pullup Resistor (Available in SOIC-8, DIP8, and LGA8)** | | | | | |
| Si8711AC-B-IS (In Production) | LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8711BC-B-IS (In Production) | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8711CC-B-IS (In Production) | LED input Open collector output with integrated pullup | 1 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8711AC-B-IP (In Production) | LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8711BC-B-IP (In Production) | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8711CC-B-IP (In Production) | LED input Open collector output with integrated pullup | 1 Mbps HCPL-4506 | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8711AD-B-IM (Sampling) | LED input Open collector output with integrated pullup | 15 Mbps HCNW-4506 | 5.0 kVrms | –40 to +125 °C | LGA8 |
| Si8711BD-B-IM (Sampling) | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCNW-4506 | 5.0 kVrms | –40 to +125 °C | LGA8 |
| Si8711CD-B-IM (Sampling) | LED input Open collector output with integrated pullup | 1 Mbps HCNW-4506 | 5.0 kVrms | –40 to +125 °C | LGA8 |

***Note:** All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

**Table 15. Si87xx Ordering Guide* (Continued)**

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|---|---|---|---|---|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| **Open Collector Output with Output Enable (Available in SOIC-8, DIP8, and LGA8)** | | | | | |
| Si8712AC-B-IS (In Production) | LED input Open collector output with enable | 15 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8712BC-B-IS (In Production) | High CMTI LED input Open collector output with enable | 15 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8712CC-B-IS (In Production) | LED input Open collector output with enable | 1 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8712AC-B-IP (In Production) | LED input Open collector output with enable | 15 Mbps HCPL-261x/260x | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8712BC-B-IP (In Production) | High CMTI LED input Open collector output with enable | 15 Mbps HCPL-261x/260x | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8712CC-B-IP (In Production) | LED input Open collector output with enable | 1 Mbps HCPL-261x/260x | 3.75 kVrms | –40 to +125 °C | DIP8/GW |
| Si8712AD-B-IM (Sampling) | LED input Open collector output with enable | 15 Mbps HCNW-2611 | 5.0 kVrms | –40 to +125 °C | LGA8 |
| Si8712BD-B-IM (Sampling) | High CMTI LED input Open collector output with enable | 15 Mbps HCNW-2611 | 5.0 kVrms | –40 to +125 °C | LGA8 |
| Si8712CD-B-IM (Sampling) | LED input Open collector output with enable | 1 Mbps HCNW-2611 | 5.0 kVrms | –40 to +125 °C | LGA8 |

***Note:** All packages are RoHS-compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

## 10. Package Outline: 8-Pin Narrow Body SOIC

Figure 15 illustrates the package details for the Si87xx in an 8-pin narrow-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

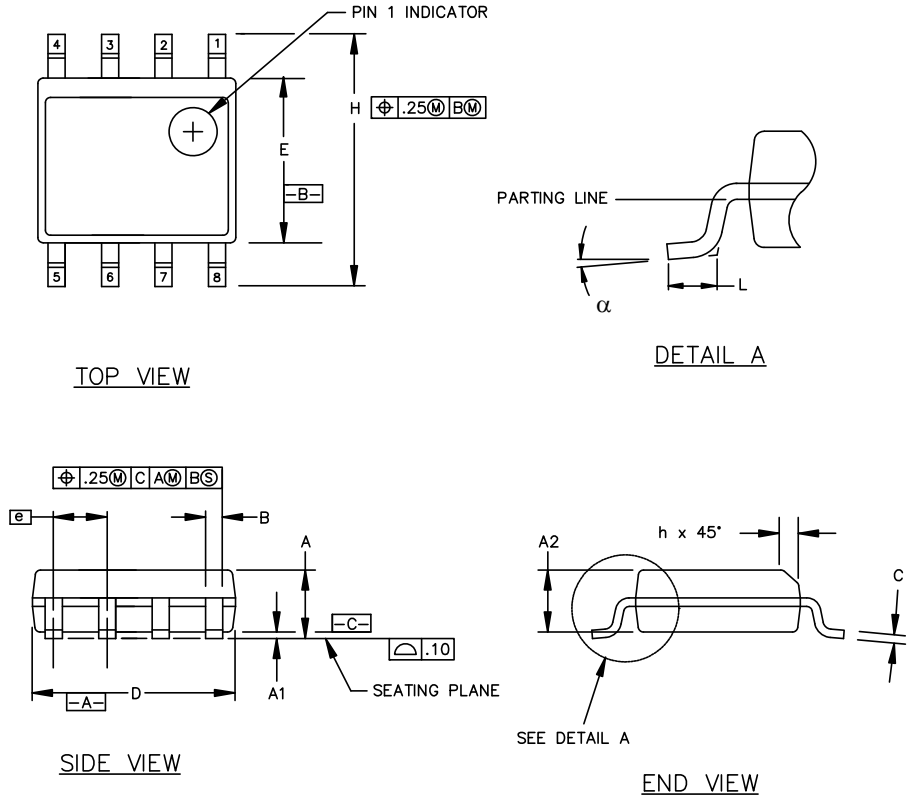



**Figure 15. 8-Pin Narrow Body SOIC Package**

**Table 16. 8-Pin Narrow Body SOIC Package Diagram Dimensions**

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| ∝ | 0° | 8° |

## 11. Land Pattern: 8-Pin Narrow Body SOIC

Figure 16 illustrates the recommended land pattern details for the Si87xx in an 8-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

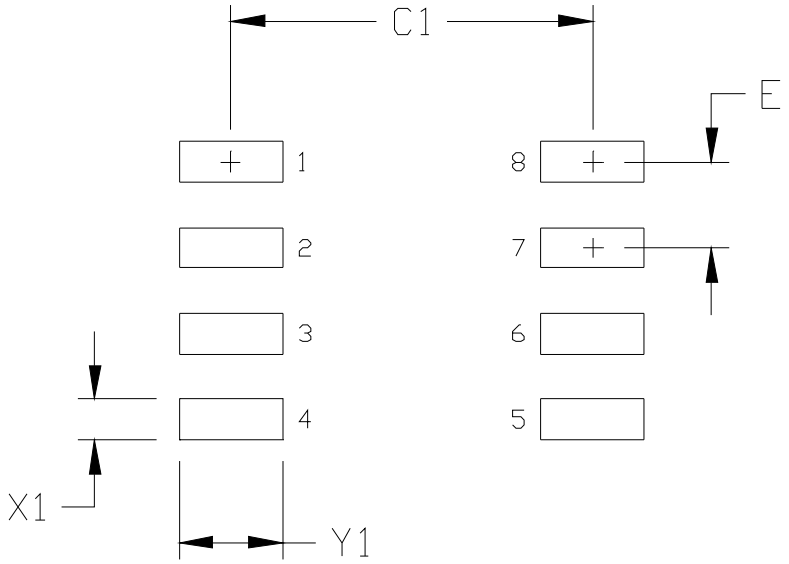



**Figure 16. 8-Pin Narrow Body SOIC Land Pattern**

**Table 17. 8-Pin Narrow Body SOIC Land Pattern Dimensions**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 5.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.55 |

**Notes:**
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 12. Package Outline: DIP8

Figure 17 illustrates the package details for the Si87xx in a DIP8 package. Table 18 lists the values for the dimensions shown in the illustration.

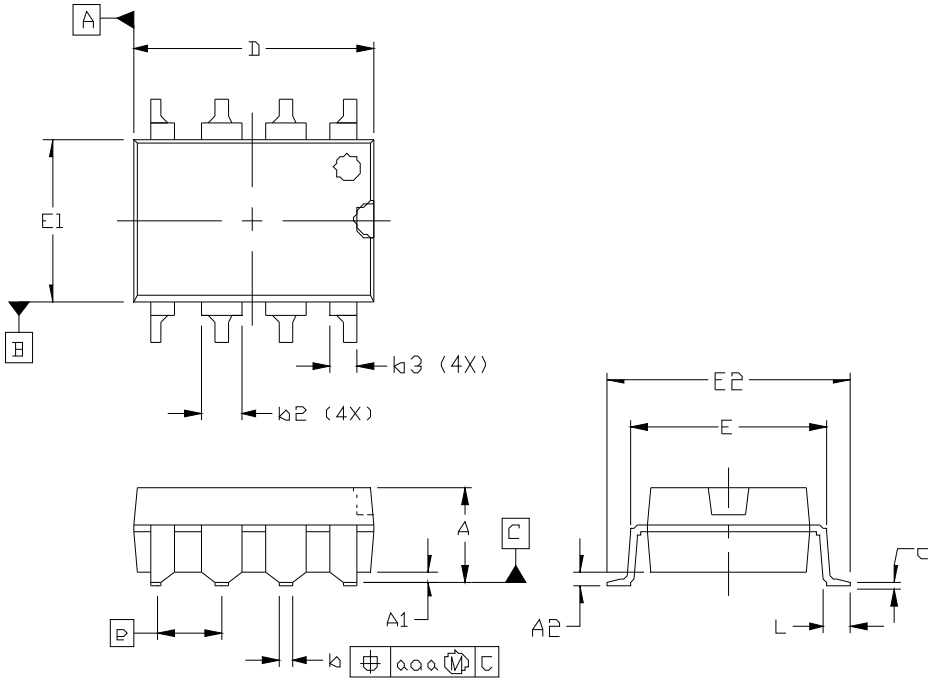



**Figure 17. DIP8 Package**

**Table 18. DIP8 Package Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| A | — | 4.19 |
| A1 | 0.55 | 0.75 |
| A2 | 3.17 | 3.43 |
| b | 0.35 | 0.55 |
| b2 | 1.14 | 1.78 |
| b3 | 0.76 | 1.14 |
| c | 0.20 | 0.33 |
| D | 9.40 | 9.90 |
| E | 7.37 | 7.87 |
| E1 | 6.10 | 6.60 |
| E2 | 9.40 | 9.90 |
| e | 2.54 BSC. | |
| L | 0.38 | 0.89 |
| aaa | — | 0.25 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 13. Land Pattern: DIP8

Figure 18 illustrates the recommended land pattern details for the Si87xx in a DIP8 package. Table 19 lists the values for the dimensions shown in the illustration.

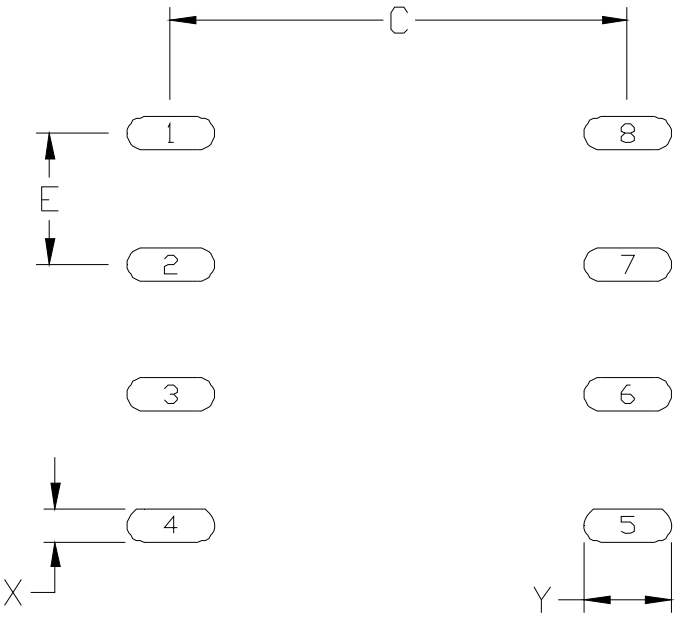



**Figure 18. DIP8 Land Pattern**

**Table 19. DIP8 Land Pattern Dimensions***

| Dimension | Min | Max |
|---|---|---|
| C | 8.85 | 8.90 |
| E | 2.54 BSC | |
| X | 0.60 | 0.65 |
| Y | 1.65 | 1.70 |
| ***Note:** This Land Pattern Design is based on the IPC-7351 specification. | | |

## 14. Package Outline: SDIP6

Figure 19 illustrates the package details for the Si87xx in an SDIP6 package. Table 20 lists the values for the dimensions shown in the illustration.

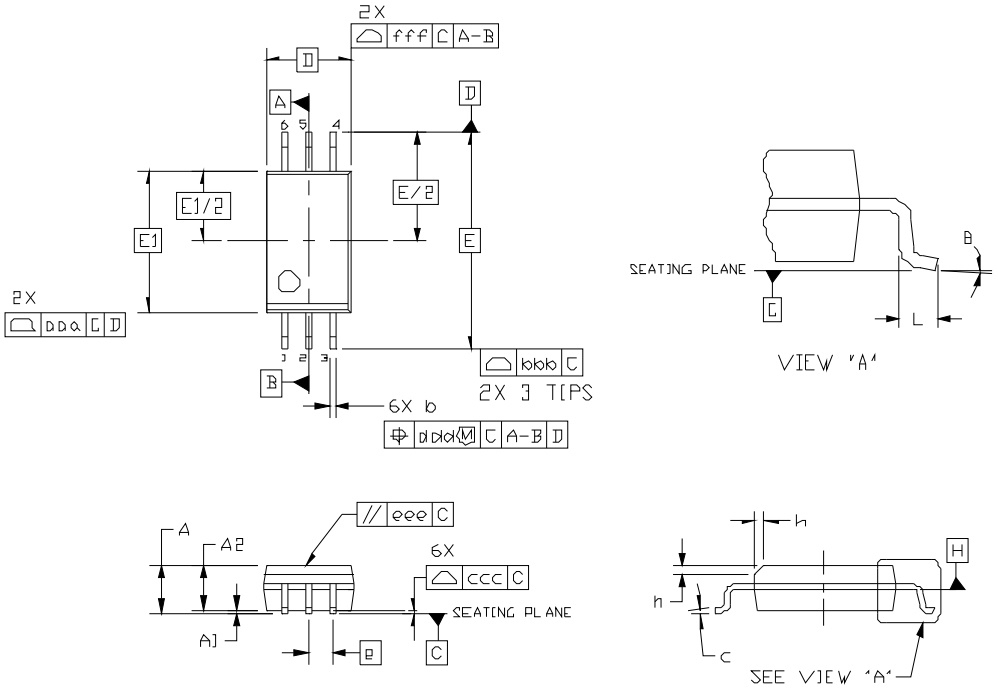



**Figure 19. SDIP6 Package**

**Table 20. SDIP6 Package Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 4.58 BSC | |
| E | 11.50 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

**Table 20. SDIP6 Package Diagram Dimensions (Continued)**

| Dimension | Min | Max |
|---|---|---|
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 15. Land Pattern: SDIP6

Figure 20 illustrates the recommended land pattern details for the Si87xx in an SDIP6 package. Table 21 lists the values for the dimensions shown in the illustration.

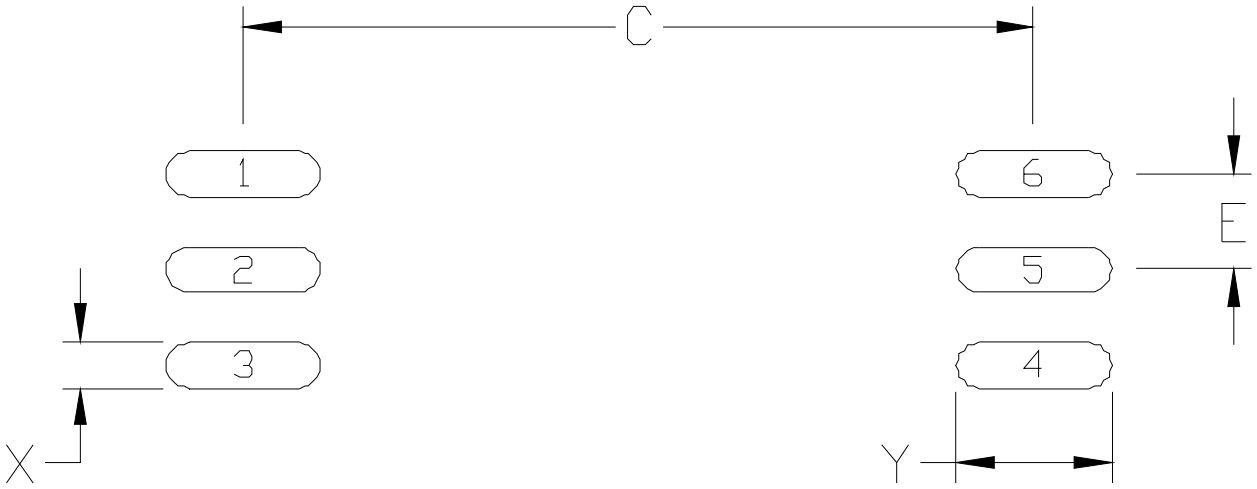



**Figure 20. SDIP6 Land Pattern**

**Table 21. SDIP6 Land Pattern Dimensions***

| Dimension | Min | Max |
|---|---|---|
| C | 10.45 | 10.50 |
| E | 1.27 BSC | |
| X | 0.55 | 0.60 |
| Y | 2.00 | 2.05 |
| ***Note:** This Land Pattern Design is based on the IPC-7351 specification. | | |

## 16. Package Outline: LGA8

Figure 21 illustrates the package details for the Si87xx in an LGA8 package. Table 22 lists the values for the dimensions shown in the illustration.

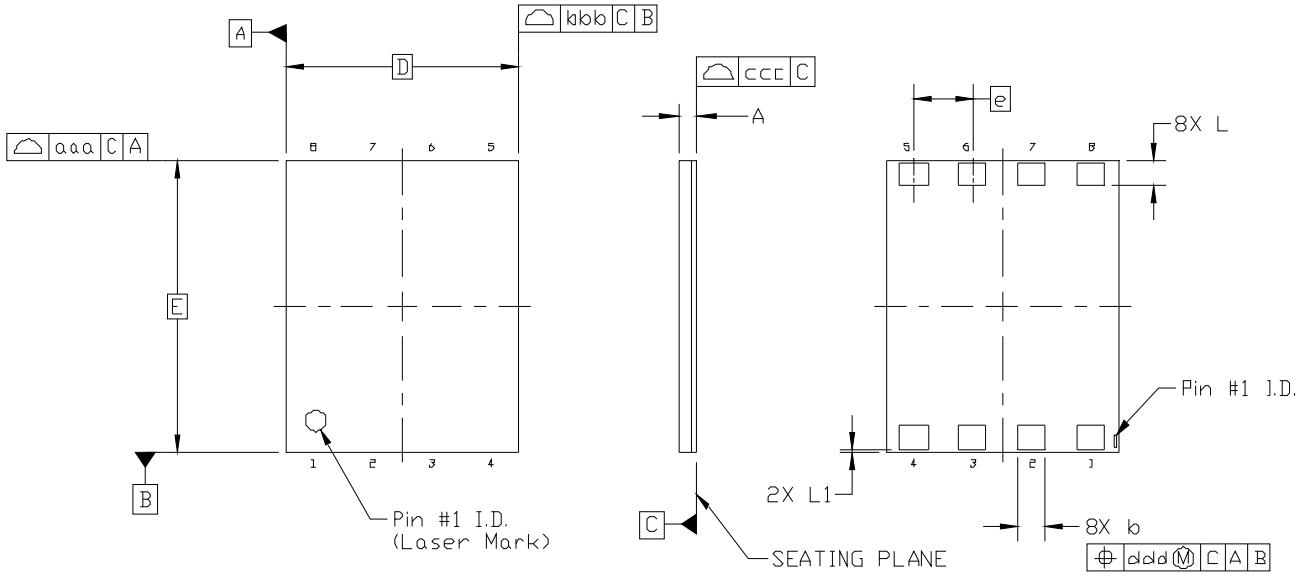



**Figure 21. LGA8 Package**

**Table 22. Package Diagram Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.74 | 0.84 | 0.94 |
| b | 1.15 | 1.20 | 1.25 |
| D | 10.00 BSC. | | |
| e | 2.54 BSC. | | |
| E | 12.50 BSC. | | |
| L | 1.05 | 1.10 | 1.15 |
| L1 | 0.05 | 0.10 | 0.15 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.10 |
| ddd | — | — | 0.10 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 17. Land Pattern: LGA8

Figure 22 illustrates the recommended land pattern details for the Si87xx in an LGA8 package. Table 23 lists the values for the dimensions shown in the illustration.

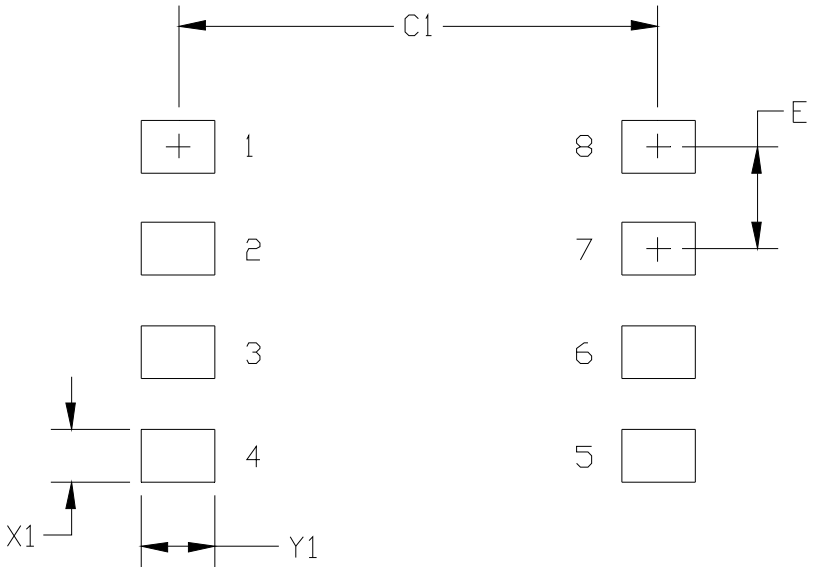



**Figure 22. LGA8 Land Pattern**

**Table 23. LGA8 Land Pattern Dimensions**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 11.80 |
| E | Pad Row Pitch | 2.54 |
| X1 | Pad Width | 1.30 |
| Y1 | Pad Length | 1.80 |

**Notes:**
1. This Land Pattern Design is based on IPC-7351 specifications.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 18. Top Marking: 8-Pin Narrow Body SOIC

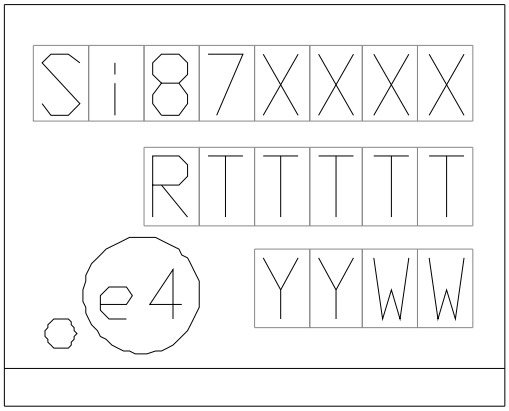



**Figure 23. 8-Pin Narrow Body SOIC Top Marking**

**Table 24. 8-Pin Narrow Body SOIC Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Customer Part Number | Si87xxxx |
| **Line 2 Marking:** | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form.<br>“R” indicates revision. |
| **Line 3 Marking:** | Circle = 43 mils Diameter<br>Left-Justified | “e4” Pb-Free Symbol |
| | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |

## 19. Top Marking: DIP8

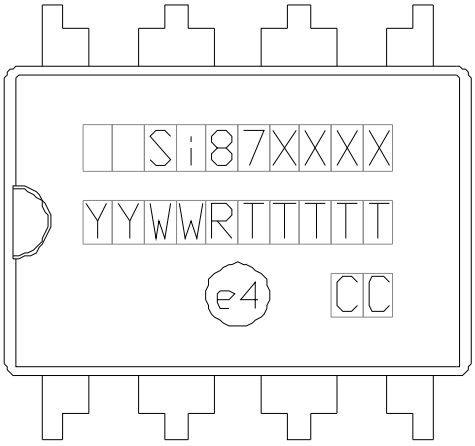



**Figure 24. DIP8 Top Marking**

**Table 25. DIP8 Top Marking Explanations**

| | | |
|---|---|---|
| **Line 1 Marking:** | Customer Part Number | Si87xxxx |
| **Line 2 Marking:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form.<br>“R” indicates revision. |
| **Line 3 Marking:** | Circle = 51 mils Diameter<br>Center-Justified | “e4” Pb-Free Symbol |
| | Country of Origin<br>(Iso-Code Abbreviation) | TH |

## 20. Top Marking: SDIP6

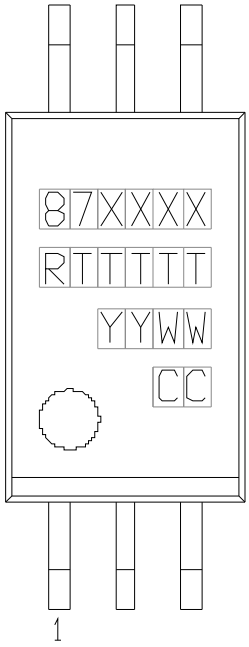



**Figure 25. SDIP6 Top Marking**

**Table 26. SDIP6 Top Marking Explanations**

| | | |
|---|---|---|
| **Line 1 Marking:** | Device | 87xxxx |
| **Line 2 Marking:** | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form.<br>“R” indicates revision. |
| **Line 3 Marking:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| **Line 4 Marking:** | Country of Origin<br>(Iso-Code Abbreviation) | TH |

## 21. Top Marking: LGA8

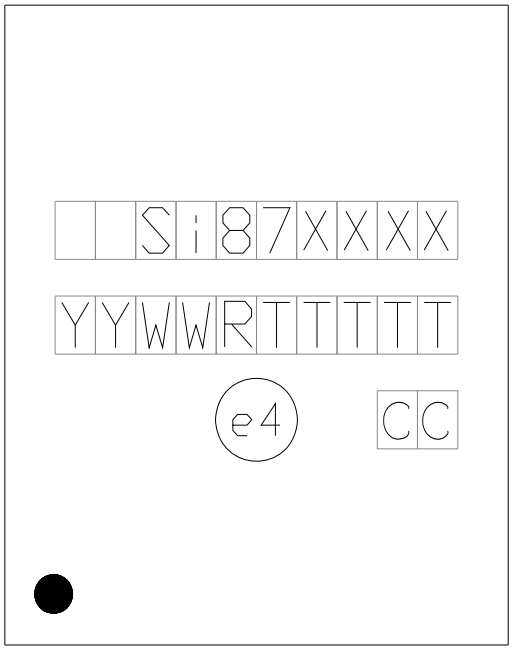



**Figure 26. LGA8 Top Marking**

**Table 27. LGA8 Top Marking Explanations**

| | | |
|---|---|---|
| **Line 1 Marking:** | Device Part Number | Si87xxxx |
| **Line 2 Marking:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. |
| | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision. |
| **Line 3 Marking:** | Circle = 1.6 mm Diameter<br>Center-Justified | "e4" Pb-Free Symbol |
| | Country of Origin<br>ISO Code Abbreviation | CC |
| **Line 4 Marking:** | Circle = 0.75 mm Diameter<br>Lower Left-Justified | Pin 1 Identifier |

# Contact Information

**Silicon Laboratories Inc.**

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

**Patent Notice**

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.