

# BUK9E15-60E

## N-channel TrenchMOS logic level FET

11 September 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in a SOT226 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

### 1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	60	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>	-	-	54	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	-	-	96	W
<b>Static characteristics</b>						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	-	11.6	15	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; V <sub>DS</sub> = 48 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	6.7	-	nC

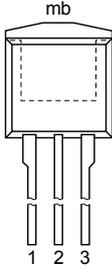
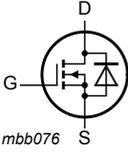


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## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>I2PAK (SOT226)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9E15-60E	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

## 4. Limiting values

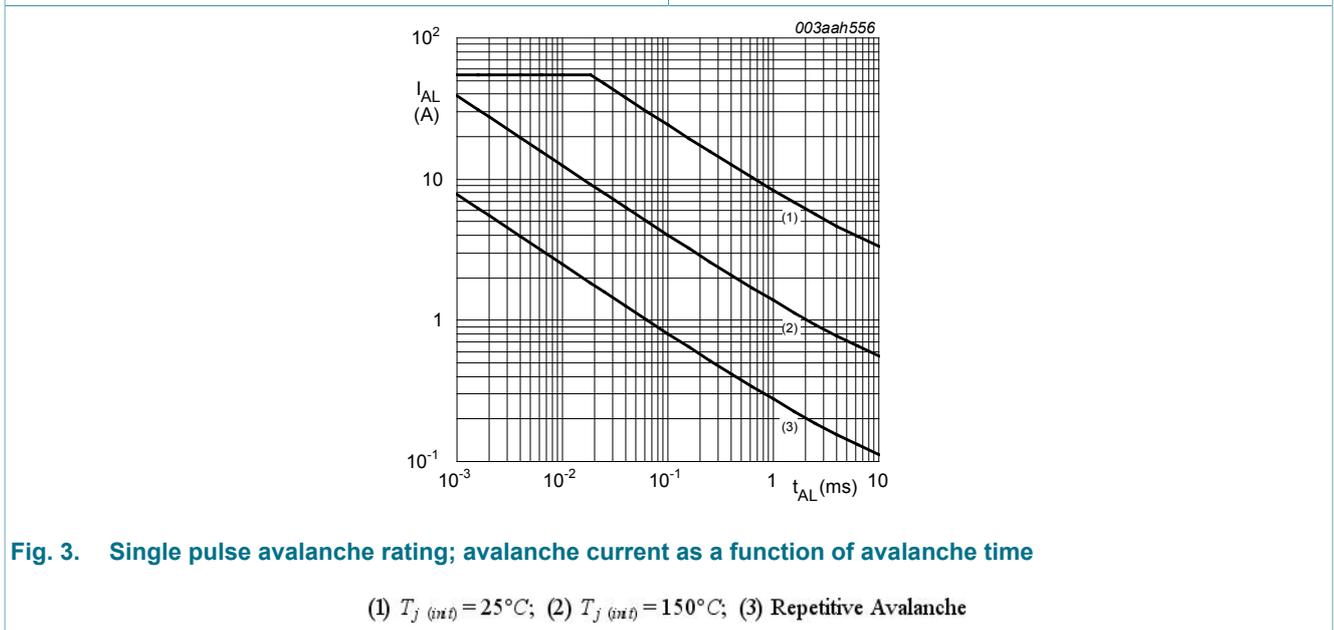
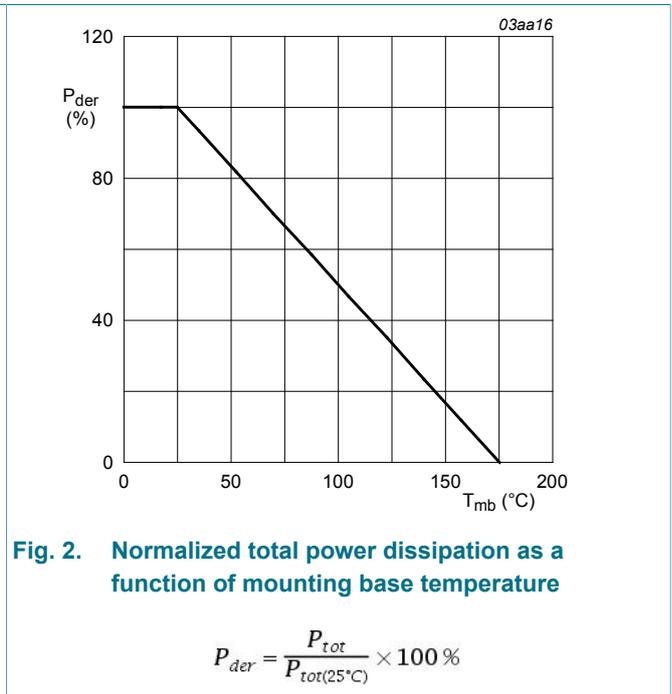
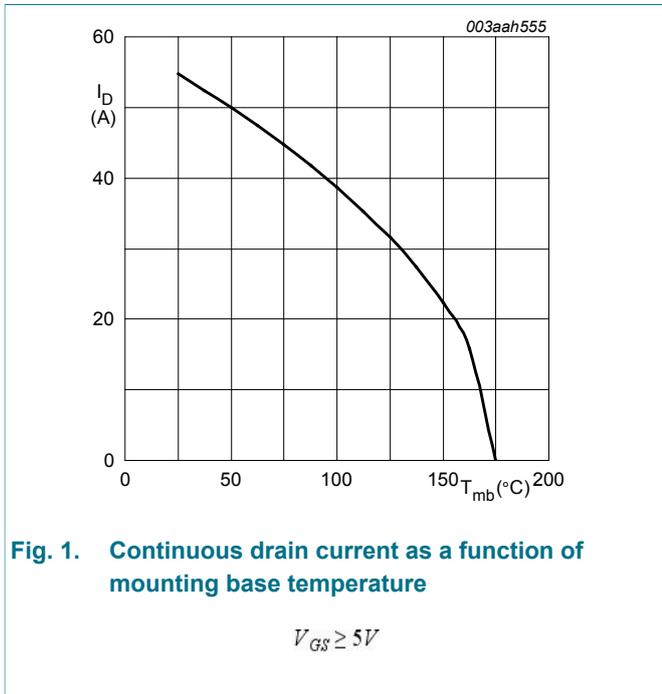
**Table 4. Limiting values**

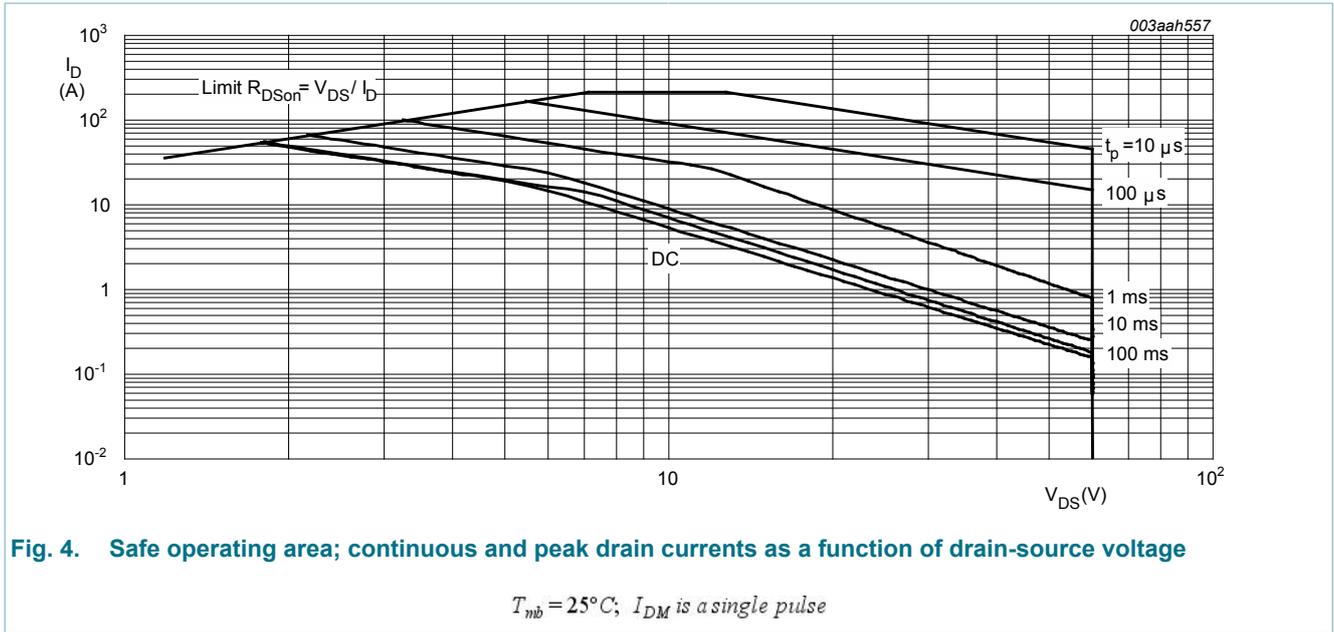
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ }^\circ\text{C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ }^\circ\text{C}$ ; Pulsed	[1][2] -15	15	V
$I_D$	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	54	A
		$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	38	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	216	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; Fig. 2	-	96	W
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ }^\circ\text{C}$	[3] -	54	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$	-	216	A

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 54 \text{ A}$ ; $V_{sup} \leq 60 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 5 \text{ V}$ ; $T_{j(init)} = 25 \text{ }^\circ\text{C}$ ; unclamped; <a href="#">Fig. 3</a>	[4][5]	-	40.5 mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering  $T_j$  and or  $V_{GS}$
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.

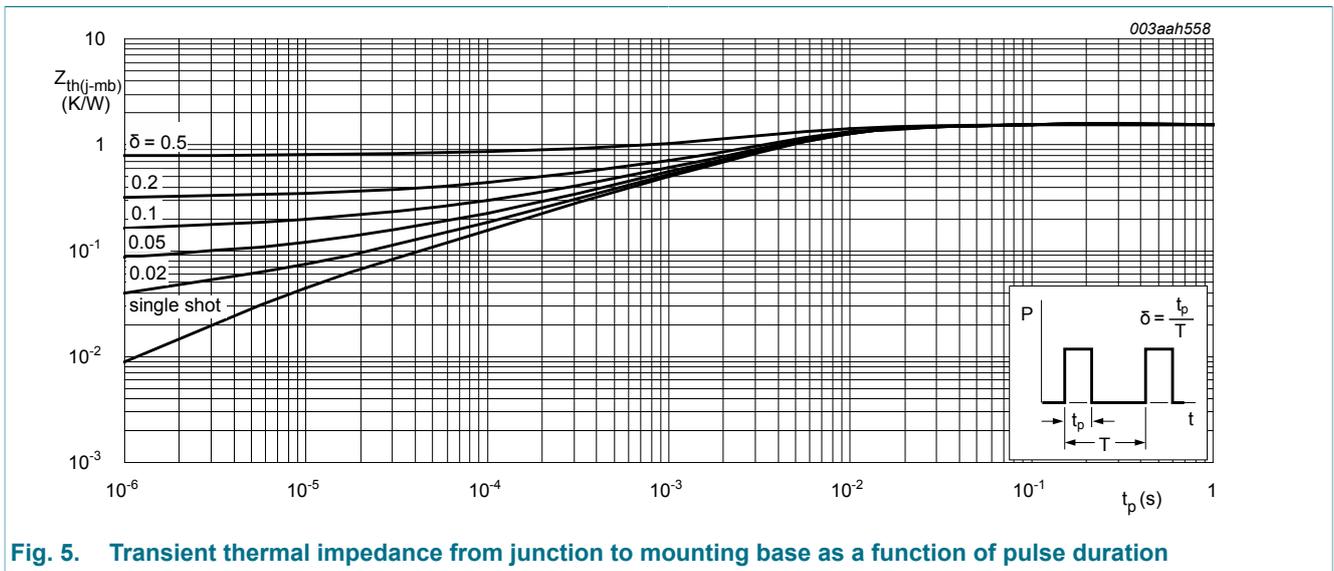




### 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	65	-	K/W

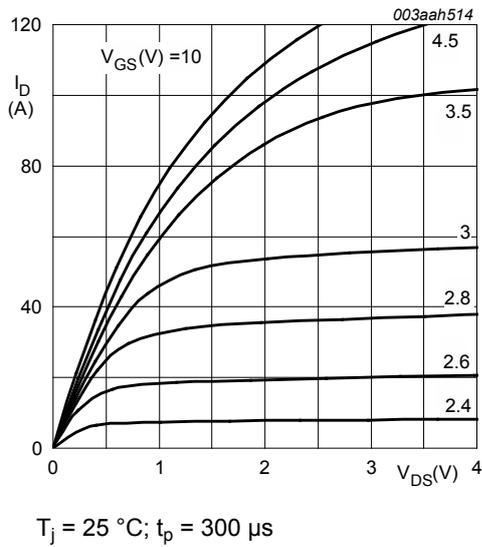


## 6. Characteristics

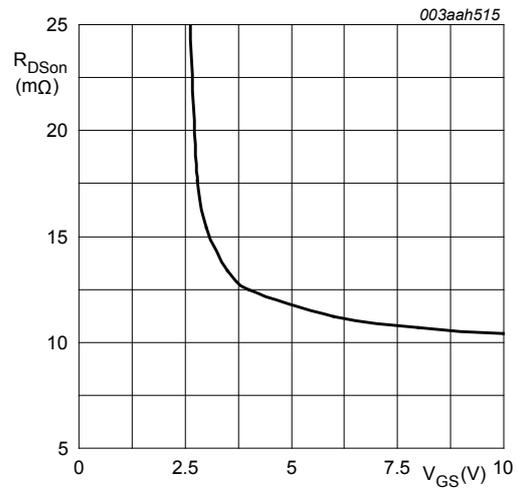
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	11.6	15	m $\Omega$
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	10.3	13	m $\Omega$
		$V_{GS} = 5 V; I_D = 15 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 11</a>	-	-	33	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 48 V; V_{GS} = 5 V;$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	20.5	-	nC
$Q_{GS}$	gate-source charge		-	4	-	nC
$Q_{GD}$	gate-drain charge		-	6.7	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 15</a>	-	1988	2651	pF
$C_{oss}$	output capacitance		-	196	235	pF
$C_{rss}$	reverse transfer capacitance		-	114	156	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45 V; R_L = 3 \Omega; V_{GS} = 5 V;$ $R_{G(ext)} = 5 \Omega$	-	16.9	-	ns
$t_r$	rise time		-	22.4	-	ns
$t_{d(off)}$	turn-off delay time		-	35.7	-	ns
$t_f$	fall time		-	22.9	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die ; $T_j = 25 \text{ }^\circ C$	-	2.5	-	nH
		from drain lead 6mm from package to centre of die ; $T_j = 25 \text{ }^\circ C$	-	4.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$L_S$	internal source inductance	from source lead to source bonding pad ; $T_j = 25\text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; Fig. 16	-	0.83	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	22.3	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}$	-	20.9	-	nC

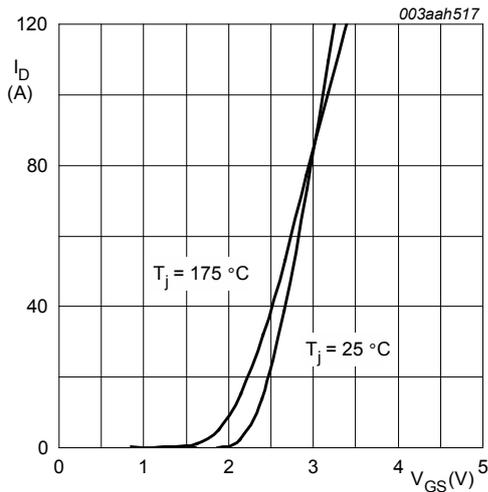


**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



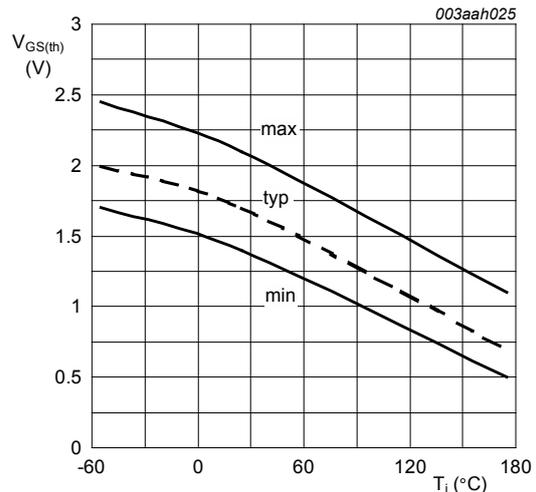
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 15\text{ A}$



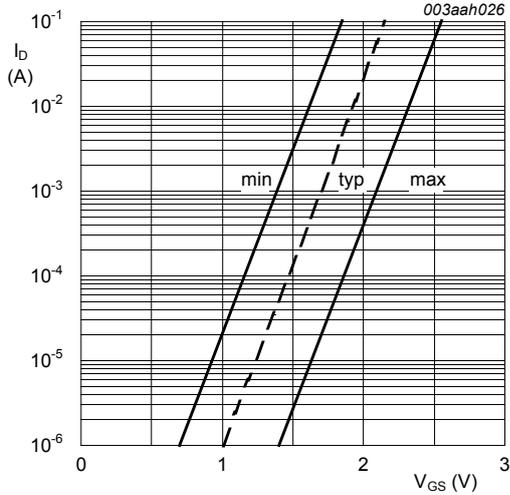
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10\text{ V}$



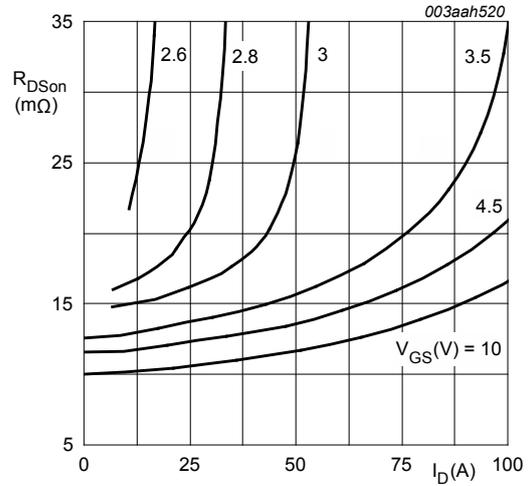
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$



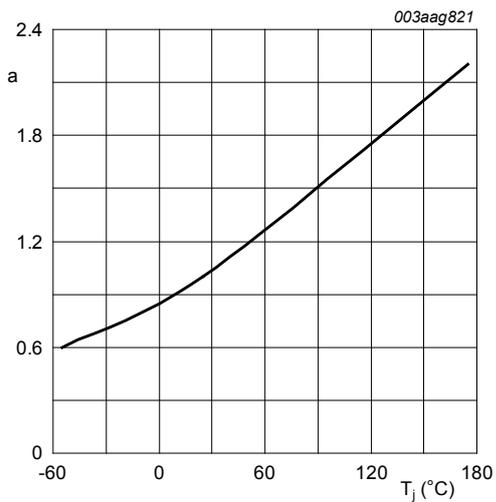
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$



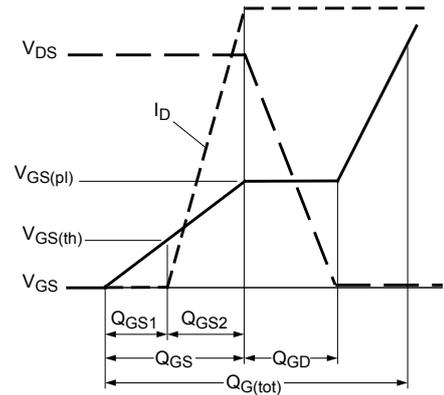
$T_j = 25^\circ\text{C}; t_p = 300\ \mu\text{s}$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

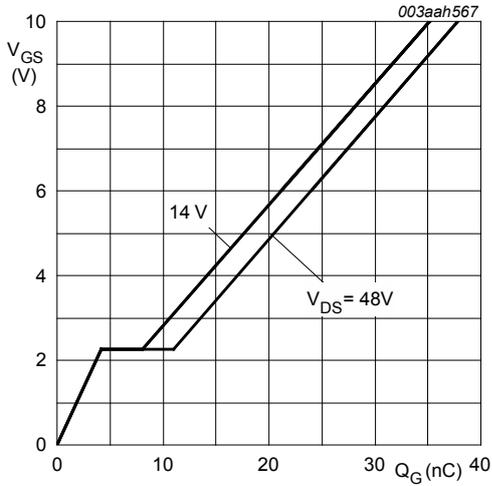


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

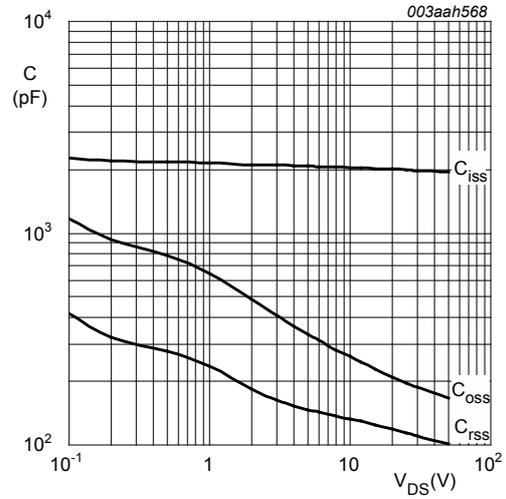


**Fig. 13. Gate charge waveform definitions**



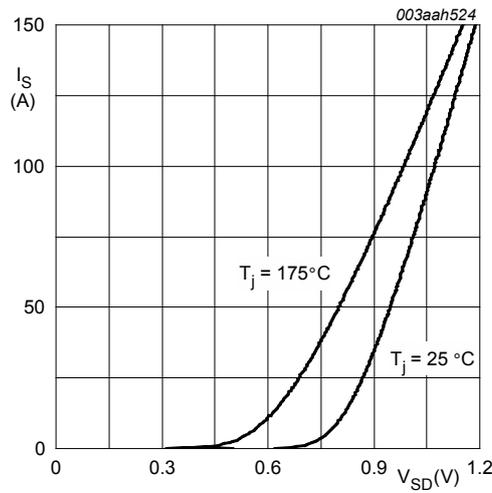
**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$T_j = 25^\circ\text{C}; I_D = 15\text{A}$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$V_{GS} = 0\text{V}; f = 1\text{MHz}$



**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$V_{GS} = 0\text{V}$

## 7. Package outline

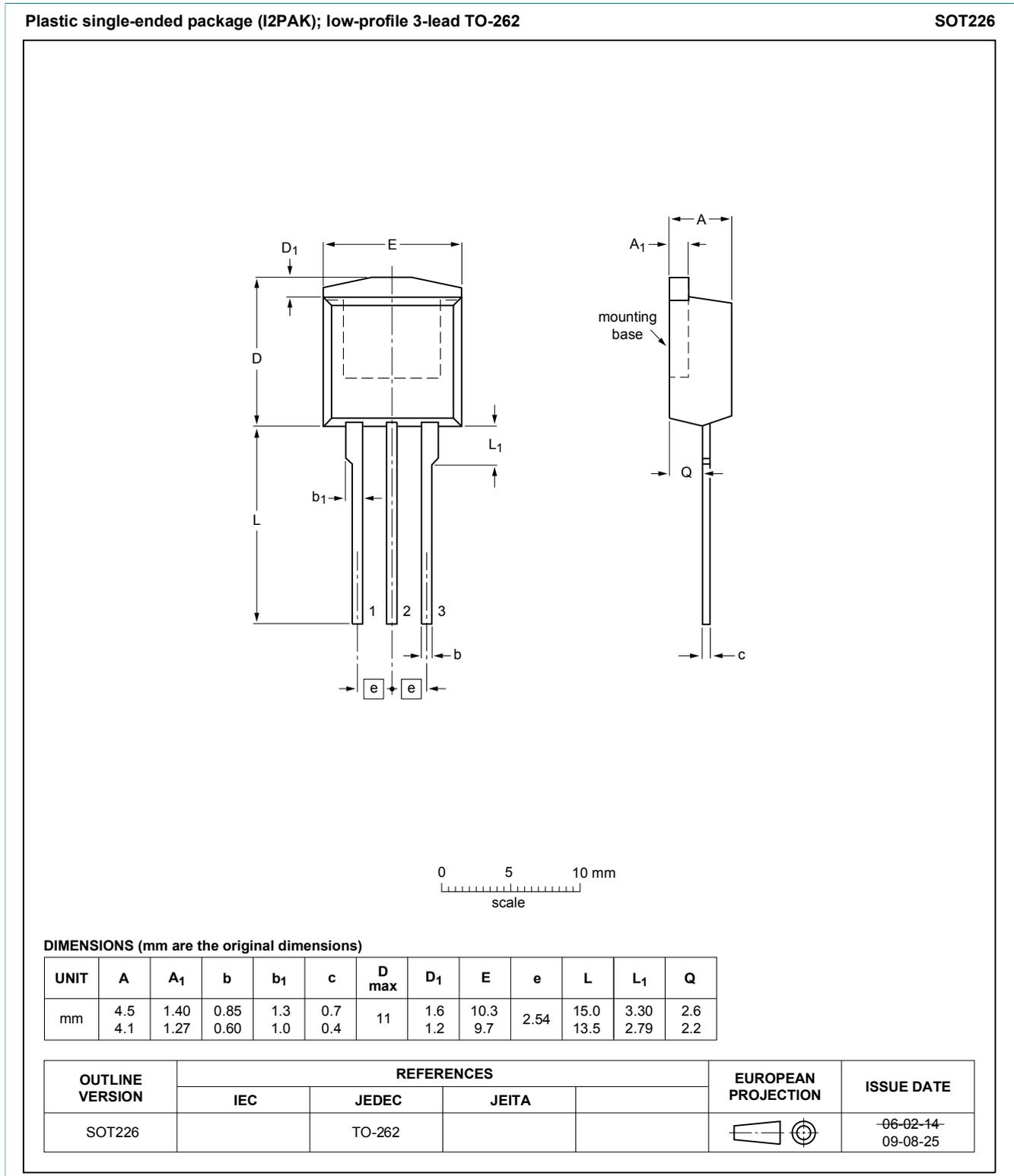


Fig. 17. Package outline I2PAK (SOT226)

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Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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