FEUL610Q111-02

LAPIS SEMICONDUCTOR

ML610Q111/ML610Q112
User's Manual

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q111 / ML610Q112.

The following manuals are also available. Read them as necessary.

- nX-U8/100 Core Instruction Manual
  Description on the basic architecture and the each instruction of the nX-U8/100 Core.

- MACU8 Assembler Package User's Manual
  Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

- CCU8 User's Manual
  Description on the method of operating the compiler.

- CCU8 Programming Guide
  Description on the method of programming.

- CCU8 Language Reference
  Description on the language specifications.

- DTU8 Debugger User's Manual
  Description on the method of operating the debugger DTU8.

- IDEU8 User's Manual
  Description on the integrated development environment IDEU8.

- uEASE User's Manual
  Description on the on-chip debug tool uEASE.

- uEASE connection Manual for ML610QXXX
  Description about the connection between uEASE and ML610Q111 and ML610Q112.

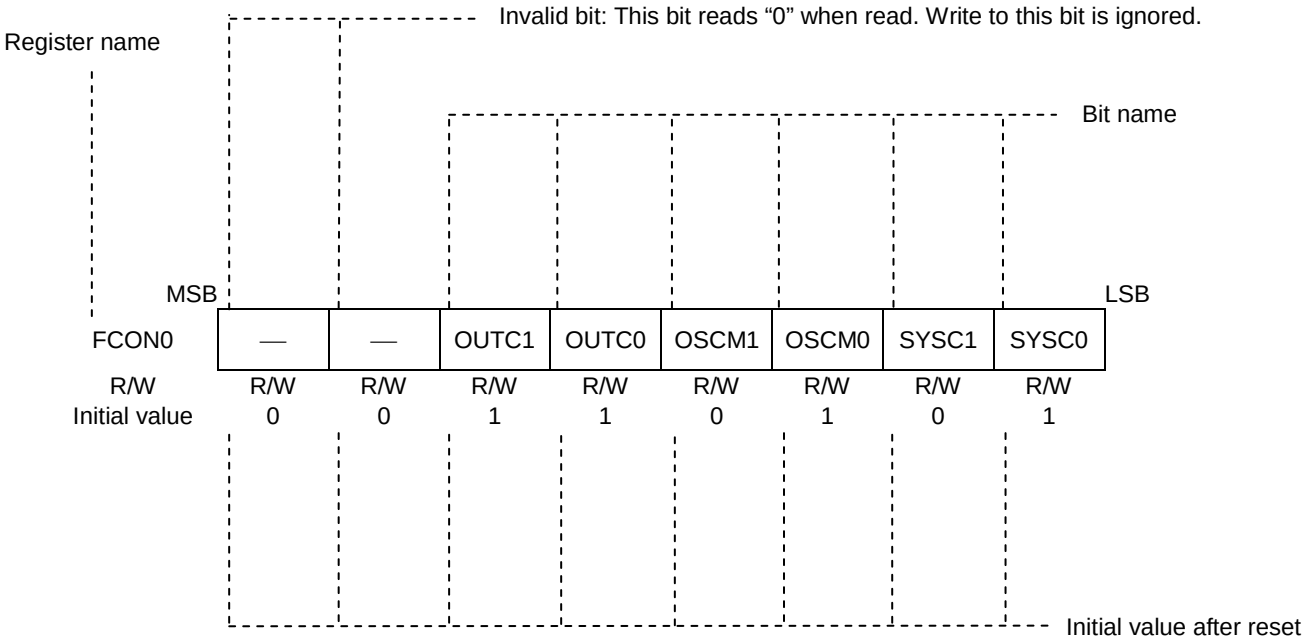
- FWuEASE Flash Writer Host Program User's Manual
  Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1 Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as timers, PWM, UART, I^2C bus interface (master/slave), synchronous serial port, voltage level supervisor (VLS) function, and 10-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipe line architecture parallel processing. It has a data-flash memory that can be written by software.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system : 16-bit instructions
  - Instruction set :
    Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5µs (@32.768kHz system clock)
    0.122µs (@8.192MHz system clock)

- Internal memory
  - ML610Q111 :
    Flash memory :
    Internal 24Kbyte Flash memory (12K×16 bits) for program (including unusable 32 byte test data area)
    Internal 4Kbyte Flash memory (2 K ×16 bits) for data
    SRAM :
    Internal 2Kbyte (2K×8 bits)
  - ML610Q112 :
    Flash memory :
    Internal 32Kbyte Flash memory (16K×16 bits) for program (including unusable 32 byte test data area)
    Internal 4Kbyte (2 K ×16 bits) for data
    SRAM :
    Internal 4Kbyte (4K×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source (Internal source: 1)
  - 30 maskable interrupt sources (Internal sources: 23, External sources: 7)

- Time base counter (TBC)
  - Low-speed time base counter × 1 channel
  - High-speed time base counter × 1 channel
    (This time base counter is divided by 1-16, then it can be used as a clock of the Timer and PWM.)

- Watchdog timer (WDT)
  - Non-maskable interrupt and reset
    (Non-maskable interrupt is generated by the first overflow, and reset is generated by the second overflow)
  - Free running
  - Overflow period: 7 types selectable by software (23.4ms, 31.25ms, 62.5ms, 125ms, 500ms, 2s, and 8s)

- Timer
  - 8 bits × 6 channels (16-bit configuration available)
  - Supports auto reload timer mode/one shot timer mode
  - Timer start/stop function by software or external trigger input
    (Timer function with external trigger input supports for only 2ch. Selectable external pins/analog comparator output as an exeternal trigger.)
  - The effective minimum pulse width of the external trigger input: Timer clock 3ϕ (about 183 ns @ 16.384 MHz)
  - Allows measurement of pulse width etc. using an external trigger input.

- PWM
  - Resolution 16 bits × 4 channels
  - Allows an output of the PWM signal in a cycle of about 122ns (@PLLCLK = 16.384MHz) to 2s (@LSCLK = 32.768kHz)
  - Supports one shot PWM mode
  - PWM start/stop function by software or external trigger input
    (Selectable external pins, analog comparator output or timer interrupt as external trigger.)
  - The effective minimum pulse width of the external trigger input: Timer clock 3ϕ (about 183 ns @ 16.384MHz)

- UART
  - TXD/RXD × 2 channels
  - Half-duplex
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C Bus Interface
  - Master function: Standard mode (100 kbits/s @ 8 MHz), First mode (400 kbits/s @ 8 MHz)
  - Slave function: Standard mode (100 kbits/s)

- Synchronous Serial Port (SSIO)
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- Successive approximation type A/D converter (SA-ADC)
  - 10-bit A/D converter
  - ML610Q111: Analog Input : 6channels
  - ML610Q112: Analog Input : 8channels

- Analog Comparator
  - 2ch
    ch0: Allows comparison of the voltage level of the two external pins or comparison of one external pin and internal reference voltage level.
    ch1: Allows comparison of one external pin and internal reference voltage level.
  - Common mode input voltage range : V_{DD} = 0.1V to V_{DD} - 1.5V
  - Internal reference voltage : 0.1-0.8V (Selectable in 50mV increments)
  - Hysteresis (Comparator0 only): 20mV(Typ.)
  - Allows selection of with/without interrupt sampling and interrupt edge.

- General-purpose ports (GPIO)
  - ML610Q111 : Input/output port × 15 channels
  - ML610Q112 : Input/output port × 25 channels

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by the watchdog timer (WDT) 2nd overflow
  - Reset by voltage level supervisor (VLS) function: Selectable by software

- Voltage level supervisor (VLS)
  - 2ch
    ch0: It can be used for voltage level detection reset.
    ch1: It can be used for voltage level detection interrupt.
  - Judgment accuracy: ±3.0% (Typ.)

- Clock
  - Low-speed clock:
    Built-in RC oscillation (32.768 kHz)
  - High-speed clock:
    Built-in PLL oscillation (16.384 MHz), external clock(max. 8.192MHz)
    * The clock of the CPU is 8.192MHz(max.)
  - Selection of high-speed clock mode by software:
    Built-in PLL oscillation, external clock

- Power management
  - HALT mode : Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode : Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear : The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4 or 1/8 of the oscillation clock)
  - Block Control Function : Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - ML610Q111 :
    20-pin TSSOP
    ML610Q111-xxxTD (Blank product: ML610Q111-NNNTD)
  - ML610Q112 :
    32-pin LQFP
    ML610Q112-xxxTC (Blank product: ML610Q112-NNNTC)

- Guaranteed operating range
  - Operating temperature: –40°C to 105°C (When the flash memory writing/erasing : –20°C to 85°C)
  - Operating voltage: V_{DD} = 2.7V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram

Figure 1-1 show the block diagram of the LSI.
"*" indicates secondary function, tertiary function or quaternary function of each port.
" ( )*2" indicates the specification of ML610Q112.

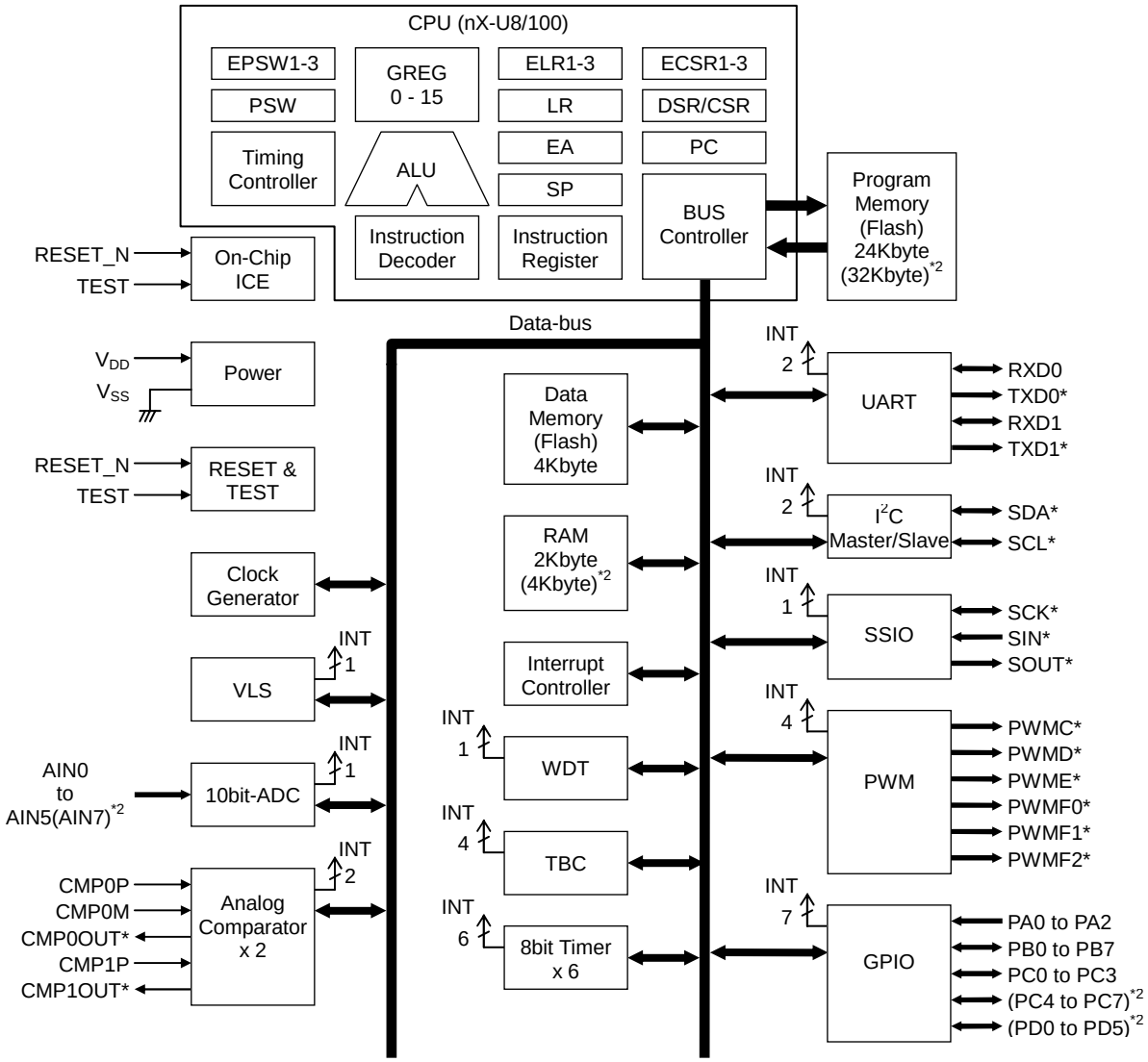
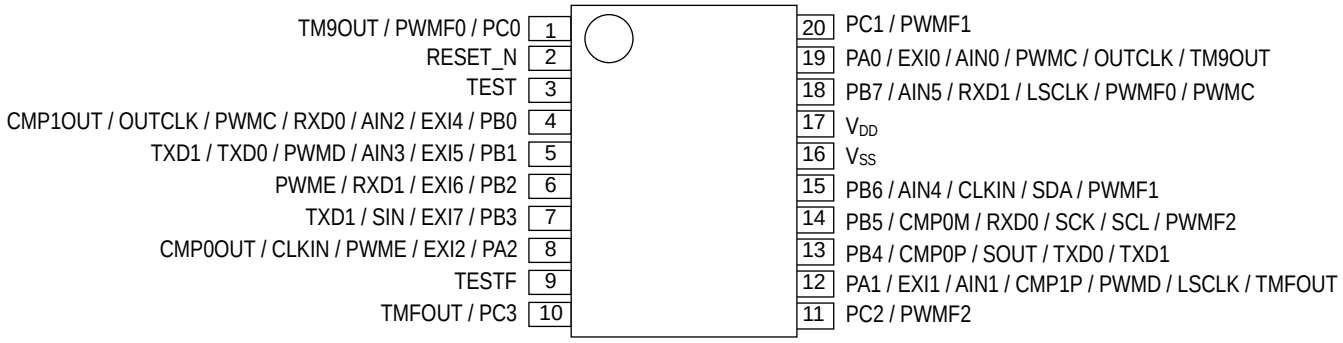


Figure 1-1 ML610Q111/ML610Q112 Block Diagram

1.3 Pins

1.3.1 Pin Layout

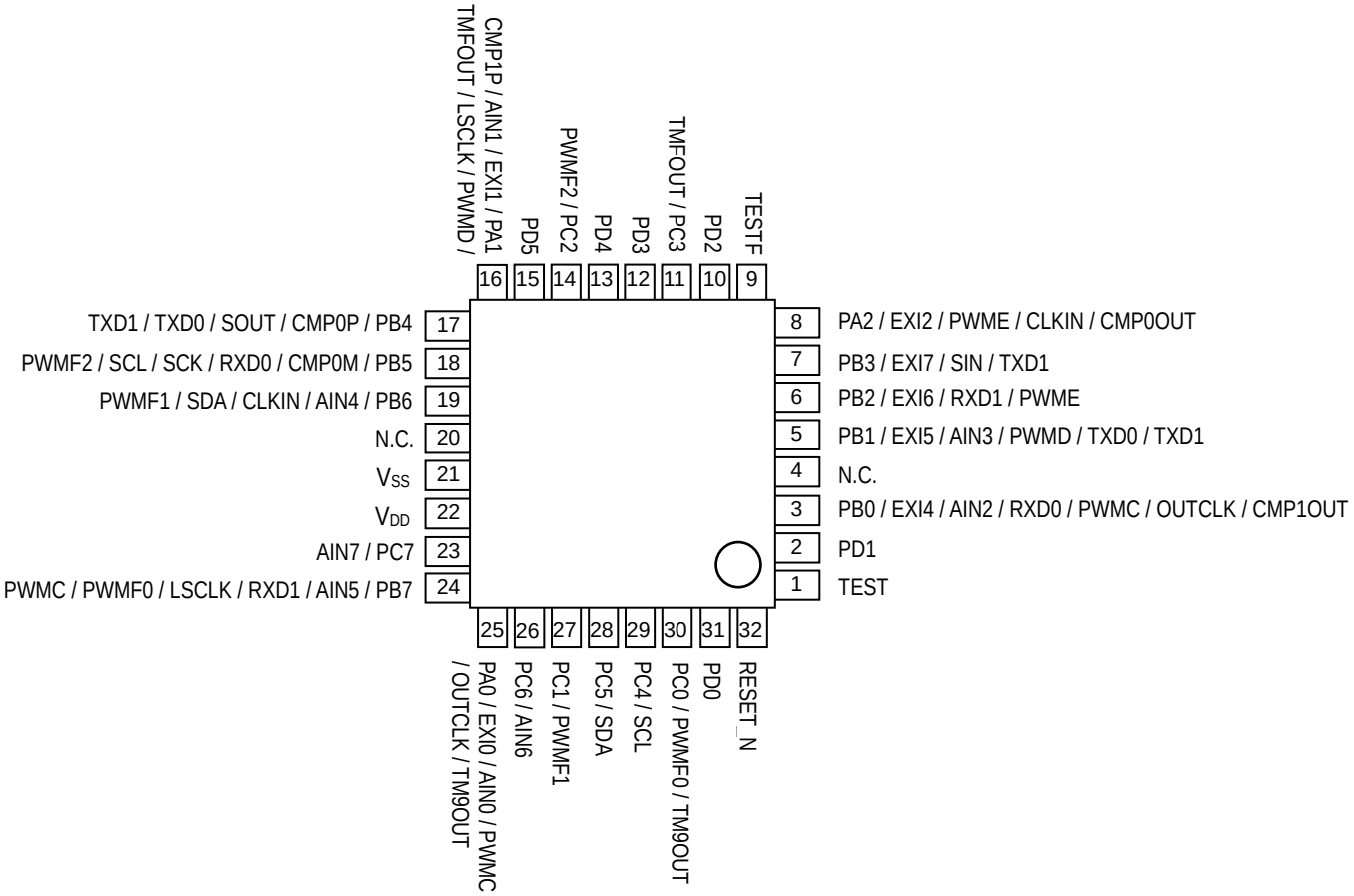
Figure 1-2 show the TSSOP20 pin layout of the ML610Q111.



* PIN No.4-8, 12-15, 18, 19 can be used as external trigger of the Timer E-F and PWMC-F.

Figure 1-2 Pin Layout of ML610Q111 TSSOP20 Package

Figure 1-3 show the LQFP32 pin layout of the ML610Q112.



* PIN No.3, 5-8, 16-19, 24, 25 can be used as external trigger of the Timer E- F and PWMC-F.

Figure 1-3 Pin Layout of ML610Q112 LQFP32 Package

1.3.2 List of Pins

Table 1-1 shows list of pins.

In the I/O column, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Table 1-1 List of pins

PIN No.		Primary function			Secondary function			Tertiary function			quaternary function		
32 LQFP	20 TSSOP	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
21	16	V_{SS}	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
22	17	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
9	9	TESTF	—	Test for Flash memory	—	—	—	—	—	—	—	—	—
32	2	RESE T_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
1	3	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—	—	—	—
25	19	PA0/ EXI0/ AIN0	I/O	Input/output port / External interrupt / ADC input	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	TM9OUT	O	timer 9 output
16	12	PA1/ EXI1/ AIN1/ CMP1P	I/O	Input/output port / External interrupt / ADC input / Analog comparator 1 non-inverted input	PWMD	O	PWMD output	LSCLK	O	Low-speed clock output	TMFOUT	O	timer F output
8	8	PA2/ EXI2	I/O	Input/output port / External interrupt / External trigger	PWME	O	PWME output	CLKIN	I	clock input	CMP0OUT	O	CMP0 output
3	4	PB0/ EXI4/ AIN2/ RXD0	I/O	Input/output port / External interrupt / ADC input / UART0 data input / External trigger	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	CMP1OUT	O	CMP1 output
5	5	PB1/ EXI5/ AIN3	I/O	Input/output port / External interrupt / ADC input / External trigger	PWMD	O	PWMD output	TXD0	O	UART0 data output	TXD1	O	UART1 data output
6	6	PB2/ EXI6/ RXD1	I/O	Input/output port / External interrupt / UART1 data input / External trigger	PWME	O	PWME output	—	—	—	—	—	—
7	7	PB3/ EXI7	I/O	Input/output port / External interrupt / External trigger	SIN	I	SSIO data input	TXD1	O	UART1 data output	—	—	—
17	13	PB4/ CMP0P	I/O	Input/output port / Analog comparator 0 non-inverted input / External trigger	SOUT	O	SSIO data output	TXD0	O	UART0 data output	TXD1	O	UART1 data output
18	14	PB5/ RXD0/ CMP0M	I/O	Input/output port / UART0 data input / Analog comparator 0 inverted input / External trigger	SCK	I/O	SSIO clock input/output	SCL	I/O	I2C clock	PWMF2	O	PWMF2 output
19	15	PB6/ AIN4	I/O	Input/output port / ADC input / External trigger	CLKIN	I	clock input	SDA	I/O	I2C data	PWMF1	O	PWMF1 output
24	18	PB7/ AIN5/ RXD1	I/O	Input/output port / Analog comparator 0 inverted input / UART data input / External trigger	LSCLK	O	Low-speed clock output	PWMF0	O	PWMF0 output	PWMC	O	PWMC output

PIN No.		Primary function			Secondary function			Tertiary function			quaternary function		
32 LQFP	20 TSSOP	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
30	1	PC0	I/O	Input/output port	—	—	—	PWMF0	O	PWMF 0output	TM9OUT	O	timer 9 output
27	20	PC1	I/O	Input/output port	—	—	—	PWMF1	O	PWMF 1output	—	—	—
14	11	PC2	I/O	Input/output port	—	—	—	PWMF2	O	PWMF 2output	—	—	—
11	10	PC3	I/O	Input/output port	—	—	—	—	—	—	TMFOUT	O	timer F output
29	—	PC4	I/O	Input/output port	SCL	I/O	I2C clock	—	—	—	—	—	—
28	—	PC5	I/O	Input/output port	SDA	I/O	I2C data	—	—	—	—	—	—
26	—	PC6/ AIN6	I/O	Input/output port / ADC input	—	—	—	—	—	—	—	—	—
23	—	PC7/ AIN7	I/O	Input/output port / ADC input	—	—	—	—	—	—	—	—	—
31	—	PD0	I/O	Input/output port	—	—	—	—	—	—	—	—	—
2	—	PD1	I/O	Input/output port	—	—	—	—	—	—	—	—	—
10	—	PD2	I/O	Input/output port	—	—	—	—	—	—	—	—	—
12	—	PD3	I/O	Input/output port	—	—	—	—	—	—	—	—	—
13	—	PD4	I/O	Input/output port	—	—	—	—	—	—	—	—	—
15	—	PD5	I/O	Input/output port	—	—	—	—	—	—	—	—	—

*: The External trigger is indicated the Timer E, F or the PWMC-F external trigger input (TETG,TFTG, PCTG, PDTG, PETG, PFTG).

1.3.3 Description of Pins

Table 1-2 shows description of pins.

Table 1-2 (1/3) Description of pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
CLKIN	I	High-speed clock output pin. This pin is used as the tertiary function of the PA2 or the secondary function of PB6 pin.	Secondary/ Tertiary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the tertiary function of the PA1 or the secondary function of the PB7 pin.	Secondary/ Tertiary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the tertiary function of the PA0 or PB0 pin.	Tertiary	—
General-purpose input/output port				
PA0 to PA2 PB0 to PB7 PC0 to PC7 PD0 to PD5	I/O	General-purpose input/output port. Since these pins have secondary functions and tertiary functions and quaternary functions, the pins cannot be used as a port when the secondary functions and tertiary functions and quaternary functions are used.	Primary	Positive
External interrupt				
EXI0 to 2, EXI4 to 7	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PA0 – PA2 and PB0 – PB3 pins.	Primary	Positive/ Negative
Synchronous Serial Port (SSIO)				
SIN	I	Synchronous serial data input pin. This pin is used as the secondary function of the PB3 pin.	Secondary	Positive
SCK	I/O	Synchronous clock input/output pin. This pin is used as the secondary function of the PB5 pin.	Secondary	—
SOUT	O	Synchronous serial data output pin. This pin is used as the secondary function of the PB4 pin.	Secondary	Positive
UART				
TXD0	O	UART0 data output pin. This pin is used as the tertiary function of the PB1 or PB4 pin.	Tertiary	Positive
RXD0	I	UART0 data input pin. This pin is used as the primary function of the PB0 or PB5 pin.	Primary	Positive
TXD1	O	UART1 data output pin. This pin is used as the quaternary function of the PB0 or PB1 or the tertiary function of the PB3 pin.	Tertiary/ Quaternary	Positive
RXD1	I	UART1 data input pin. This pin is used as the primary function of the PB2 or PB7 pin.	Primary	Positive
I^2C Bus Interface				
SCL	I/O	I^2C clock pin. This pin is used as the tertiary function of the PB5 or the secondary function of the PC4 pin.	Secondary/ Tertiary	Positive
SDA	I/O	I^2C data pin. This pin is used as the tertiary function of the PB6 or the secondary function of the PC5 pin.	Secondary/ Tertiary	Positive

Table 1-2 (2/3) Description of pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Timer				
TETG, TFTG	I	External clock input pin used for both Timer E and Timer F. These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins.	Primary	—
TM9OUT	O	Timer 9 output pin. This pin is used as the quaternary function of the PA0 or PC0 pin.	Quaternary	Positive
TMFOUT	O	Timer F output pin. This pin is used as the quaternary function of the PA1 or PC3 pin.	Quaternary	Positive
PWM				
PCTG, PDTG, PETG, PFTG	I	External trigger input pins of PWMC to PWMF. These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins.	Primary	—
PWMC	O	PWMC output pin. This pin is used as the secondary function of the PB0 or PA0 or the quaternary function of the PB7 pin.	Secondary/ Quaternary	Positive/ negative
PWMD	O	PWMC output pin. This pin is used as the secondary function of the PB1 or PA1 pin.	Secondary	Positive/ negative
PWME	O	PWME output pin. This pin is used as the secondary function of the PB2 or PA2 pin.	Secondary	Positive/ negative
PWMF0	O	PWMF0 output pin. This pin is used as the tertiary function of the PB7 or PC0 pin.	Tertiary	Positive/ negative
PWMF1	O	PWMF1 output pin. This pin is used as the quaternary function of the PB6 or the tertiary function of the PC1 pin.	Tertiary/ Quaternary	Positive/ negative
PWMF2	O	PWMF2 output pin. This pin is used as the quaternary function of the PB5 or the tertiary function of the PC2 pin.	Tertiary/ Quaternary	Positive/ negative
Successive approximation type A/D converter				
AIN0	I	Channel 0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin.	Primary	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin.	Primary	—
AIN2	I	Channel 2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin.	Primary	—
AIN3	I	Channel 3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin.	Primary	—
AIN4	I	Channel 4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin.	Primary	—
AIN5	I	Channel 5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin.	Primary	—
AIN6	I	Channel 6 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PC6 pin.	Primary	—
AIN7	I	Channel 7 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PC7 pin.	Primary	—
Comparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the PB4 pin.	Primary	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the PB5 pin.	Primary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PA2 pin.	Quaternary	—
CMP1P	I	Non-inverting input for comparator1. This pin is used as the primary function of the PA1 pin.	Primary	—
CMP1OUT	O	Output for comparator1. This pin is used as the quaternary function of the PB0 pin.	Quaternary	—

Table 1-2 (3/3) Description of pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	Positive
TESTF	—	Test pin for flash memory. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—

1.3.4 Termination of Unused Pins

Table 1-3 shows methods of terminating the unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST	Open
TESTF	Open
PA0 to PA2	Open
PB0 to PB7	Open
PC0 to PC7	Open
PD0 to PD5	Open
N.C.	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

Chapter 2

CPU and Memory Space

2 CPU and Memory Space

2.1 Overview

This LSI includes 8-bit CPU nX-U8/100 and the memory model is "SMALL model".
For details of the CPU nX-U8/100, see "nX-U8/100 Core Instruction Manual".

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The ROM window area data has a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of 1 segment and ML610Q111 has 24-Kbyte (12-Kword) capacity, ML610Q112 has 32-Kbyte (16-Kword) capacity.
Figure 2-1 shows the configuration of the program memory space of the ML610Q111.
Figure 2-2 shows the configuration of the program memory space of the ML610Q112.

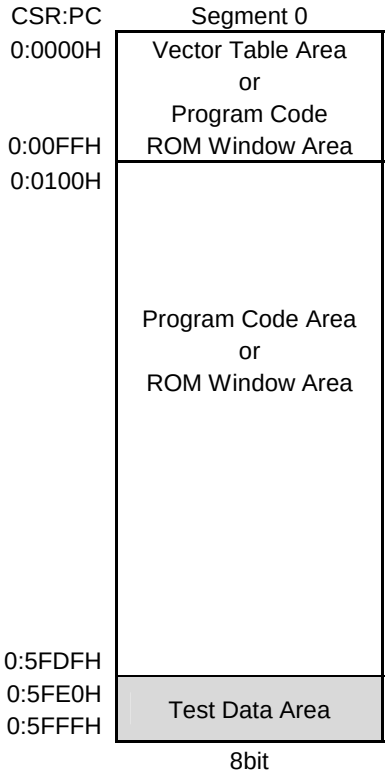


Figure 2-1 Configuration of Program Memory Space of the ML610Q111

Notes:
- Because test program data is stored in the 32 bytes (16 words) test data area (0: 5FE0H to 0:5FFFH) of the Segment 0, this area cannot be used as a program code area.
- The address "0: 5FE0H to 0: 5FFFH" in the test area is write-able and erase-able. Fill the area with "0FFH". If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

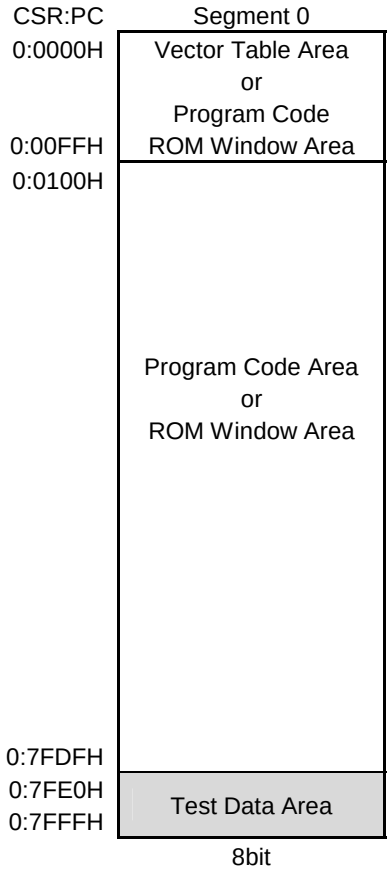


Figure 2-2 Configuration of Program Memory Space of the ML610Q112

Notes:
- Because test program data is stored in the 32 bytes (16 words) test data area (0:7FE0H to 0:7FFFH) of the Segment 0, this area cannot be used as a program code area.
- The address "0: 7FE0H to 0: 7FFFH" in the test area is write-able and erase-able. Fill the area with "0FFH". If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 2-Kbyte RAM area(ML610Q111), 4-Kbyte RAM area(ML610Q112) and SFR area and 4-Kbyte Segment 2 and A of the flash data area and the ROM reference areas of the Segment 8.
The data memory stores 8-bit data and is specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by each instruction.
Figure 2-3 shows the configuration of the data memory space of the ML610Q111.
Figure 2-4 shows the configuration of the data memory space of the ML610Q112.

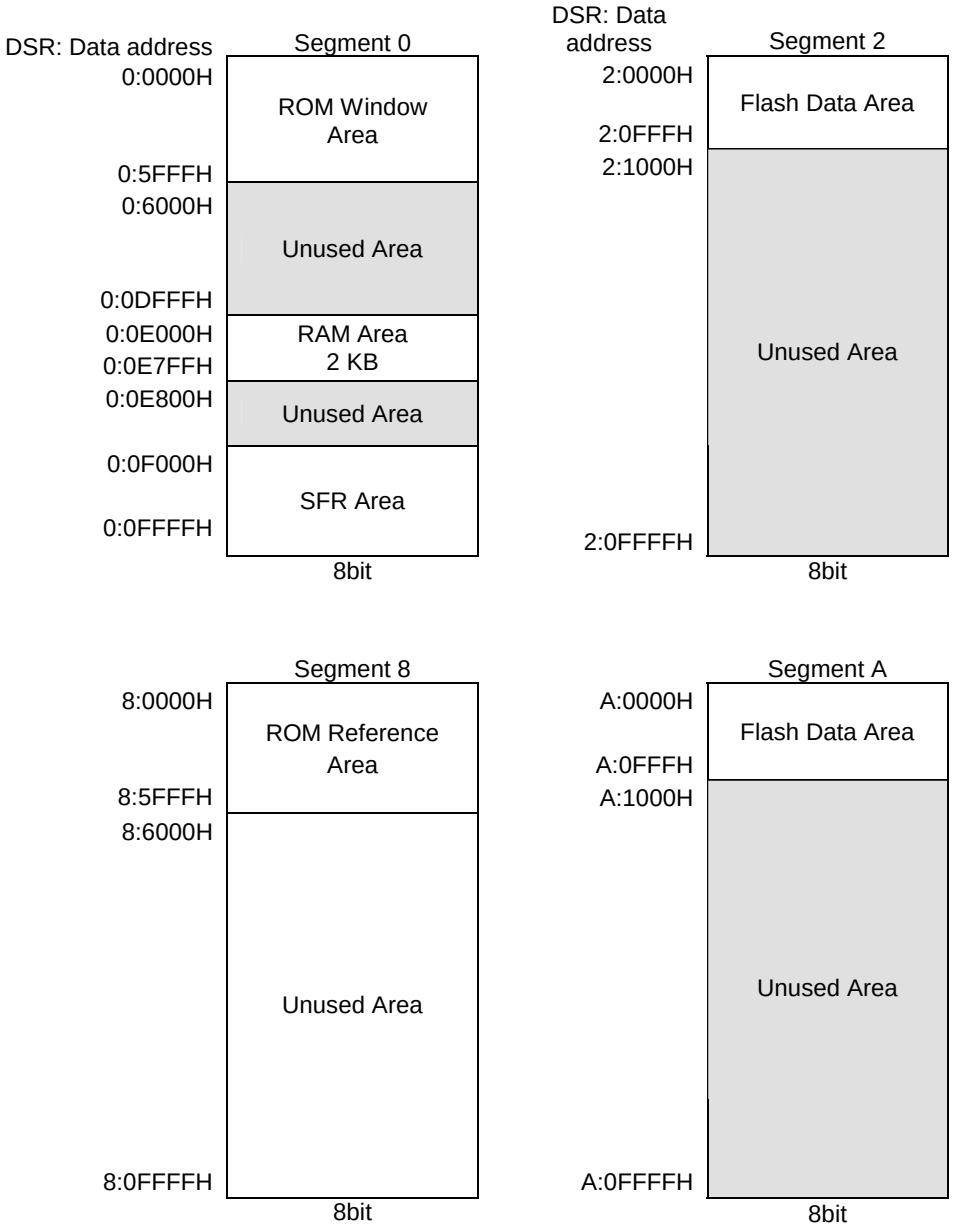


Figure 2-3 Configuration of Data Memory Space of the ML610Q111

Notes:
– The contents of the 2-Kbyte RAM area are undefined at power-on and system reset. Initialize this area by software.

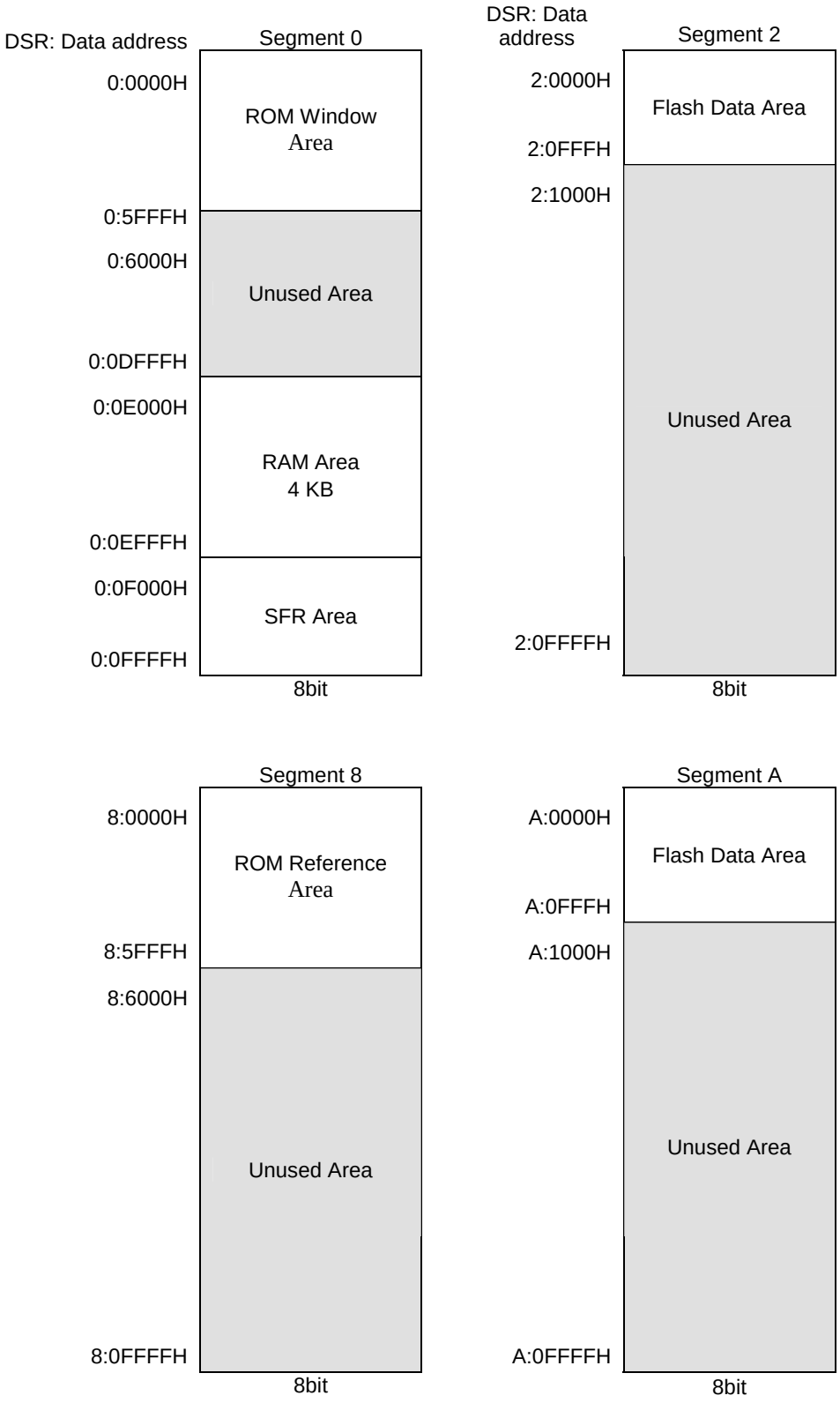


Figure 2-4 Configuration of Data Memory Space of the ML610Q112

Notes:
– The contents of the 4-Kbyte RAM area are undefined at power-on and system reset. Initialize this area by software.

2.4 Instruction Length

The length of an instruction is 16 bits.

2.5 Data Type

The data types supported include byte (8 bits) and word (16 bits).

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) to retain a data segment address. For details of DSR, see "nX-U8/100 Core Instruction Manual".

[Description of Bits]

- **DSR3-DSR0** (bits 3-0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Prohibited
0	0	1	0	Data segment 2
0	0	1	1	Prohibited
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Data segment 8
1	0	0	1	Prohibited
1	0	1	0	Data segment A
1	0	1	1	Prohibited
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Chapter 3

Reset Function

3 Reset Function

3.1 Overview

This LSI has the five reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

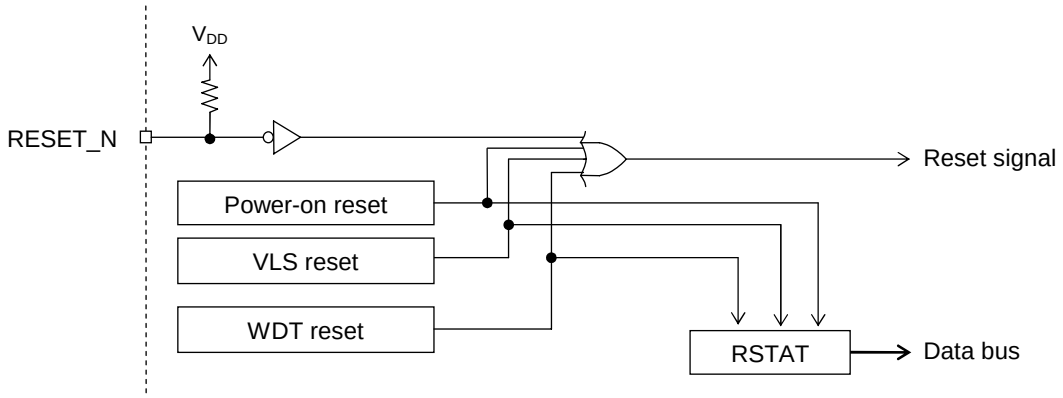
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by the voltage level supervisor (VLS)
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESET_N pin has an internal pull-up resistor
- 46.8ms, 62.5ms, 125ms, 250ms, 1sec, 4 sec, or 16sec can be selected as the watchdog timer (WDT) second overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT: Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined

3.2.2 Reset Status Register (RSTAT)

Address: 0F001H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	VLSR	—	—	WDTR	—	POR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	1

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]

- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

- **WDTR** (bit 2)
  The WDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

- **VLSR** (bit 5)
  The VLSR is a flag that indicates that the voltage level supervisor (VLS) reset is generated. This bit is set to "1" when the reset by the VLS is generated.

VLSR	Description
0	Voltage level supervisor (VLS) reset not occurred
1	Voltage level supervisor (VLS) reset occurred

Note:
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1 Operation of System Reset Mode

System reset has the highest priority among all the processing and any other processing being executed up to then is cancelled.
The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by the voltage level supervisor (VLS)
- Software reset by the BRK instruction (only the CPU is reset)

In system reset mode, the following processing is performed.

(1) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(2) CPU is initialized.

- All the registers in CPU are initialized.
- The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
- The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEEVL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 4

MCU Control Function

4 MCU Control Function

4.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

- System reset mode
- Program run mode
- HALT mode
- STOP mode

For system reset mode, see Chapter 3, "Reset Function".

This LSI has a block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies) to make even more reducing the current consumption.

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies).

4.1.2 Configuration

Figure 4-1 shows a CPU operating state transition diagram.

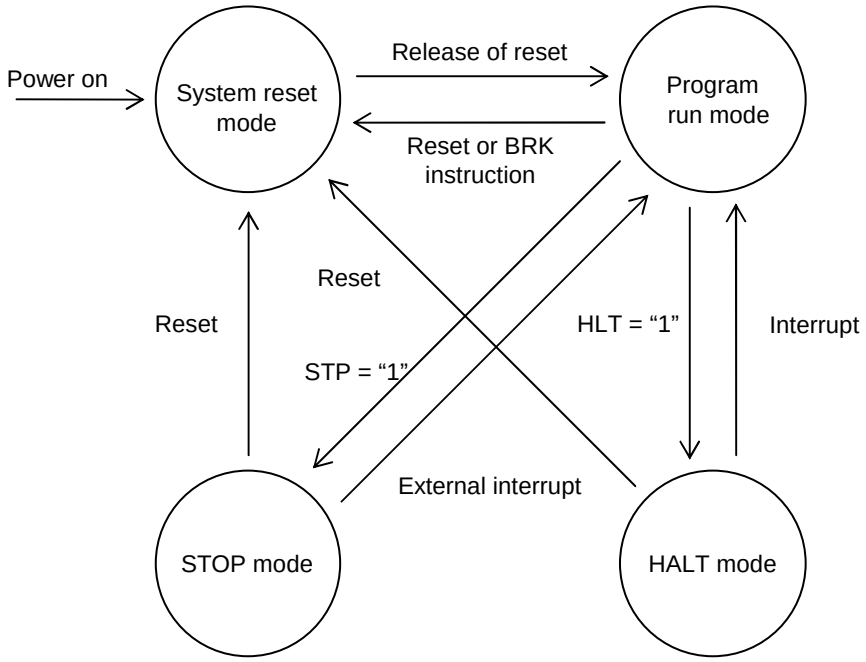


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	—	W	8	—
0F009H	Standby control register	SBYCON	—	W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	—	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	—	R/W	8	00H

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: — (Undefined)

	7	6	5	4	3	2	1	0
STPACP	—	—	—	—	—	—	—	—
R/W	W	W	W	W	W	W	W	W
Initial value	—	—	—	—	—	—	—	—

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH" (n: an arbitrary value) and "0AnH" (n: an arbitrary value), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".
During a system reset, the stop code acceptor is disabled.

Note:
The STOP code acceptor can not be enabled on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	—	—	—	—	—	—	STP	HLT
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

- **HLT** (bit 0)
  The HALT bit is used for setting a HALT mode. When the HALT bit is set to "1", the mode is changed to the HALT mode. When the WDT interrupt request, or enabled (the interrupt enable flag is "1") interrupt request is issued, the HALT bit is set to "1" and the mode is returned to program run mode.

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. When the interrupt request enabled by the interrupt enable register (IE0-IE7) is issued, the STP bit is set to "0" and the LSI returns to the program run mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Prohibited

Note:
The mode can not be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition). When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. Refer to the "nX-U8/100 Core Instruction Manual" for details of PSW.

4.2.4 Block Control Register 2 (BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C0	DI2C1	—	—	DUA1	DUA0	—	DSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DSIO0** (bit 0)
  DSIO0 controls the operation of Synchronous Serial Port 0.

DSIO0	Description
0	Enables the operation of Synchronous Serial Port 0 (initial value).
1	Disables the operation of Synchronous Serial Port 0.

- **DUA0** (bit 2)
  DUA0 controls the operation of UART0.

DUA0	Description
0	Enables the operation of UART0 (initial value).
1	Disables the operation of UART0.

- **DUA1** (bit 3)
  DUA1 controls the operation of UART1.

DUA1	Description
0	Enables the operation of UART1 (initial value).
1	Disables the operation of UART1.

- **DI2C1** (bit 6)
  DI2C1 controls the operation of I^2C bus Interface (Slave).

DI2C1	Description
0	Enables the operation of I^2C bus Interface (Slave) (initial value).
1	Disables the operation of I^2C bus Interface (Slave).

- **DI2C0** (bit 7)
  DI2C0 controls the operation of I^2C bus Interface (Master).

DI2C0	Description
0	Enables the operation of I^2C bus Interface (Master) (initial value).
1	Disables the operation of I^2C bus Interface (Master).

Note:
– If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
– Refer to Chapter 11, "Synchronous Serial Port" for details of the Synchronous Serial Port operation.
– Refer to Chapter 12, "UART" for details of the UART operation.
– Refer to Chapter 13, "I2C Bus Interface Master" for details of the I2C Bus Interface Master operation.
– Refer to Chapter 14, "I2C Bus Interface Slave" for details of the I2C Bus Interface Slave operation.

4.2.5 Block Control Register 4 (BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	—	—	—	—	—	—	—	DSAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DSAD** (bit 0)
  The DSAD bit is used to control SA type A/D converter operation. When the DSAD bit is set to "1", the circuits related to SA type A/D converter are reset and turned off.

DSAD	Description
0	Enables operating SA type A/D converter (initial value)
1	Disables operating SA type A/D converter

Note:
– If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
– Refer to Chapter 20, "Successive Approximation Type A/D Converter" for details of the successive approximation type A/D converter operation.

4.2.6 Block Control Register 6 (BLKCON6)

Address: 0F02EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON6	DTMF	DTME	—	—	DTMB	DTMA	DTM9	DTM8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON6 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DTM8** (bit 0)
  DTM8 controls the operation of the Timer8.

DTM8	Description
0	Enables the operation of the Timer8 (initial value).
1	Disables the operation of the Timer8.

- **DTM9** (bit 1)
  DTM9 controls the operation of the Timer9.

DTM9	Description
0	Enables the operation of the Timer9 (initial value).
1	Disables the operation of the Timer9.

- **DTMA** (bit 2)
  DTMA controls the operation of the TimerA.

DTMA	Description
0	Enables the operation of the TimerA (initial value).
1	Disables the operation of the TimerA.

- **DTMB** (bit 3)
  DTMB controls the operation of the TimerB.

DTMB	Description
0	Enables the operation of the TimerB (initial value).
1	Disables the operation of the TimerB.

- **DTME** (bit 6)
  DTME controls the operation of the TimerE.

DTME	Description
0	Enables the operation of the TimerE (initial value).
1	Disables the operation of the TimerE.

- **DTMF** (bit 7)
  DTMF controls the operation of the TimerF.

DTMF	Description
0	Enables the operation of the TimerF (initial value).
1	Disables the operation of the TimerF.

Note:

- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 8, "Timers" for details of the Timer operation.

4.2.7 Block Control Register 7 (BLKCON7)

Address: 0F02FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON7	—	—	—	—	DPWF	DPWE	DPWD	DPWC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON7 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DPWC** (bit 0)
  DPWC controls the operation of the PWMC.

DPWC	Description
0	Enables the operation of the PWMC (initial value).
1	Disables the operation of the PWMC.

- **DPWD** (bit 1)
  DPWD controls the operation of the PWMD.

DPWD	Description
0	Enables the operation of the PWMD (initial value).
1	Disables the operation of the PWMD.

- **DPWE** (bit 2)
  DPWE controls the operation of the PWME.

DPWE	Description
0	Enables the operation of the PWME (initial value).
1	Disables the operation of the PWME.

- **DPWF** (bit 3)
  DPWF controls the operation of the PWMF.

DPWF	Description
0	Enables the operation of the PWMF (initial value).
1	Disables the operation of the PWMF.

Note:
– If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
– Refer to Chapter 10, "PWM" for details of the Timer operation.

4.3 Description of Operation

4.3.1 Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, low level detection reset, VLS reset, or WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2 HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE0–IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK) and the HALT mode is returned to the program run mode released.
Figure 4-2 shows the operation waveforms in HALT mode.

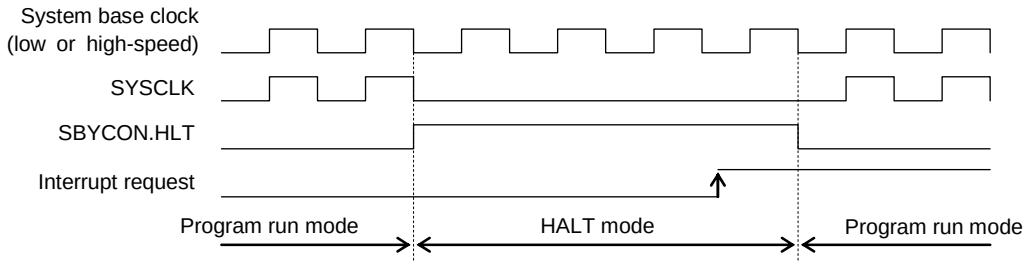


Figure 4-2 Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3 STOP Mode

The STOP mode is the state where low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by writing "5nH" (n: an arbitrary value) and "0AnH" (n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the stop code acceptor is disabled.
When a VLS interrupt request or an interrupt-enabled (the interrupt enable flag is "1") interrupt request is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 STOP Mode When CPU Operates with Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When interrupt-enabled (the interrupt enable flag is "1") interrupt request occurs, the STP bit is set to "0" and low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts after the low-speed clock was oscillating. When the high-speed clock was not oscillating before the STOP mode is entered, high-speed oscillation does not start.
When an interrupt request occurs, the STOP mode is released after counting low-speed clock (LSCLK) 32 times., the mode is returned to the program run mode, and the low-speed clock(LSCLK) restarts supply to the peripheral circuits. When the low-speed clock (LSCLK) restart, the high-speed clocks (OSCLK and HSCLK) restarts supply to the peripheral circuits after counting for stabilizing the clock oscillation (8192-pules count for PLL or 128-pulse count for External clock).
Figure 4-3 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.

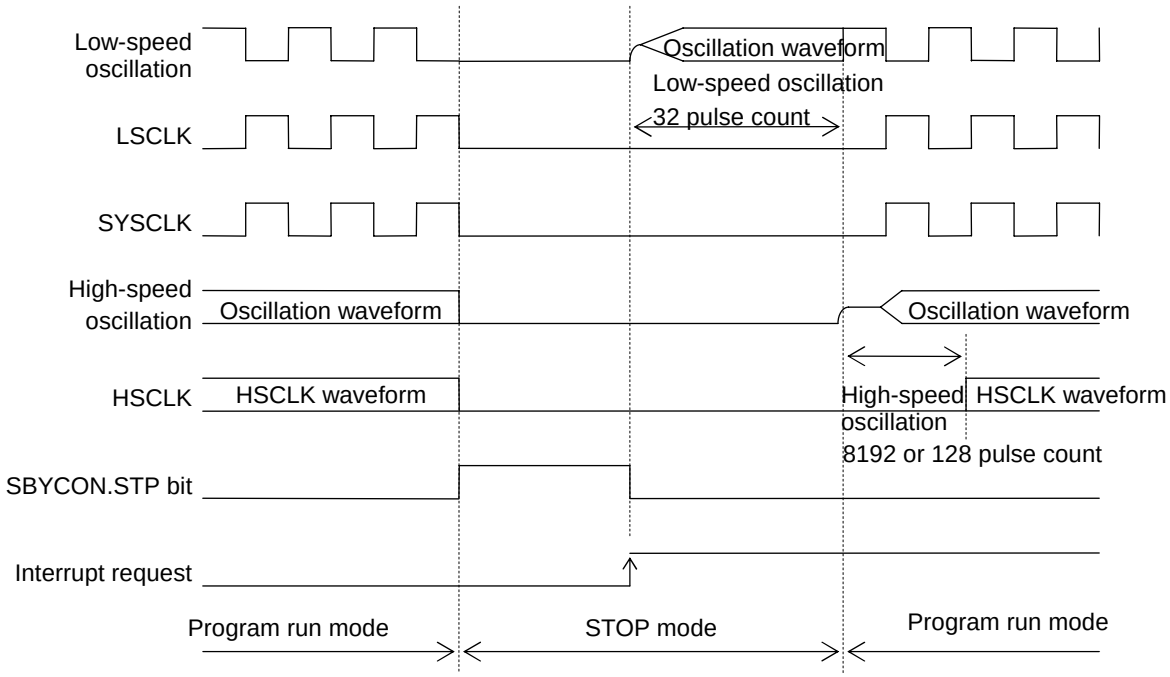


Figure 4-3 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.3.2 STOP Mode When CPU Operates with High-Speed Clock

When the CPU is operating with a high-speed clock and the STP bit of SBYCON is set to "1" with the stop code acceptor enabled, the STOP mode is entered and high-speed oscillation and low-speed oscillation stop.
When interrupt-enabled (the interrupt enable flag is "1") interrupt request occurs, the STP bit is set to "0" and the low-speed and high-speed oscillation restart.

When an interrupt request is issued, after counting the low-speed clock oscillation stabilization time (32-pulse count), the STOP mode is released after the elapse of the high-speed clock (OSCLK) oscillation stabilization time (8192-pulse count for PLL or 128-pulse count for External clock), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
The low-speed clock (LSCLK) restart supply to the peripheral circuit, after restarting the high-speed clocks (OSCLK and HSCLK).

Figure 4-4 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.

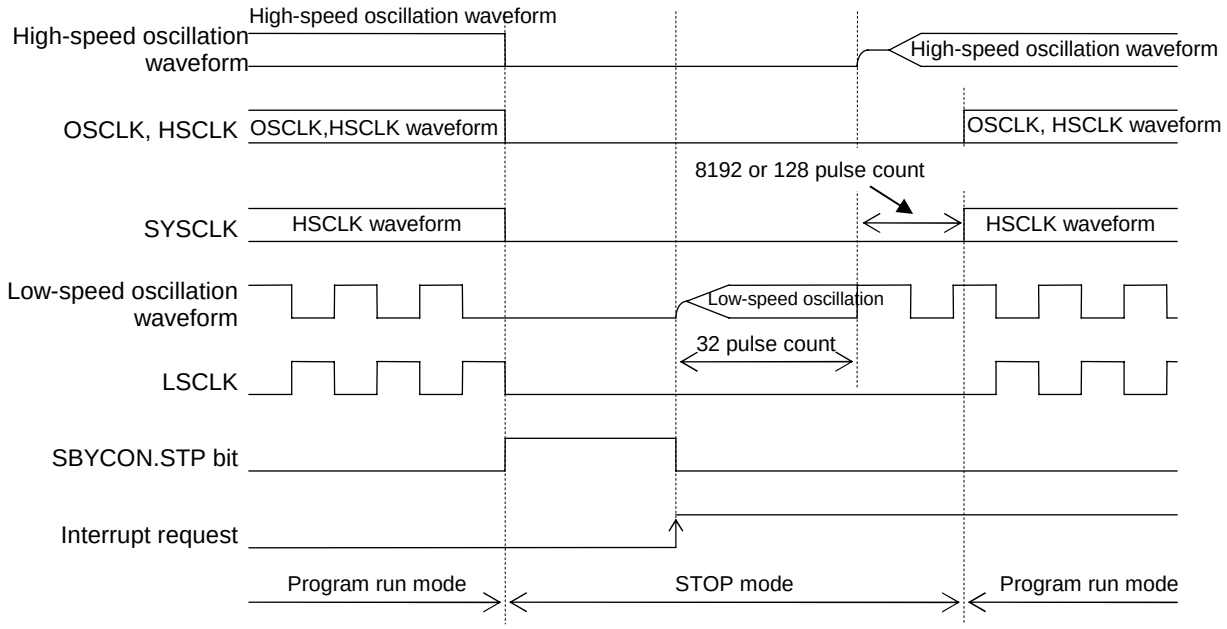


Figure 4-4 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
The STOP mode is entered two cycles after the instruction that sets the STP bit to "1" and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to "1".

4.3.3.3 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE7), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from STOP/HALT mode.

Table 4-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	–	0	Not returned from STOP/HALT mode.
3	*	–	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0, 1, 2	*	–	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	*	0	Not returned from STOP/HALT mode.
*	*	0	1	
*	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0, 1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Notes:
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither nonmaskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.4 Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.

When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

BLKCON2 register controls (enables or disables) the operation of Synchronous Serial Port, UART0, UART1, and I2C.
BLKCON4 register controls (enables or disables) the operation of SA type A/D converter.
BLKCON6 register controls (enables or disables) the operation of Timer8, Timer9, TimerA, TimerB, TimerE and TimerF.
BLKCON7 register controls (enables or disables) the operation of PWMC, PWMD, PWME and PWMF.

Note:
– If the appropriate bit of the block register is set to "1", all relevant registers are initialized.
– Refer to the relevant chapter for details of operation or notes of each block.

Chapter 5

Interrupts (INTs)

5 Interrupts (INTs)

5.1 Overview

This LSI has 31 interrupt sources (External interrupts: 7 sources, Internal interrupts: 24 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 7, "Time Base Counter"
Chapter 8, "Timers"
Chapter 9, "Watchdog Timer"
Chapter 10, "PWM"
Chapter 11, "Synchronous Serial Port"
Chapter 12, "UART"
Chapter 13, "I^2C Bus Interface (Master)"
Chapter 14, "I^2C Bus Interface (Slave)"
Chapter 15, "PortA"
Chapter 16, "PortB"
Chapter 19, "PortAB Interrupts"
Chapter 20, "Successive Approximation Type A/D Converter"
Chapter 21, "Voltage Level Supervisor"
Chapter 22, "Analog Comparator"

5.1.1 Features

- 1 non-maskable interrupt sources (Internal source)
- 30 maskable interrupt sources (Internal sources: 23, External sources: 7)
- Software interrupt (SWI): 64 sources max.
- External interrupts and Analog Comparator interrupts allow edge selection and sampling selection.

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H

5.2.2 Interrupt Enable Register 0 (IE0)

Address: 0F010H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE0	—	EVLS	—	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE0 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE0 is not reset.

[Description of Bits]

- **EVLS** (bit 6)
  EVLS is the enable flag for the voltage level supervisor interrupt (VLSINT).

EVLS	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	EPB3	EPB2	EPB1	EPB0	—	EPA2	EPA1	EPA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **EPA0** (bit 0)
  EPA0 is the enable flag for the input/output port PA0 pin interrupt (PA0INT).

EPA0	Description
0	Disabled (initial value)
1	Enabled

- **EPA1** (bit 1)
  EPA1 is the enable flag for the input/output port PA1 pin interrupt (PA1INT).

EPA1	Description
0	Disabled (initial value)
1	Enabled

- **EPA2** (bit 2)
  EPA2 is the enable flag for the input/output port PA2 pin interrupt (PA2INT).

EPA2	Description
0	Disabled (initial value)
1	Enabled

- **EPB0** (bit 4)
  EPB0 is the enable flag for the input/output port PB0 pin interrupt (PB0INT).

EPB0	Description
0	Disabled (initial value)
1	Enabled

- **EPB1** (bit 5)
  EPB1 is the enable flag for the input/output port PB1 pin interrupt (PB1INT).

EPB1	Description
0	Disabled (initial value)
1	Enabled

- **EPB2** (bit 6)
  EPB2 is the enable flag for the input/output port PB2 pin interrupt (PB2INT).

EPB2	Description
0	Disabled (initial value)
1	Enabled

- **EPB3** (bit 7)
  EPB3 is the enable flag for the input/output port PB3 pin interrupt (PB3INT).

EPB3	Description
0	Disabled (initial value)
1	Enabled

5.2.4 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	EI2CM	EI2CS	—	—	—	ESAD	—	ESIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]

- **ESIO0** (bit 0)
  ESIO0 is the enable flag for the synchronous serial port0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

- **ESAD** (bit 2)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

- **EI2CS** (bit 6)
  EI2CS is the enable flag for the I^2C bus interface (slave) interrupt (I2CSINT).

EI2CS	Description
0	Disabled (initial value)
1	Enabled

- **EI2CM** (bit 7)
  EI2CM is the enable flag for the I^2C bus interface (master) interrupt (I2CMINT).

EI2CM	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	—	—	—	—	ETM9	ETM8	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

[Description of Bits]

- **ETM8** (bit 2)
  ETM8 is the enable flag for the timer 8 interrupt (TM8INT).

ETM8	Description
0	Disabled (initial value)
1	Enabled

- **ETM9** (bit 3)
  ETM9 is the enable flag for the timer 9 interrupt (TM9INT).

ETM9	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	ECMP1	ECMP0	—	—	—	—	EUA1	EUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **EUA1** (bit 1)
  EUA1 is the enable flag for the UART1 interrupt (UA1INT).

EUA1	Description
0	Disabled (initial value)
1	Enabled

- **ECMP0** (bit 6)
  ECMP0 is the enable flag for the comparator0 interrupt (CMP0INT).

ECMP0	Description
0	Disabled (initial value)
1	Enabled

- **ECMP1** (bit 7)
  ECMP1 is the enable flag for the comparator1 interrupt (CMP1INT).

ECMP1	Description
0	Disabled (initial value)
1	Enabled

5.2.7 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	ETMB	ETMA	ETMF	ETME	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

- **ETME** (bit 4)
  ETME the enable flag for the timer E interrupt (TMEINT).

ETME	Description
0	Disabled (initial value)
1	Enabled

- **ETMF** (bit 5)
  ETMF the enable flag for the timer F interrupt (TMFINT)

ETMF	Description
0	Disabled (initial value)
1	Enabled

- **ETMA** (bit 6)
  ETMA the enable flag for the timer A interrupt (TMAINT).

ETMA	Description
0	Disabled (initial value)
1	Enabled

- **ETMB** (bit 7)
  ETMB the enable flag for the timer B interrupt (TMBINT)

ETMB	Description
0	Disabled (initial value)
1	Enabled

5.2.8 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	E32H	—	E128H	—	EPWF	EPWE	EPWD	EPWC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

- **EPWC** (bit 0)
  EPWC is the enable flag for the PWMC interrupt (PWCINT)

EPWC	Description
0	Disabled (initial value)
1	Enabled

- **EPWD** (bit 1)
  EPWD is the enable flag for the PWMD interrupt (PWDINT)

EPWD	Description
0	Disabled (initial value)
1	Enabled

- **EPWE** (**bit** 2)
  EPWE is the enable flag for the PWME interrupt (PWEINT)

EPWE	Description
0	Disabled (initial value)
1	Enabled

- **EPWF** (bit 3)
  EPWF is the enable flag for the PWMF interrupt (PWFINT)

EPWF	Description
0	Disabled (initial value)
1	Enabled

- **E128H** (bit 5)
  E128H is the enable flag for the time base counter 128 Hz interrupt (T128HINT).

E128H	Description
0	Disabled (initial value)
1	Enabled

- **E32H** (bit 7)
  E32H is the enable flag for the time base counter 32 Hz interrupt (T32HINT).

E32H	Description
0	Disabled (initial value)
1	Enabled

5.2.9 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	—	—	—	—	E2H	—	—	E16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]

- **E16H** (bit 0)
  E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

- **E2H** (bit 3)
  E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

5.2.10 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	—	QVLS	—	—	—	—	—	QWDT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

- **QVLS** (bit 6)
  QVLS is the request flag for the volage level supervisor interrupt (VLSINT)

QVLS	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	QPB3	QPB2	QPB1	QPB0	—	QPA2	QPA1	QPA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPA0** (bit 0)
  QPA0 is the request flag for the input port PA0 pin interrupt (PA0INT).

QPA0	Description
0	No request (initial value)
1	Request

- **QPA1** (bit 1)
  QPA1 is the request flag for the input port PA1 pin interrupt (PA1INT).

QPA1	Description
0	No request (initial value)
1	Request

- **QPA2** (bit 2)
  QPA2 is the request flag for the input port PA2 pin interrupt (PA2INT).

QPA2	Description
0	No request (initial value)
1	Request

- **QPB0** (bit 4)
  QPB0 is the request flag for the input port PB0 pin interrupt (PB0INT).

QPB0	Description
0	No request (initial value)
1	Request

- **QPB1** (bit 5)
  QPB1 is the request flag for the input port PB1 pin interrupt (PB1INT).

QPB1	Description
0	No request (initial value)
1	Request

- **QPB2** (bit 6)
  QPB2 is the request flag for the input port PB2 pin interrupt (PB2INT).

QPB2	Description
0	No request (initial value)
1	Request

- **QPB3** (bit 7)
  QPB3 is the request flag for the input port PB3 pin interrupt (PB3INT).

QPB3	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.12 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	QI2CM	QI2CS	—	—	—	QSAD	—	QSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QSIO0** (bit 0)
  QSIO0 is the request flag for the synchronous serial port0 interrupt (SIO0INT)

QSIO0	Description
0	No request (initial value)
1	Request

- **QSAD** (bit 2)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT)

QSAD	Description
0	No request (initial value)
1	Request

- **QI2CS** (bit 6)
  QI2CS is the request flag for the I^2C bus interface (slave) interrupt (I2CSINT)

QI2CS	Description
0	No request (initial value)
1	Request

- **QI2CM** (bit 7)
  QI2CM is the request flag for the I^2C bus interface (master) interrupt (I2CMINT)

QI2CM	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	—	—	—	—	QTM9	QTM8	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTM8** (bit 2)
  QTM8 is the request flag for the timer 8 interrupt (TM8INT).

QTM8	Description
0	No request (initial value)
1	Request

- **QTM9** (bit 3)
  QTM9 is the request flag for the timer 9 interrupt (TM9INT).

QTM9	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	QCMP1	QCMP0	—	—	—	—	QUA1	QUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QUA1** (bit 1)
  QUA1 is the request flag for the UART1 interrupt (UA1INT).

QUA1	Description
0	No request (initial value)
1	Request

- **QCMP0** (bit 6)
  QCMP0 is the request flag for comparator0 interrupt (CMP0INT).

QCMP0	Description
0	No request (initial value)
1	Request

- **QCMP1** (bit 7)
  QCMP1 is the request flag for comparator1 interrupt (CMP1INT).

QCMP1	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.15 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	QTMB	QTMA	QTMF	QTME	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTME** (bit 4)
  QTME is the request flag for the timer E interrupt (TMEINT).

QTME	Description
0	No request (initial value)
1	Request

- **QTMF** (bit 5)
  QTMF is the request flag for the timer F interrupt (TMFINT).

QTMF	Description
0	No request (initial value)
1	Request

- **QTMA** (bit 6)
  QTMA is the request flag for the timer A interrupt (TMAINT).

QTMA	Description
0	No request (initial value)
1	Request

- **QTMB** (bit 7)
  QTMB is the request flag for the timer B interrupt (TMBINT).

QTMB	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.16 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	—	Q128H	—	QPWF	QPWE	QPWD	QPWC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPWC** (bit 0)
  QPWC is the request flag for the PWMC interrupt (PWCINT).

QPWC	Description
0	No request (initial value)
1	Request

- **QPWD** (bit 1)
  QPWD is the request flag for the PWMD interrupt (PWDINT).

QPWD	Description
0	No request (initial value)
1	Request

- **QPWE** (bit 2)
  QPWE is the request flag for the PWME interrupt (PWEINT).

QPWE	Description
0	No request (initial value)
1	Request

- **QPWF** (bit 3)
  QPWF is the request flag for the PWMF interrupt (PWFCINT).

QPWF	Description
0	No request (initial value)
1	Request

- **Q128H** (bit 5)
  Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

- **Q32H** (bit 7)

  Q32H is the request flag for the time base counter 32 Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.17 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	—	—	—	—	Q2H	—	—	Q16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **Q16H** (bit 0)
  Q16H is the request flag for the time base counter 16 Hz interrupt (T16HINT).

Q16H	Description
0	No request (initial value)
1	Request

- **Q2H** (bit 3)
  Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the instruction to write to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the the interrupt shift cycle starts after the next 1 instruction is executed.

5.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT), interrupt enable/disable for 30 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to 7). WDTINT is non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-1 Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
3	Voltage level supervisor interrupt	VLSINT	000CH
5	PA0 interrupt	PA0INT	0010H
6	PA1 interrupt	PA1INT	0012H
7	PA2 interrupt	PA2INT	0014H
9	PB0 interrupt	PB0INT	0018H
10	PB1 interrupt	PB1INT	001AH
11	PB2 interrupt	PB2INT	001CH
12	PB3 interrupt	PB3INT	001EH
13	Synchronous Serial Port0 interrupt	SIO0INT	0020H
15	Successive approximation type A/D converter interrupt	SADINT	0024H
19	I^2C Bus Interface (Slave) interrupt	I2CSINT	002CH
20	I^2C Bus Interface (Master) interrupt	I2CMINT	002EH
23	Timer 8 interrupt	TM8INT	0034H
24	Timer 9 interrupt	TM9INT	0036H
29	UART 0 interrupt	UA0INT	0040H
30	UART 1 interrupt	UA1INT	0042H
35	Comparator interrupt0	CMP0INT	004CH
36	Comparator interrupt1	CMP1INT	004EH
41	Timer E interrupt	TMEINT	0058H
42	Timer F interrupt	TMFINT	005AH
43	Timer A interrupt	TMAINT	005CH
44	Timer B interrupt	TMBINT	005EH
45	PWMC interrupt	PWCINT	0060H
46	PWMD interrupt	PWDINT	0062H
47	PWME interrupt	PWEINT	0064H
48	PWMF interrupt	PWFINT	0066H
50	TBC128Hz interrupt	T128HINT	006AH
52	TBC32Hz interrupt	T32HINT	006EH
53	TBC16Hz interrupt	T16HINT	0070H
56	TBC2Hz interrupt	T2HINT	0076H

Note:
- When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
- Please define vector tables for all unused interrupts for fail safe.

5.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW toEPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to"1".
(6) Load the interrupt start address into PC.

5.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2.
(2) Transfer CSR to ECSR2.
(3) Transfer PSW to EPSW2.
(4) Set the ELEVEL field to "2".
(5) Load the interrupt start address into PC.

5.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW to EPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to "1".
(6) Load the interrupt start address into PC.

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

State A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: State A-1-1

```
Intrpt_A-1-1;          ; A-1-1 state
   DI                  ; Disable interrupt
    :
    :
    :
   RTI                 ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: State A-1-2

```
Intrpt_A-1-2;          ; Start
   PUSH ELR, EPSW      ; Save ELR and EPSW at the
                         beginning
   EI                  ; Enable interrupt
    :
    :
    :
    :
    :
   POP PC, PSW         ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

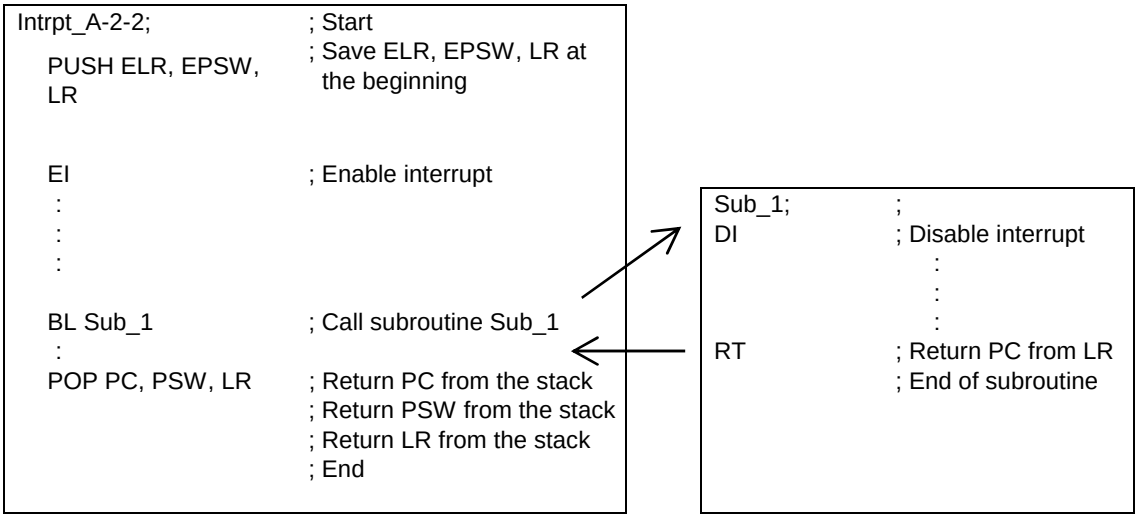
A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: A-2-2



State B: Non-maskable interrupt is being processed

B-1: When a subroutine is not called

- Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to PC and those of the EPSW register to PSW.

B-2: When a subroutine is called

B-2-1: When a subroutine is not called for an interruption routine to a run time by a program

- Processing immediately after the start of interrupt routine execution
  "PUSH ELR, EPSW" are specified and the return address of an interruption and the status of EPSW are evacuated to a stack.
- Processing at the end of interrupt routine execution
  Specifying "POP PC, PSW" instead of a RTI supervisor call, the save data of EPSW returns the save data of the return address of an interruption to PC at PSW. B-2-2: When a subroutine is called for an interruption routine to a run time by a program
- Processing immediately after the start of interrupt routine execution
  "PUSH LR, ELR, EPSW" are specified and the return address of an interruption, the return address of a subroutine, and the status of EPSW are evacuated to a stack.
- Processing at the end of interrupt routine execution
  Specifying "POP PC, PSW, LR" instead of a RTI supervisor call, as for the save data of the return address of an interruption, the save data of EPSW returns the save data of LR to LR to PC to PSW.

Example of description: State B-1

```
Intrpt_B-1;          ; B-1 state
   RTI               ; Return PC from ELR
                     ; Return PSW form EPSW
                     ; End
```

Example of description: State B-2-1

```
Intrpt_B-2-2;        ; Start
   PUSH ELR, EPSW    ; Save ELR and EPSW at the
                       beginning
   :
   :
   :
   POP PC, PSW       ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2;        ; Start
   PUSH ELR, EPSW,   ; Save ELR, EPSW, LR at
   LR                  the beginning
   :
   :
   :
   BL Sub_1          ; Call subroutine Sub_1
   :
   POP PC, PSW, LR   ; Return PC from the stack
                     ; Return PSW from the
                     stack
```

```
Sub_1;
                     :
                     :
                     :
RT                   ; Return PC from LR
                     ; End of subroutine
```

5.3.5 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

Reference:
For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Chapter 6

Clock Generation Circuit

6 Clock Generation Circuit

6.1 Overview

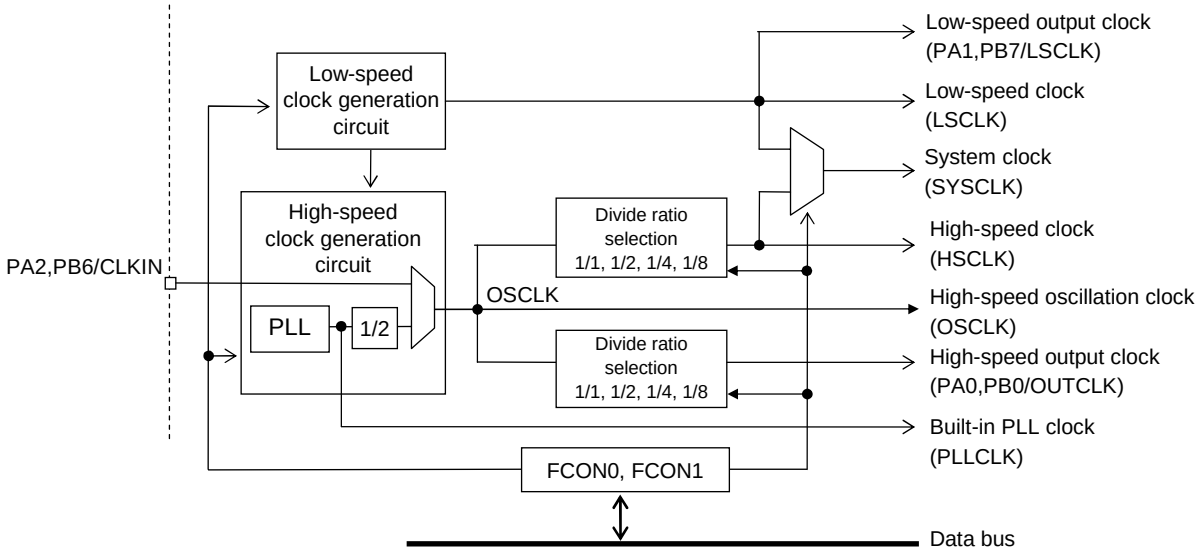
The clock generation circuit generates and provides a low-speed clock (LSCLK), high-speed clock (HSCLK), built-in PLL clock (PLLCLK), high-speed oscillation clock (OSCLK), system clock (SYSCLK), low-speed output clock (LSCLK), and high-speed output clock (OUTCLK). LSCLK, and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and LSCLK/OUTCLK is a clock that is output from a port.
For the LSCLK and OUTCLK output port, see Chapter 15, "Port A" and Chapter 16, "Port B".
Additionally, for the STOP mode described in this chapter, see Chapter 4, "MCU Control Function".

6.1.1 Features

- Low-speed clock generation circuit:
  – Built-in RC oscillation (32.768kHz) mode
- High-speed clock generation circuit: Software selection
  – Built-in PLL oscillation mode
  – External clock input mode

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1

Figure 6-1 Configuration of Clock Generation Circuit

Note:
This LSI starts operation with the 32.768kHz RC oscillation clock after power-on or a system reset. At initialization by software, set the FCON0, FCON1 register to switch the clock to a required one.

6.1.3 List of Pins

Pin name	I/O	Description
PA0/OUTCLK	O	High-speed clock output pin Used for the tertiary function of the PA0 pin
PB0/OUTCLK	O	High-speed clock output pin Used for the tertiary function of the PB0 pin
PA2/CLKIN	I	External clock input pin Used for the tertiary function of the PA2 pin
PB6/CLKIN	I	External clock input pin Used for the secondary function of the PB6 pin
PA1/LSCLK	O	Low-speed clock output pin Used for the tertiary function of the PA1 pin
PB7/LSCLK	O	Low-speed clock output pin Used for the secondary function of the PB7 pin

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	00H

6.2.2 Frequency Control Register 0 (FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bits
Initial value: 3BH

	7	6	5	4	3	2	1	0
FCON0	—	—	OUTC1	OUTC0	OSCM1	OSCM0	SYSC1	SYSC0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	1	1	1	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.
OSCM1 always returns the value "1".

[Description of Bits]

- **SYSC1, SYSC0** (bits 1, 0)

The SYSC1 and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits (including high-speed time base counter). OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected. The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 8.192MHz.
At system reset, 1/8OSCLK is selected.

SYSC1	SYSC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

- **OSCM1, OSCM0** (bits 3, 2)

The OSCM1 and OSCM0 bits are used to select the mode of the high-speed clock generation circuit. PLL oscillation mode, or external clock input mode can be selected.
The setting of OSCM0 can be changed only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0").
At system reset, PLL oscillation mode is selected.

OSCM1	OSCM0	Description
1	0	Built-in PLL oscillation mode (initial value)
1	1	External clock input mode (PA2,PB6/CLKIN)

- **OUTC1, OUTC0** (bits 5, 4)

The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the tertiary function of PA0 pin, PB0 pin are used.
OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	OSCLK
0	1	1/2 OSCLK
1	0	1/4 OSCLK
1	1	1/8 OSCLK (initial value)

Note:
– To switch the mode of the high-speed clock generation circuit using the OSCM1 and OSCM0 bits, stop the high-speed oscillation and set the system clock to the low-speed clock (set the ENOSC bit and SYSCLK of FCON1 to "0").
– In external clock mode, an external clock is input from the PA2/CLKIN, PB6/CLKIN pin. And in external clock mode, input a clock that does not exceed 8.192 MHz.
– In external clock mode, when using PA2/CLKIN and PB6/CLKIN as external clock input pin, PA2/CLKIN has the higher priority.

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FCON1	LPLL	—	—	—	—	—	ENOSC	SYSCLK
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSCLK** (bit 0)

  The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 1, 2, 4, 8) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK (initial value)
1	HSCLK

- **ENOSC** (bit 1)

  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator.

ENOSC	Description
0	Disables high-speed oscillation (initial value)
1	Enables high-speed oscillation

- **LPLL** (bit 7)

  The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
  When the LPLL bit is set to "1", this indicates that the PLL oscillation frequency is locked within 16.384 MHz±1.0%.
  When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillation frequency is not within 16.384 MHz±1.0%.
  LPLL is a read-only bit.

LPLL	Description
0	Disables the use of PLL oscillation (initial value)
1	Enables the use of PLL oscillation

Note:
– LPLL flag is a reference flag. The oscillation stabilization time for 3ms (max) is required after PLL oscillation starting.
– Although the oscillated frequency of PLL is 16.384MHz, a CPU clock is a maximum of 8.192MHz.

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Clock Generation Circuit (built-in RC oscillating circuit)

Figure 6-2 shows the circuit configuration of the low-speed clock generation circuit.
The 32.768kHz RC oscillation clock generation circuit is activated by the occurrence of power ON reset or port reset or WDT reset or VLS reset. In starting by reset, after waiting oscillation stable time (256 counts), the clock is supplied to the peripheral circuit. In the return from a STOP mode, after waiting oscillation stable time(32 coounts), a clock is supplied to a peripheral circuit.

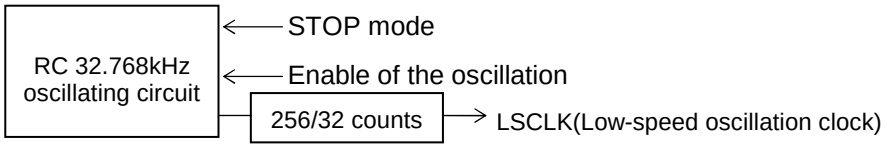


Figure 6-2 Circuit Configuration of RC 32.768 kHz Oscillation Mode

6.3.1.2 Operation of Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power-on reset.
The low-speed clock (LSCLK) is supplied to the peripheral circuits after a lapse of the low-speed clock oscillation stabilization period (256 counts) after power-on.
When the low-speed clock generation circuit shifts to STOP mode by software, it stops oscillation. It resumes oscillation when the STOP mode is released by an external interrupt. Then, LSCLK is supplied to the peripheral circuits after a lapse of the low-speed clock oscillation stabilization period (32 counts). For STOP mode, see Chapter 4, "MCU Control Function".
Figure 6-3 shows the waveforms of the low-speed clock generation circuit.

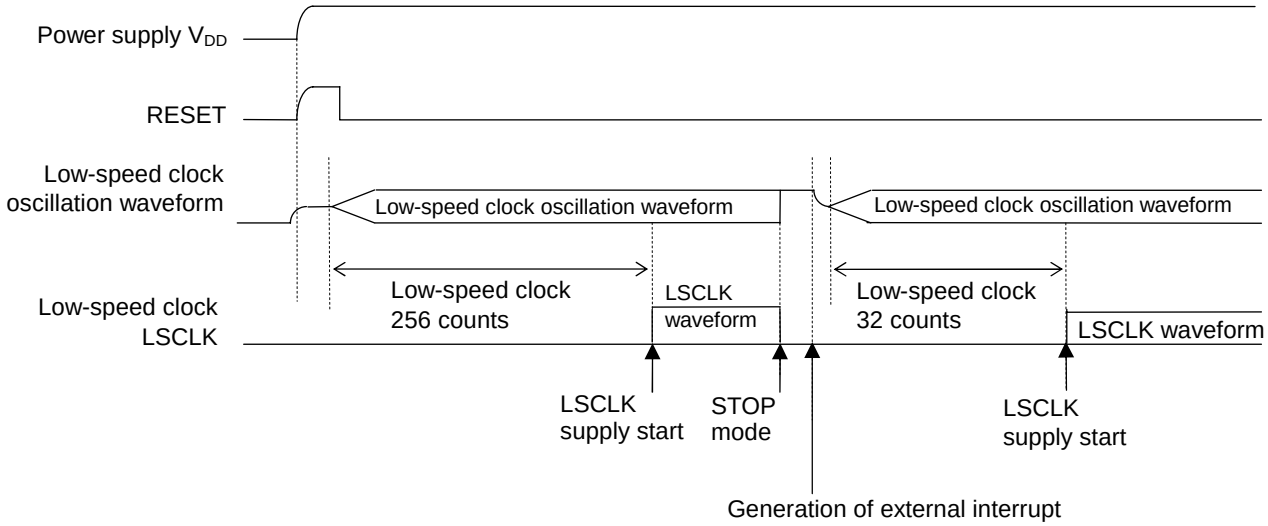


Figure 6-3 Operation of Low-Speed Clock Generation Circuit

Note:
After the power supply is turned on, CPU starts operation with a low-speed clock (RC 32.768kHz oscillation).

6.3.2 High-Speed Clock

For the high-speed clock generation circuit, built-in PLL oscillation mode or external clock input mode can be selected by the OSCM1 bit and OSCM0 bit of the frequecy control register0 (FCON0).

6.3.2.1 Built-in PLL Oscillation Mode

The PLL oscillation circuit generates the PLLCLK, which is a clock of 16.384 MHz (= 32.768 kHz × 500).
And the clock generated by dividing the PLLCLK by 2, which is used as high-speed oscillation clock (OSCLK).
When the frequency of a PLL oscillation clock is less than 16.384MHz ± 1.0%, the LPLL flag of FCON1 is set to "1."
In built-in PLL oscillation mode (OSCM0 = "0", OSCM1 = "1"), supply of OSCLK (high-speed oscillation clock) is started when the clock pulse, which is generated by dividing the PLLCLK by 2 count reaches 8192 after oscillation is enabled (ENOSC is set to "1").
In built-in PLL oscillation mode, both the PA2,PB6/CLKIN pin can be used as general-purpose input ports.
Figure 6-4 shows the circuit configuration in PLL oscillation mode.

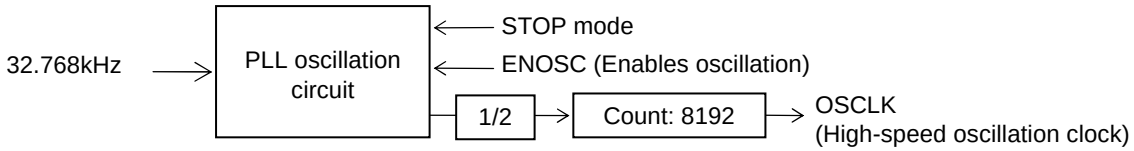


Figure 6-4 Circuit Configuration in PLL Oscillation Mode

6.3.2.2 High-Speed External Clock Input Mode

In high-speed external clock input mode, an external clock is input from the PA2 or PB6/CLKIN pin.
When set as external clock input mode(OSCM0="1", OSCM1="1"), supply of OSCLK is started after permitting an oscillation(ENOSC is set to "1.") and counting an external input clock 128 times.
Figure 6-5 shows the circuit configuration in high-speed external clock input mode.

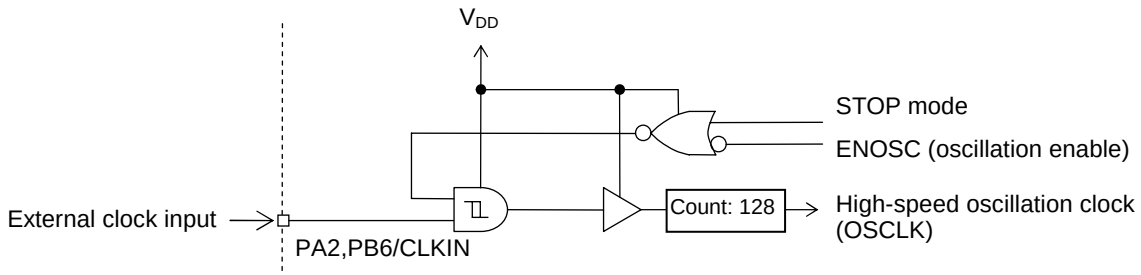


Figure 6-5 Circuit Configuration in High-Speed External Clock Input Mode

Notes:
- If the PA2,PB6/CLKIN pin is left open in high-speed external clock input mode, excessive current can flow. Therefore, be sure to input a "H" level (V_{DD}) or a "L" level (V_{SS}) to the CLKIN pin.
- The clock that is input must not exceed 8.192 MHz, the guaranteed maximum operating frequency of the system clock (SYSCLK) of this LSI.
- In external clock input mode, priority is given to PA2 when both PA2 and PB6 are set as a clock input pin

6.3.2.3 Operation of High-Speed Clock Generation Circuit

For the high-speed clock generation circuit, starting/stopping oscillation can be controlled by the frequency control register 0,1 (FCON0,1).

After selecting high-speed oscillation mode and its frequency in FCON0, the oscillation will be started if the ENOSC bit of FCON1 is set to "1." After an oscillation start, after waiting the oscillation stabilization period of a high-speed oscillation clock(OSCLK) in each mode, HSCLK begins to be supplied to a peripheral circuit.

The high-speed clock generation circuit stops oscillation when it enters STOP mode by software. When a STOP mode is canceled by external interruption and an oscillation restarts, after waiting the oscillation stabilization period of a low-speed oscillation(LSCLK) and a high-speed oscillation(OSCLK) clock in each mode, HSCLK begins to be supplied to a peripheral circuit. The oscillation stabilization period is the duration of 128 clock pulses in high-speed external clock input mode and the duration of 8192 clock pulses in PLL oscillation mode.

Figure 6-6 shows the waveforms of the high-speed clock generation circuit in bult-in PLL oscillation mode.

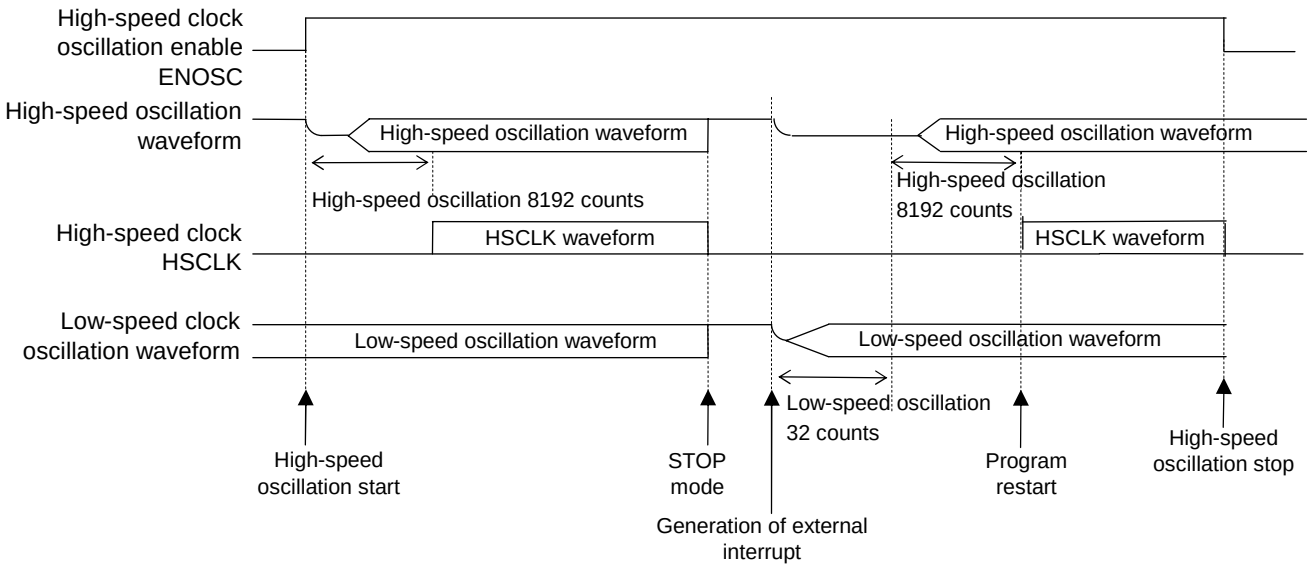


Figure 6-6 Operation of the High-Speed Clock Generation Circuit in bult-in PLL Oscillation Mode

6.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-7 shows a flow of system clock switching processing (HSCLK→LSCLK) and Figure 6-8 shows a flow of system clock switching processing (LSCLK→HSCLK).

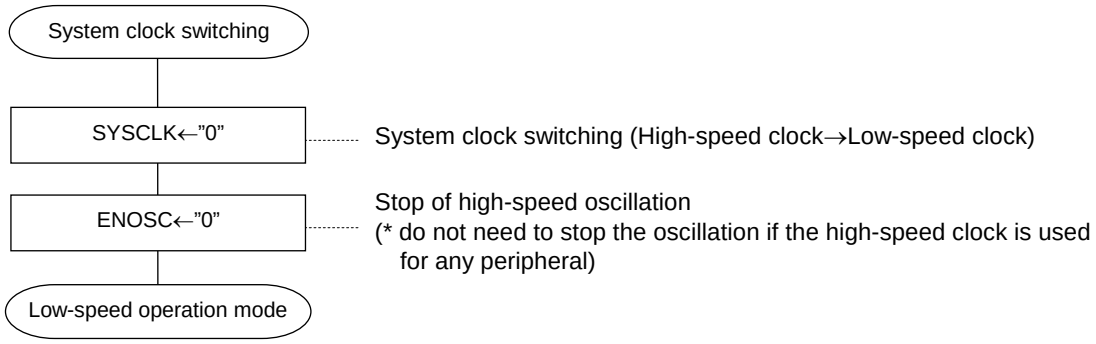


Figure 6-7 Flow of System Clock Switching Processing (HSCLK→LSCLK)

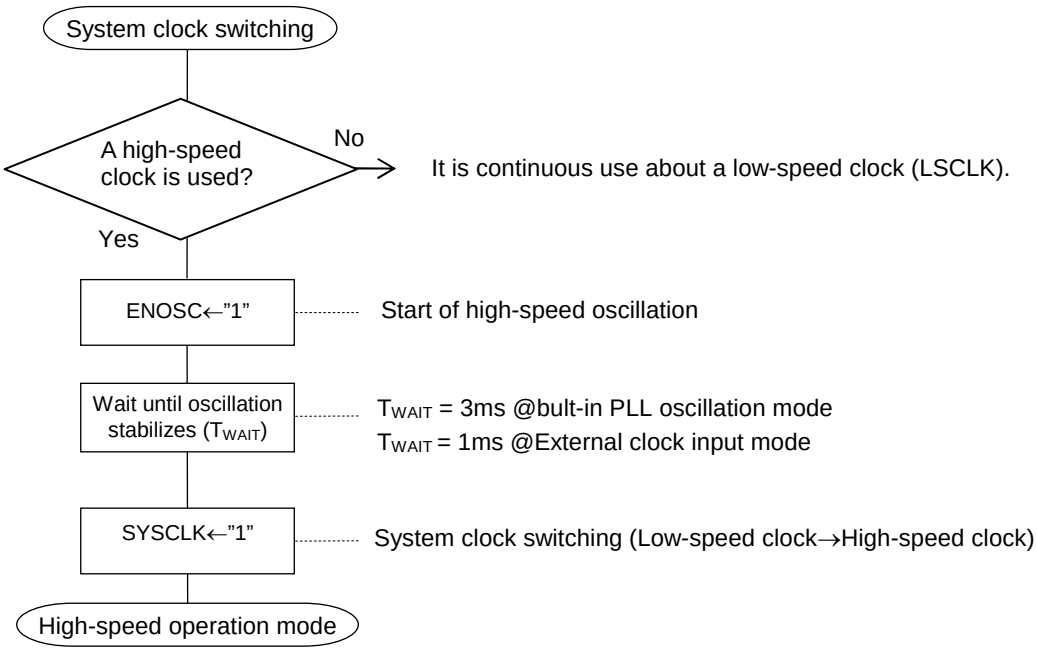


Figure 6-8 Flow of System Clock Switching Processing (LSCLK→HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Specifying port registers

For enable a clock output function, each related port register needs to be set up. Refer to the Chapter 15, "Port A" and the Chapter 16 "Port B" for details of each register.

6.4.1 Functioning PB7 (LSCLK) as the low speed clock output

Set PB7MD0 bit (bit7 of PBMOD0 register) to "1" for specifying the low speed clock output as the secondary function of PB7.

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	**0**	*	*	*	*	*	*	*

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	**1**	*	*	*	*	*	*	*

Set PB7C1 bit (bit7 of PBCON1 register) to "1" and set PB7C0 bit(bit7 of PBCON0 register) to "1", and set PB7DIR bit(bit7 of PBDIR register) to "0"for specifying the PB7 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C1**	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7DIR**	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	**0**	*	*	*	*	*	*	*

Data of PB7D bit (bit7 of PBD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
Data	******	*	*	*	*	*	*	*

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

6.4.2 Functioning PB0 (OUTCLK) as the High speed clock output

Set PB0MD1 bit (bit0 of PBMOD1 register) to "1" for specifying the low speed clock output as the tertiary function of PB0.

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	**PB0MD1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	**PB0MD0**
Data	*	*	*	*	*	*	*	**0**

Set PB0C1 bit (bit0 of PBCON1 register) to "1" and set PB0C0 bit(bit0 of PBCON0 register) to "1", and set PB0DIR bit(bit0 of PBDIR register) to "0"for specifying the PB0 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	**PB0C1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	**PB0C0**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	**PB0DIR**
Data	*	*	*	*	*	*	*	**0**

Data of PB0D bit (bit0 of PBD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	**PB0D**
Data	*	*	*	*	*	*	*	******

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

6.4.3 Functioning PA2 (CLKIN) as the External clock input

Set PA2MD1 bit (bit2 of PAMOD1 register) to "1" as the tertiary function of PA2.

Reg. name	PAMOD1 register (Address: 0F255H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2MD1**	PA1MD1	PA0MD1
Data	—	—	—	—	—	**1**	*	*

Reg. name	PAMOD0 register (Address: 0F254H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2MD0**	PA1MD0	PA0MD0
Data	—	—	—	—	—	**0**	*	*

Set PA2C1 bit (bit2 of PACON1 register) to "0" and set PA2C0 bit(bit2 of PACON0 register) to "0", and set PA2DIR bit(bit2 of PADIR register) to "1"for specifying the PA2 as input.

Reg. name	PACON1 register (Address: 0F253H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2C1**	PA1C1	PA0C1
Data	—	—	—	—	—	**0**	*	*

Reg. name	PACON0 register (Address: 0F252H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2C0**	PA1C0	PA0C0
Data	—	—	—	—	—	**0**	*	*

Reg. name	PADIR register (Address: 0F251H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2DIR**	PA1DIR	PA0DIR
Data	—	—	—	—	—	**1**	*	*

Data of PA2D bit (bit2 of PAD register) does not affect to the External clock input function, so don't care the data for the function.

Reg. name	PAD register (Address: 0F250H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	—	—	—	—	—	**PA2D**	PA1D	PA0D
Data	—	—	—	—	—	******	*	*

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

Chapter 7

Time Base Counter

7 Time Base Counter

7.1 Overview

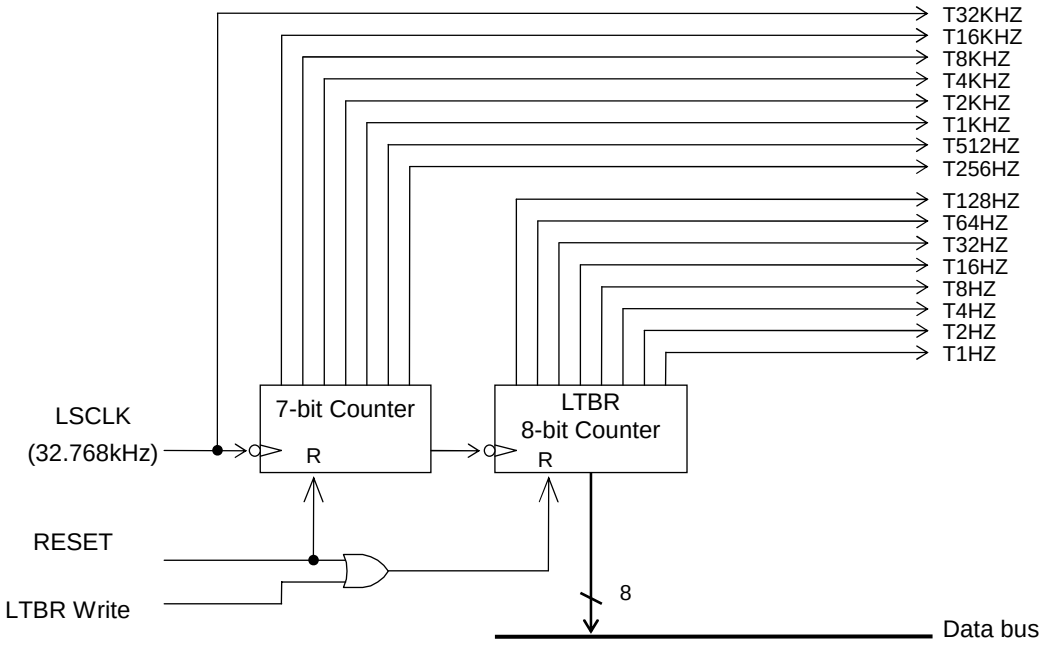
This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 6, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 5, "Interrupts".

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- HTBC generates the divided clock by dividing the high-speed clock (HSCLK) frequency of HTBCLK. It is used as the timer's clock or the PWM's clocks.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

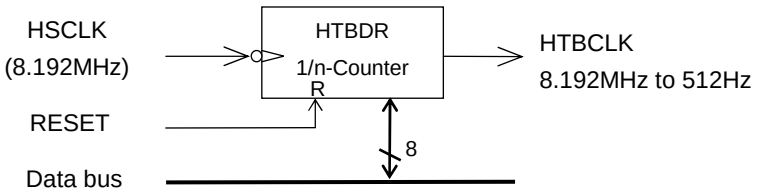
7.1.2 Configuration

Figure 7-1 and Figure 7-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.



LTBR: Low-speed time base counter register

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)



HTBDR: High-speed time base counter frequency divide register

Figure 7-2 Configuration of High-Speed Time Base Counter

Note:
The frequency of HSCLK is changed by setting of SYSC1 bit and SYSC0 bit in the frequency control register 0 (FCON0).

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	—	R/W	8	00H

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter.
The T128HZ-T1HZ outputs are set to "0" when write operation is performed for LTBR. However, write data is invalid.

Note:
A TBC interrupt (128Hz interrupt, 32Hz interrupt, 16Hz interrupt, or 2Hz interrupt) may occur depending on the LTBR write timing (see Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR"). Therefore, take care in software programming, refer to Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR".

7.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	—	—	—	—	HTD3	HTD2	HTD1	HTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the divide ratio of the 4-bit, 1/n counter.

[Description of Bits]

- **HTD3 to HTD0** (bits 3-0)

The HTD3-HTD0 bits are used to set the frequency divide ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Divide ratio	Frequency of HTBCLK (*1)
0	0	0	0	× 1/16 (initial value)	512 kHz
0	0	0	1	× 1/15	546 kHz
0	0	1	0	× 1/14	586 kHz
0	0	1	1	× 1/13	630 kHz
0	1	0	0	× 1/12	682 kHz
0	1	0	1	× 1/11	744 kHz
0	1	1	0	× 1/10	820 kHz
0	1	1	1	× 1/9	910 kHz
1	0	0	0	× 1/8	1024 kHz
1	0	0	1	× 1/7	1170 kHz
1	0	1	0	× 1/6	1366 kHz
1	0	1	1	× 1/5	1638 kHz
1	1	0	0	× 1/4	2048 kHz
1	1	0	1	× 1/3	2730 kHz
1	1	1	0	× 1/2	4096 kHz
1	1	1	1	× 1/1	8192 kHz

*1: Indicates the frequency when the high-speed oscillation clock (HSCLK) is 8192 kHz.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T32HZ, T16HZ, and T2HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-3 shows an example of program to read LTBR.

```
        LEA     offset LTBR         ; EA←LTBR address
MARK:
        L       R0,     [EA]        ; 1st read
        L       R1,     [EA]        ; 2nd read
;
        CMP     R0,     R1          ; Comparison for LTBR
        BNE     MARK                ; To MARK when the values do not coincide
;
            :
```

Figure 7-3 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid.
Since an interrupt occurs if a falling edge occurs in the T128Hz to T1Hz outputs during writing to LTBR, take care in software programming.
Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

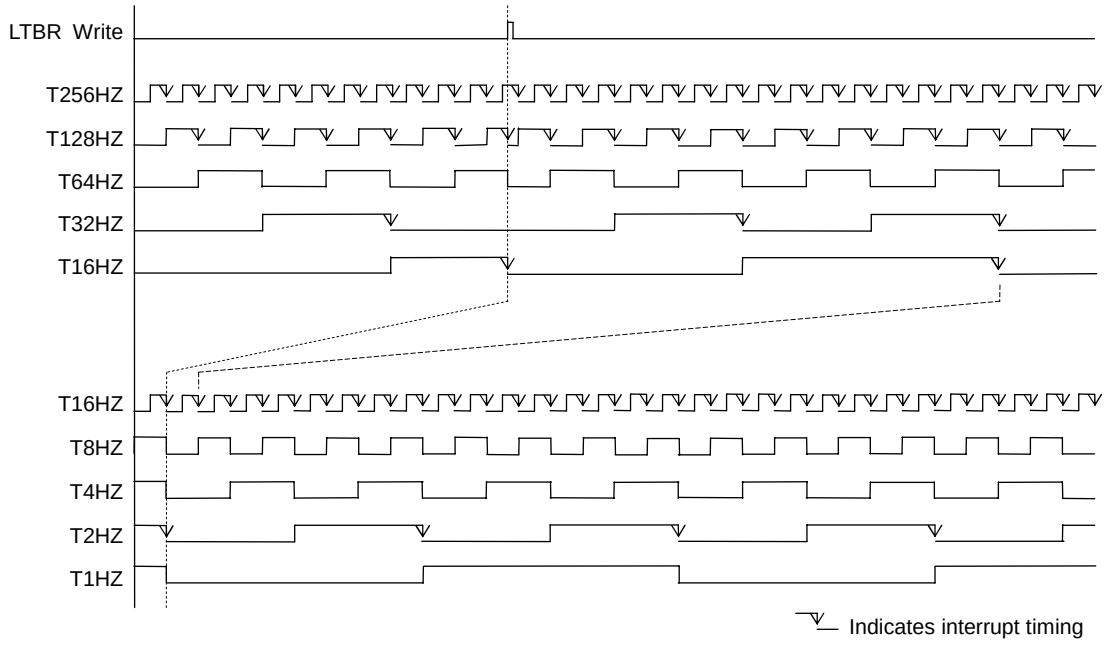


Figure 7-4 Interrupt Timing and Reset Timing by Writing to LTBR

7.3.2 High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16×HSCLK to 1/1×HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as an operaiton clock of the timer and PWM.
Figure 7-5 shows the output waveform of HTBCLK.

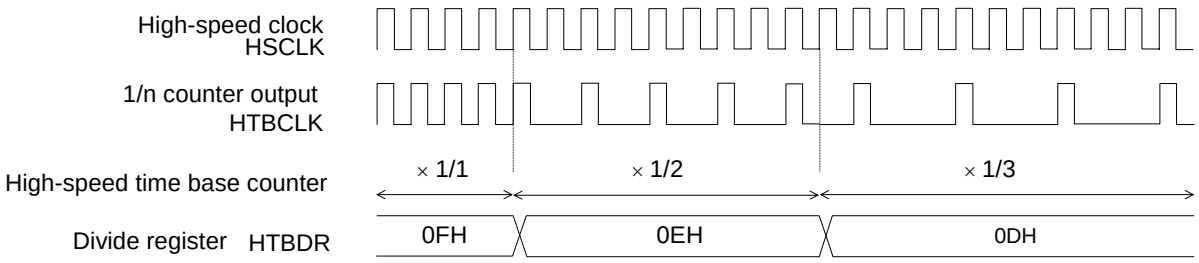


Figure 7-5 Output Waveform of HTBCLK

Chapter 8

Timers

8 Timers

8.1 Overview

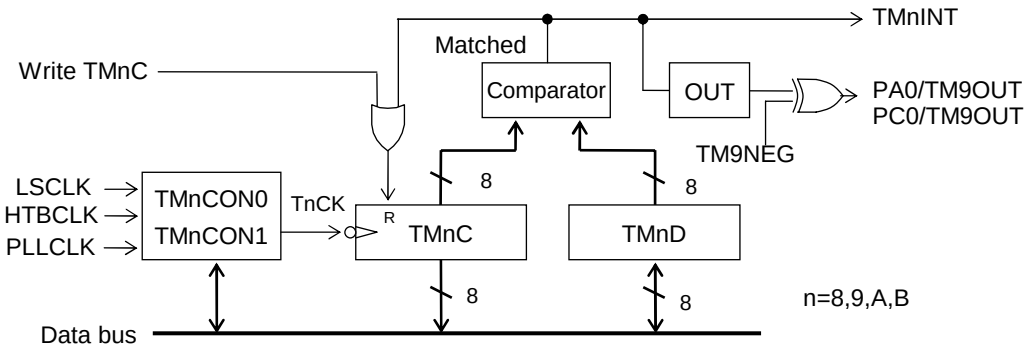
This LSI includes 6 channels of 8-bit timers.

8.1.1 Features

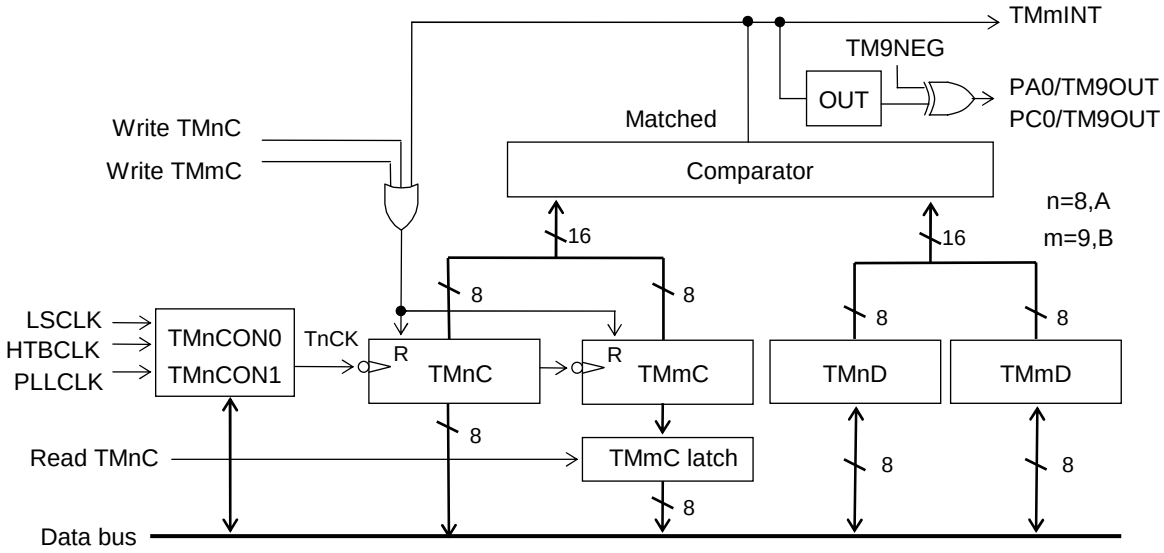
- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=8, 9, A, B, E, F) and timer data register (TMnD) coincide.
- A timer configured by combining timer 8 and timer 9, timer A and timer B, or timer E and timer F can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK), high-speed time base clock (HTBCLK), or the divided clock PLLCLK can be selected.
- The timer out signal of a timer 9 and Timer F (TM9OUT, TMFOUT) can be outputted.
- The output logic of the TM9OUT and TMFOUT signals can be switched to the positive or negative logic.
- Auto-reload timer mode and one-shot timer mode can be selected.
- For timer E and timer F, timer start/stop by the external trigger input can be controlled.
- Pulse width, etc. can be measured using the external trigger input. (Measurable minimum pulse width is timer clock 3ϕ)

8.1.2 Configuration

Figure 8-1 shows the configuration of the timers.



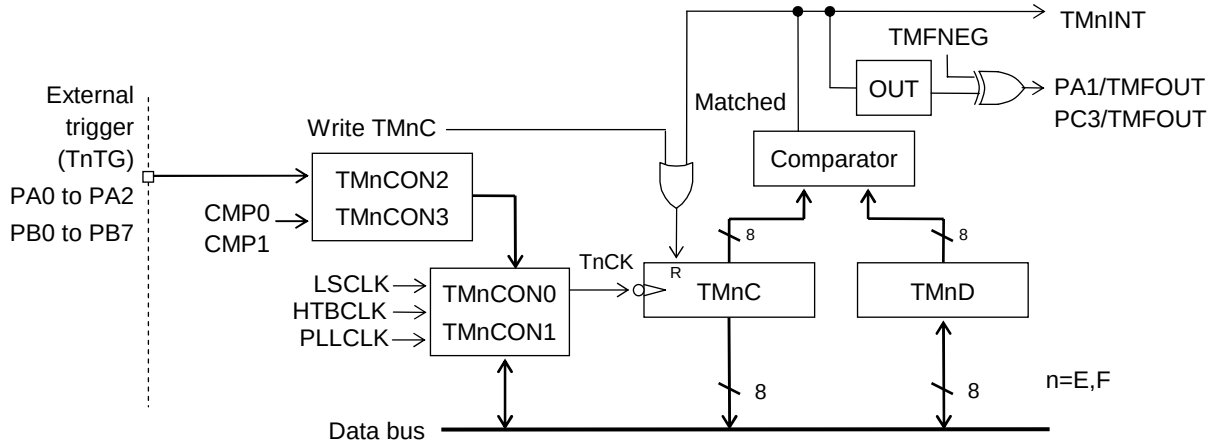
(a) In 8-bit Timer Mode (Timers 8 to B)



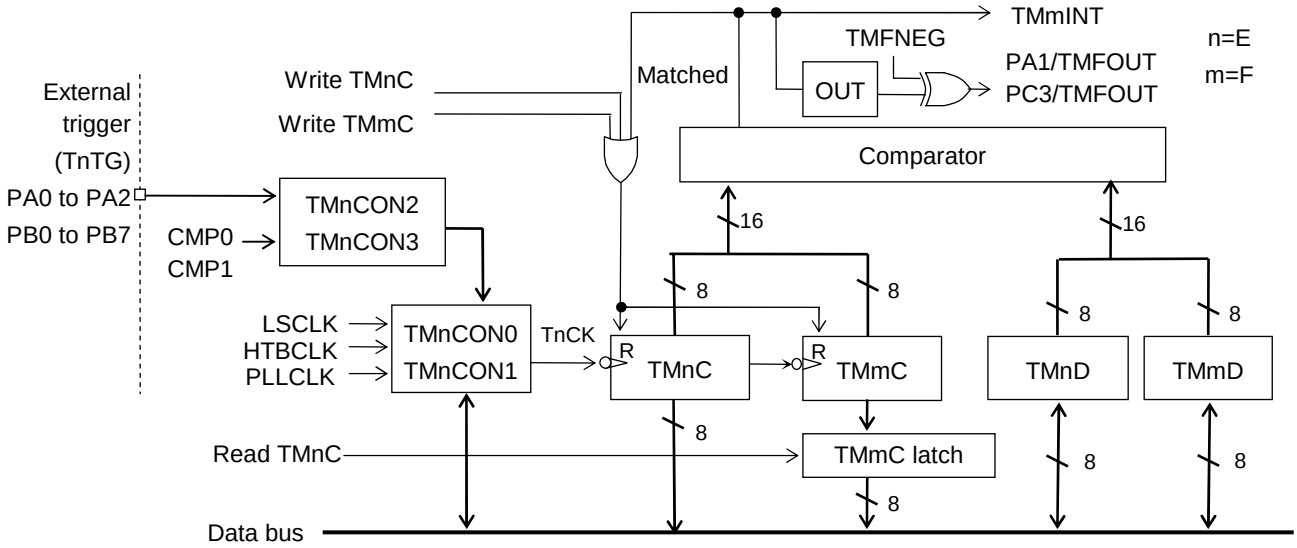
(b) In 16-bit Timer Mode (Timer 8 to B)

TMnCON0	: Timer control register 0
TMnCON1	: Timer control register 1
TMmD, TMnD	: Timer data register
TMmC, TMnC	: Timer counter register

Figure 8-1a the configuration of timers



(c) In 8-bit Timer Mode (Timer E, F)



(d) In 16-bit Timer Mode (Timer E, F)

TMnCON0 : Timer control register 0
TMnCON1 : Timer control register 1
TMnCON2 : Timer control register 2
TMnCON3 : Timer control register 3
TMmD, TMnD : Timer data register
TMmC, TMnC : Timer counter register
CMP0/1 : Comparator output

Figure 8-1b the configuration of timers

8.1.3 List of Pins

Pin name	Input/output	Function
PA0/TnTG/TM9OUT	I/O	External trigger input of timer E/F Timer 9 output pin: Use for the quaternary function of PA0.
PA1/TnTG/TMFOUT	I/O	External trigger input of timer E/F Timer 9 output pin: Use for the quaternary function of PA1.
PA2/TnTG	I	External trigger input of timer E/F
PB0~7/TnTG	I	External trigger input of timer E/F
PC0/TM9OUT	I/O	Timer 9 output pin: Use for the quaternary function of PC0.
PC3/TMFOUT	I	Timer F output pin: Use for the quaternary function of PC3.

(n = E, F)

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F8E0H	Timer 8 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 8 counter register	TM8C		R/W	8	00H
0F8E2H	Timer 8 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 8 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 9 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 9 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 9 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 9 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer A data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer A counter register	TMAC		R/W	8	00H
0F8EAH	Timer A control register 0	TMACON0	TMACON	R/W	8/16	00H
0F8EBH	Timer A control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer B data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer B counter register	TMBC		R/W	8	00H
0F8EEH	Timer B control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer B control register 1	TMBCON1		R/W	8	00H
0F360H	Timer E data register	TMED	TMEDC	R/W	8/16	0FFH
0F361H	Timer E counter register	TMEC		R/W	8	00H
0F362H	Timer E control register 0	TMECON0	TMECON	R/W	8/16	00H
0F363H	Timer E control register 1	TMECON1		R/W	8	00H
0F364H	Timer E control register 2	TMECON2	TMECON23	R/W	8/16	00H
0F365H	Timer E control register 3	TMECON3		R/W	8	00H
0F368H	Timer F data register	TMFD	TMFDC	R/W	8/16	0FFH
0F369H	Timer F counter register	TMFC		R/W	8	00H
0F36AH	Timer F control register 0	TMFCON0	TMFCON	R/W	8/16	00H
0F36BH	Timer F control register 1	TMFCON1		R/W	8	00H
0F36CH	Timer F control register 2	TMFCON2	TMFCON23	R/W	8/16	00H
0F36DH	Timer F control register 3	TMFCON3		R/W	8	00H

8.2.2 Timer 8 Data Register (TM8D)

Address: 0F8E0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM8D	T8D7	T8D6	T8D5	T8D4	T8D3	T8D2	T8D1	T8D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM8D is a special function register (SFR) to set the value to be compared with the Timer 8 counter register (TM8C) value.

Note:
Set TM8D when the timer stops.
In 8-bit timer mode, writing "00H" to TM8D sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TM8D and the high-order TM9D sets the low-order TM8D to "01H" and the high-order TM9D to "00H".
However, when TM8D is read, "00H" is read.

8.2.3 Timer 9 Data Register (TM9D)

Address: 0F8E4H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM9D	T9D7	T9D6	T9D5	T9D4	T9D3	T9D2	T9D1	T9D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM9D is a special function register (SFR) to set the value to be compared with the value of the Timer 9 counter register (TM9C).

Note:
Set TM9D when the timer stops (When T9STAT bit of TM9CON1 register is "0").
In 8-bit timer mode, writing "00H" to TM9D sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TM8D and the high-order TM9D sets the low-order TM8D to "01H" and the high-order TM9D to "00H".

8.2.4 Timer A Data Register (TMAD)

Address: 0F8E8H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMAD	TAD7	TAD6	TAD5	TAD4	TAD3	TAD2	TAD1	TAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMAD is a special function register (SFR) to set the value to be compared with the Timer A counter register (TMAC) value.

Note:
Set TMAD when the timer stops.
In 8-bit timer mode, writing "00H" to TMAD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMAD and the high-order TMBD sets the low-order TMAD to "01H" and the high-order TMBD to "00H".
However, when TMAD is read, "00H" is read.

8.2.5 Timer B Data Register (TMBD)

Address: 0F8ECH
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMBD	TBD7	TBD6	TBD5	TBD4	TBD3	TBD2	TBD1	TBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMBD is a special function register (SFR) to set the value to be compared with the value of the Timer B counter register (TMBC).

Note:
Set TMBD when the timer stops (When TBSTAT bit of TMBCON1 register is "0").
In 8-bit timer mode, writing "00H" to TMBD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMAD and the high-order TMBD sets the low-order TMAD to "01H" and the high-order TMBD to "00H".

8.2.6 Timer E Data Register (TMED)

Address: 0F360H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMED	TED7	TED6	TED5	TED4	TED3	TED2	TED1	TED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMED is a special function register (SFR) to set the value to be compared with the Timer E counter register (TMEC) value.

Note:
Set TMED when the timer stops (When TESTAT bit of TMECON1 register is "0").
In 8-bit timer mode, writing "00H" to TMED sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMED and the high-order TMFD sets the low-order TMED to "01H" and the high-order TMFD to "00H".
However, when TMED is read, "00H" is read.

8.2.7 Timer F Data Register (TMFD)

Address: 0F368H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMFD	TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMFD is a special function register (SFR) to set the value to be compared with the value of the Timer F counter register (TMFC).

Note:
Set TMFD when the timer stops (When TFSTAT bit of TMFCON1 register is "0").
In 8-bit timer mode, writing "00H" to TMFD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMED and the high-order TMFD sets the low-order TMED to "01H" and the high-order TMFD to "00H".

8.2.8 Timer 8 Counter Register (TM8C)

Address: 0F8E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8C	T8C7	T8C6	T8C5	T8C4	T8C3	T8C2	T8C1	T8C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM8C is performed, TM8C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TM8C and the high-order TM9C are set to "00H" when write operation to either the low-order or the high-order is performed.

During timer operation, the contents of TM8C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TM8C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-1 TM8C Read Enable/Disable during Timer Operation

Timer clock T8CK	System clock SYSCLK	TM8C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TM8C twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TM8C twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.9 Timer 9 Counter Register (TM9C)

Address: 0F8E5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9C	T9C7	T9C6	T9C5	T9C4	T9C3	T9C2	T9C1	T9C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM9C is performed, TM9C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TM8C and the high-order TM9C are set to "00H" when write operation to either the low-order or the high-order is performed.
When reading TM9C in 16-bit timer mode, be sure to read TM8C first since the count value of TM9C is stored in the TM9C latch when TM8C is read.

During timer operation, the contents of TM9C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TM9C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-2 TM9C Read Enable/Disable during Timer Operation

Timer clock T9CK	System clock SYSCLK	TM9C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TM9C twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TM9C twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.10 Timer A Counter Register (TMAC)

Address: 0F8E9H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMAC	TAC7	TAC6	TAC5	TAC4	TAC3	TAC2	TAC1	TAC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMAC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMAC is performed, TMAC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TMAC and the high-order TMBC are set to "00H" when write operation to either the low-order or the high-order is performed.

During timer operation, the contents of TMAC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-3 shows whether a TMAC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-3 TMAC Read Enable/Disable during Timer Operation

Timer clock TACK	System clock SYSCLK	TMAC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMAC twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMAC twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.11 Timer B Counter Register (TMBC)

Address: 0F8EDH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBC	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMBC is performed, TMBC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TMAC and the high-order TMBC are set to "00H" when write operation to either the low-order or the high-order is performed.
When reading TMBC in 16-bit timer mode, be sure to read TMAC first since the count value of TMBC is stored in the TMBC latch when TMAC is read.

During timer operation, the contents of TMBC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-4 shows whether a TMBC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-4 TMBC Read Enable/Disable during Timer Operation

Timer clock TBCK	System clock SYSCLK	TMBC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMBC twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMBC twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.12 Timer E Counter Register (TMEC)

Address: 0F361H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMEC	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMEC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMEC is performed, TMEC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TMEC and the high-order TMFC are set to "00H" when write operation to either the low-order or the high-order is performed.

During timer operation, the contents of TMEC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-5 shows whether a TMEC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-5 TMEC Read Enable/Disable during Timer Operation

Timer clock TECK	System clock SYSCLK	TMEC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMEC twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMEC twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.13 Timer F Counter Register (TMFC)

Address: 0F369H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFC	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMFC is performed, TMFC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, both the low-order TMEC and the high-order TMFC are set to "00H" when write operation to either the low-order or the high-order is performed.
When reading TMFC in 16-bit timer mode, be sure to read TMEC first since the count value of TMFC is stored in the TMFC latch when TMEC is read.

During timer operation, the contents of TMFC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-6 shows whether a TMFC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-6 TMFC Read Enable/Disable during Timer Operation

Timer clock TFCK	System clock SYSCLK	TMFC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMFC twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
1/2 HTBCLK to 1/64 HTBCLK	LSCLK	Read disabled.
1/2 HTBCLK to 1/64 HTBCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting up, read consecutively TMFC twice until the last data matched the previous data.
PLLCLK	LSCLK	Read disabled.
PLLCLK	HSCLK	Read disabled.

8.2.14 Timer 8 Control Register 0 (TM8CON0)

Address: 0F8E2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON0	T8OST	—	T89M16	—	—	T8CS2	T8CS1	T8CS0
R/W	R/W	R	R/W	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON0 is a special function (SFR) to control the Timer 8.
Rewrite TM8CON0 while the Timer 8 is stopped (T8STAT of the TM8CON1 register is "0").

[Description of Bits]

- **T8CS2, T8CS1, T8CS0** (bits 2 to 0)

The T8CS2, T8CS1, T8CS0 bits are used for selecting the operation clock of Timer 8. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16HTBCLK , 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.

T8CS2	T8CS1	T8CS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

- **T89M16** (bit 5)

The T89M16 bit is used for selecting the operating mode of Timer 8 and Timer 9.
In 8-bit timer mode, each of Timer 8 and Timer 9 operates independently as a 8-bit timer.
In 16-bit timer mode, Timer 8 and Timer 9 are connected and they operate as a 16-bit timer.
In 16-bit timer mode, Timer 9 is incremented by a Timer 8 overflow signal.
A Timer 8 interrupt (TM8INT) is not generated.

T89M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **T8OST** (bit 7)

The T8OST bit is used for selecting the operating mode of Timer 8. When T8OST is set to "1", the one-shot timer mode is available.

T8OST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.15 Timer 9 Control Register 0 (TM9CON0)

Address: 0F8E6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON0	T9OST	T9NEG	—	—	—	T9CS2	T9CS1	T9CS0
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON0 is a special function (SFR) to control the Timer 9.
Rewrite TM9CON0 while the Timer 9 is stopped (T9STAT of the TM9CON1 register is "0").

[Description of Bits]

- **T9CS2, T9CS1, T9CS0** (bits 2 to 0)

  The T9CS2, T9CS1, T9CS0 bits are used for selecting the operation clock of Timer 9. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16 HTBCLK, 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.
  In cases where the 16-bit timer mode has been selected by setting T89M16 of TM8CON0 to "1", the values of T9CS2, T9CS1, T9CS0 are invalid.

T9CS2	T9CS1	T9CS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

- **T9NEG** (bit 6)

  The T9NEG bit is used to select the output logic of TM9OUT. The initial value of TM9OUT output is "0" for the positive logic, and "1" for the negative logic.

T9NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **T9OST** (bit 7)

  The T9OST bit is used for selecting the operating mode of Timer 9. When T9OST is set to "1", the one-shot timer mode is available.
  In cases where the 16-bit timer mode has been selected by setting T89M16 of TM9CON0 to "1", the value of T9OST is invalid.

T9OST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.16 Timer A Control Register 0 (TMACON0)

Address: 0F8EAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON0	TAOST	—	TABM16	—	—	TACS2	TACS1	TACS0
R/W	R/W	R	R/W	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON0 is a special function (SFR) to control the Timer A.
Rewrite TMACON0 while the Timer A is stopped (TASTAT of the TMACON1 register is "0").

[Description of Bits]

- **TACS2, TACS1, TACS0** (bits 2 to 0)

The TACS2, TACS1, TACS0 bits are used for selecting the operation clock of Timer A. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16 HTBCLK, 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.

TACS2	TACS1	TACS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

- **TABM16** (bit 5)

The TABM16 bit is used for selecting the operating mode of Timer A and Timer B.
In 8-bit timer mode, each of Timer A and Timer B operates independently as a 8-bit timer.
In 16-bit timer mode, Timer A and Timer B are connected and they operate as a 16-bit timer.
In 16-bit timer mode, Timer B is incremented by a Timer A overflow signal. A Timer A interrupt (TMAINT) is not generated.

TABM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **TAOST** (bit 7)

The TAOST bit is used for selecting the operating mode of Timer A. When TAOST is set to "1", the one-shot timer mode is available.

TAOST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.17 Timer B Control Register 0 (TMBCON0)

Address: 0F8EEH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON0	TBOST	—	—	—	—	TBCS2	TBCS1	TBCS0
R/W	R/W	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON0 is a special function (SFR) to control the Timer B.
Rewrite TMBCON0 while the Timer B is stopped (TBSTAT of the TMBCON1 register is "0").

[Description of Bits]

- **TBCS2, TBCS1, TBCS0** (bits 2 to 0)

  The TBCS2, TBCS1, TBCS0 bits are used for selecting the operation clock of Timer B. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16 HTBCLK, 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.
  In cases where the 16-bit timer mode has been selected by setting TABM16 of TMACON0 to "1", the values of TBCS2, TBCS1, TBCS0 are invalid.

TBCS2	TBCS1	TBCS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

- **TBOST** (bit 7)

  The TBOST bit is used for selecting the operating mode of Timer B. When TBOST is set to "1", the one-shot timer mode is available.
  In cases where the 16-bit timer mode has been selected by setting TABM16 of TMACON0 to "1", the value of TBOST is invalid.

TBOST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.18 Timer E Control Register 0 (TMECON0)

Address: 0F362H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON0	—	—	—	—	TECS2	TEFM16	TECS1	TECS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON0 is a special function (SFR) to control the Timer E.
Rewrite TMECON0 while the Timer E is stopped (TERUN, TETGEN and TESTAT of the TMECON1 register are "0").

[Description of Bits]

- **TECS2, TECS1, TECS0** (bits 3, 1 to 0)

  The TECS2, TECS1, TECS0 bits are used for selecting the operation clock of Timer E. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16 HTBCLK, 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.

TECS2	TECS1	TECS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

- **TEFM16** (bit 2)

  The TEFM16 bit is used for selecting the operating mode of Timer E and Timer F.
  In 8-bit timer mode, each of Timer E and Timer F operates independently as a 8-bit timer.
  In 16-bit timer mode, Timer E and Timer F are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, Timer F is incremented by a Timer E overflow signal.
  A Timer E interrupt (TMEINT) is not generated.

TEFM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

8.2.19 Timer F Control Register 0 (TMFCON0)

Address: 0F36AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON0	—	—	—	—	TFCS2	—	TFCS1	TFCS0
R/W	R	R	R	R	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON0 is a special function (SFR) to control the Timer F.
Rewrite TMFCON0 while the Timer F is stopped (TFEN, TFTGEN and TFSTAT of the TMFCON1 register are "0").

[Description of Bits]

- **TFCS2, TFCS1, TFCS0** (bits 3, 1 to 0)

  The TFCS2, TFCS1, TFCS0 bits are used for selecting the operation clock of Timer F. LSCLK, HTBCLK, 1/64 HTBCLK, 1/16 HTBCLK, 1/8 HTBCLK, 1/4 HTBCLK, 1/2 HTBCLK, and PLLCLK can be selected.
  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON0 to "1", the values of TFCS2, TFCS1, TFCS0 are invalid.

TFCS2	TFCS1	TFCS0	Description
0	0	0	LSCLK (initial value)
0	0	1	HTBCLK
0	1	0	1/64 HTBCLK
0	1	1	1/16 HTBCLK
1	0	0	1/8 HTBCLK
1	0	1	1/4 HTBCLK
1	1	0	1/2 HTBCLK
1	1	1	PLLCLK

8.2.20 Timer 8 Control Register 1 (TM8CON1)

Address: 0F8E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON1	T8STAT	—	—	—	—	—	—	T8RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON1 is a special function register (SFR) to control the Timer 8.

[Description of Bits]

- **T8RUN** (bit 0)
  The T8RUN bit is used for controlling count stop/start of Timer 8.

T8RUN	Description
0	Stops counting.
1	Starts counting.

- **T8STAT** (bit 7)
  The T8STAT bit is used for indicating "counting stopped"/"counting in progress" of Timer 8.

T8STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.21 Timer 9 Control Register 1 (TM9CON1)

Address: 0F8E7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON1	T9STAT	—	—	—	—	—	—	T9RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON1 is a special function register (SFR) to control the Timer 9.

[Description of Bits]

- **T9RUN** (bit 0)
  The T9RUN bit is used for controlling count stop/start of Timer 9.
  When T89M16 of TM8CON0 is set to "1" and 16 bit timer mode is selected, make sure that it is set to "0".
  Timer 9 is incremented caused by a Timer 8 overflow signal regardless of the value of T9RUN.

T9RUN	Description
0	Stops counting.
1	Starts counting.

- **T9STAT** (bit 7)
  The T9STAT bit is used for indicating "counting stopped"/"counting in progress" of Timer 9.
  When T89M16 of TM8CON0 is set to "1" and 16 bit timer mode is selected, "0" is read.

T9STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.22 Timer A Control Register 1 (TMACON1)

Address: 0F8EBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON1	TASTAT	—	—	—	—	—	—	TARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON1 is a special function register (SFR) to control the Timer A.

[Description of Bits]

- **TARUN** (bit 0)
  The TARUN bit is used for controlling count stop/start of Timer A.

TARUN	Description
0	Stops counting.
1	Starts counting.

- **TASTAT** (bit 7)
  The TASTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer A.

TASTAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.23 Timer B Control Register 1 (TMBCON1)

Address: 0F8EFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON1	TBSTAT	—	—	—	—	—	—	TBRUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON1 is a special function register (SFR) to control the Timer B.

[Description of Bits]

- **TBRUN** (bit 0)
  The TBRUN bit is used for controlling count stop/start of Timer B.
  When TABM16 of TMACON0 is set to "1" and 16 bit timer mode is selected, make sure that it is set to "0".
  Timer B is incremented caused by a Timer A overflow signal regardless of the value of TBRUN.

TBRUN	Description
0	Stops counting.
1	Starts counting.

- **TBSTAT** (bit 7)
  The TBSTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer B.
  When TABM16 of TMACON0 is set to "1" and 16 bit timer mode is selected, "0" is read.

TBSTAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.24 Timer E Control Register 1 (TMECON1)

Address: 0F363H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON1	TESTAT	—	—	—	—	—	TETGEN	TERUN
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON1 is a special function register (SFR) to control the Timer E.

[Description of Bits]

- **TERUN** (bit 0)
  The TERUN bit is used for controlling count stop/start of Timer E.

TERUN	Description
0	Stops counting.
1	Starts counting.

- **TETGEN** (bit 1)
  The TETGEN bit is enable flag of timer E count stop/start by the external trigger input.

TETGEN	Description
0	Disables the count stop/start by the external trigger. (Initial value)
1	Enables the count stop/start by the external trigger.

- **TESTAT** (bit 7)
  The TESTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer E.

TESTAT	Description
0	Counting stopped.
1	Counting in progress.

Note:
For the auto-reload timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TERUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TERUN bit shows "1" as is controlled to start (keep) counting. Therefore, reading TERUN bit can be used for recognizing which interrupt occurred.
For one shot timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TERUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TERUN bit also shows "0" as is controlled to stop counting. To recognizing which interrupt occurred, read timer count register and timer data register and check if the timer count register value is consistent timer data register value.
When the timer count is stopped by the external trigger and TERUN bit shows "0", make sure to start the next operation after TESTAT bit shows "0" as the timer count is halted.

8.2.25 Timer F Control Register 1 (TMFCON1)

Address: 0F36BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON1	TFSTAT	—	—	—	—	—	TFTGEN	TFRUN
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON1 is a special function register (SFR) to control the Timer F.

[Description of Bits]

- **TFRUN** (bit 0)

  The TFRUN bit is used for controlling count stop/start of Timer F.
  When TEFM16 of TMECON0 is set to "1" and 16 bit timer mode is selected, make sure that it is set to "0".
  Timer F is incremented caused by a Timer E overflow signal regardless of the value of TFRUN.

TFRUN	Description
0	Stops counting.
1	Starts counting.

- **TFTGEN** (bit 1)

  The TFTGEN bit is enable flag of timer F stop/start by the external trigger input.
  When TEFM16 of TMECON0 is set to "1" and 16 bit timer mode is selected, make sure that it is set to "0".

TFTGEN	Description
0	Disables the count stop/start by the external trigger. (Initial value)
1	Enables the count stop/start by the external trigger.

- **TFSTAT** (bit 7)

  The TFSTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer F.
  When TEFM16 of TMECON0 is set to "1" and 16 bit timer mode is selected, "0" is read.

TFSTAT	Description
0	Counting stopped.
1	Counting in progress.

Note:
For the auto-reload timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TFRUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TFRUN bit shows "1" as is controlled to start (keep) counting. Therefore, reading TFRUN bit can be used for recognizing which interrupt occurred.
For one shot timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TFRUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TFRUN bit also shows "0" as is controlled to stop counting. To recognizing which interrupt occurred, read timer count register and timer data register and check if the timer count register value is consistent timer data register value.
When the timer count is stopped by the external trigger and TFRUN bit shows "0", make sure to start the next operation after TFSTAT bit shows "0" as the timer count is halted.

8.2.26 Timer E Control Register 2 (TMECON2)

Address: 0F364H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON2	TEOST	—	TETRM1	TETRM0	—	—	TEST1	TEST0
R/W	R/W	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON2 is a special function (SFR) to control the Timer E.
Rewrite TMECON2 while the Timer E is stopped (TFRUN, TETGEN and TESTAT of the TMECON1 register are "0").

[Description of Bits]

- **TEST1, TEST0** (bits 1, 0)
  The TEST1 and TEST0 bits are used to select the start/stop mode of the timer E counter.

TEST1	TEST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **TETRM1, TETRM0** (bits 5, 4)
  The TETRM1 and TETRM0 bits are used to select the start mode of the timer E counter.This is valid only when the external input start and stop modes are selected. When the timer count is stopped by the external input, an interrupt is generated.

TETRM1	TETRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

- **TEOST** (bit 7)
  The TEOST bit is used for the operation mode of timer E. When TEOST is set to "1", the one-shot timer mode is available.

TEOST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.27 Timer F Control Register 2 (TMFCON2)

Address: 0F36CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON2	TFOST	TFNEG	TFTRM1	TFTRM0	—	—	TFST1	TFST0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON2 is a special function (SFR) to control the Timer F.
Rewrite TMFCON2 while the Timer F is stopped (TFRUN, TFTGEN and TFSTAT of the TMFCON1 register are "0").

[Description of Bits]

- **TFST1, TFST0** (bits 1, 0)

  The TFST1 and TFST0 bits are used to select the start/stop mode of the timer F counter.
  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON0 to "1", the values of TFST1 and TFST0 are invalid.

TFST1	TFST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **TFTRM1, TFTRM0** (bits 5, 4)

  The TFTRM1 and TFTRM0 bits are used to select the start mode of the timer F counter.This is valid only when the external input start and stop modes are selected. When the timer count is stopped by the external input, an interrupt is generated.
  When TEFM16 of TMECON0 is set to "1" and 16 bit timer mode is selected, the value of TFTRM1 and TFTRM0 becomes invalid.

TFTRM1	TFTRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

- **TFNEG** (bit 6)

  The TFNEG bit is used to select the output logic of TMFOUT. The initial value of TMFOUT output is "0" for the positive logic and "1" for the negative logic.

TFNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **TFOST** (bit 7)

  The TFOST bit is used for the operation mode of timer E. When TFOST is set to "1", the one-shot timer mode is available.

  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON0 to "1", the value of TFOST is invalid.

TFOST	Description
0	Auto-reload timer mode (initial value)
1	One shot timer mode

8.2.28 Timer E Control Register 3 (TMECON3)

Address: 0F365H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON3	—	—	—	—	TESTSS	TESTS2	TESTS1	TESTS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON3 is a special function register (SFR) to control the Timer E.
Rewrite TMECON3 when TERUN, TETGEN, and TESTAT of TMECON1 register are "0".

[Description of Bits]

- **TESTSS, TESTS2, TESTS1**, **TESTS0** (bits 3 to 0)
  The TESTSS, TESTS2, TESTS1, and TESTS0 bits are used to select the external input start/stop pins of the timer E. To use these bits to select the Port A and B pins, use the Port A and B mode registers 0,1 (PnMOD0, PnMOD1) to select the primary function and use the Port A and B direction (PnDIR) to set the input mode for the appropriate pins.
  (n=A,B)

TESTS2	**TESTS1**	**TESTS0**	Description	
			When TESTSS="0" (initial value)	When TESTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0	PB3 pin
1	0	0	CMP1	PB4 pin
1	0	1	Prohibited (*)	PB5 pin
1	1	0	Prohibited (*)	PB6 pin
1	1	1	Prohibited (*)	PB7 pin

8.2.29 Timer F Control Register 3 (TMFCON3)

Address: 0F36DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON3	—	—	—	—	TFSTSS	TFSTS2	TFSTS1	TFSTS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON3 is a special function register (SFR) to control the Timer F.
Rewrite TMFCON3 when TFRUN, TFTGEN, and TFSTAT of TMFCON1 register are "0".

[Description of Bits]

- **TFSTSS, TFSTS2, TFSTS1**, **TFSTS0** (bits 3 to 0)

  The TFSTSS, TFSTS2, TFSTS1, and TFSTS0 bits are used to select the external input start/stop pins of the timer F. To use these bits to select the Port A and B pins, use the Port A and B mode registers 0,1 (PnMOD0, PnMOD1) to select the primary function and use the Port A and B direction (PnDIR) to set the input mode for the appropriate pins.
  (n=A,B)
  When TEFM16 of TMECON0 is set to "1" and 16 bit timer mode is selected, the value of TFSTSS and TFSTS2 and TFSTS1 and TFSTS0 becomes invalid.

TFSTS2	TFSTS1	TFSTS0	Description	
			When TFSTSS="0" (initial value)	When TFSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0	PB3 pin
1	0	0	CMP1	PB4 pin
1	0	1	Prohibited (*)	PB5 pin
1	1	0	Prohibited (*)	PB6 pin
1	1	1	Prohibited (*)	PB7 pin

8.3 Description of Operation

8.3.1 Timer basic operation

When the TnRUN bit of timer 8 to B,E,F control register 1 (TMnCON1) is set to "1", the timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer 8 to B,E,F control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.
When the count value of TMnC and the timer 8 to B,E,F data register (TMnD) coincide, timer 8 to B,E,F interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing.
When the TnRUN bit is set to "0", TMnC stops incrementing after counting the falling of the timer clock (TnCK) once. Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 8 to B,E,F control register 1 (TMnCON1) is "0". When the TnRUN bit is set to "1" again, TMnC restarts incrementing from the previous value. To initialize TMnC to "00H", perform a write operation to TMnC.
The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n = 8 \text{ to } B,E,F)$$

TMnD: Timer 8 to B,E,F data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 8 to B,E,F control register 0 (TMnCON0)

After the TnRUN bit is set to "1", the timer is synchronized by the timer clock to start counting. Therefore, an error of a maximum of 1 clock period occurs until the first timer interrupt occurs. The timer interrupt periods from the second time onward are constant.

Figure 8-2 shows the operation timing diagram of Timer 8 to B,E,F.
Whenever the value of the count value of TMnC and the preset value of a timer n data register (TMnD) is matched , the output value of timer out (TM9OUT, TMFOUT) is reversed. This timer out can be outputted outside as fourthly function of a port A. Timer out is set to "0" to the time of system reset, and a timer count stop.

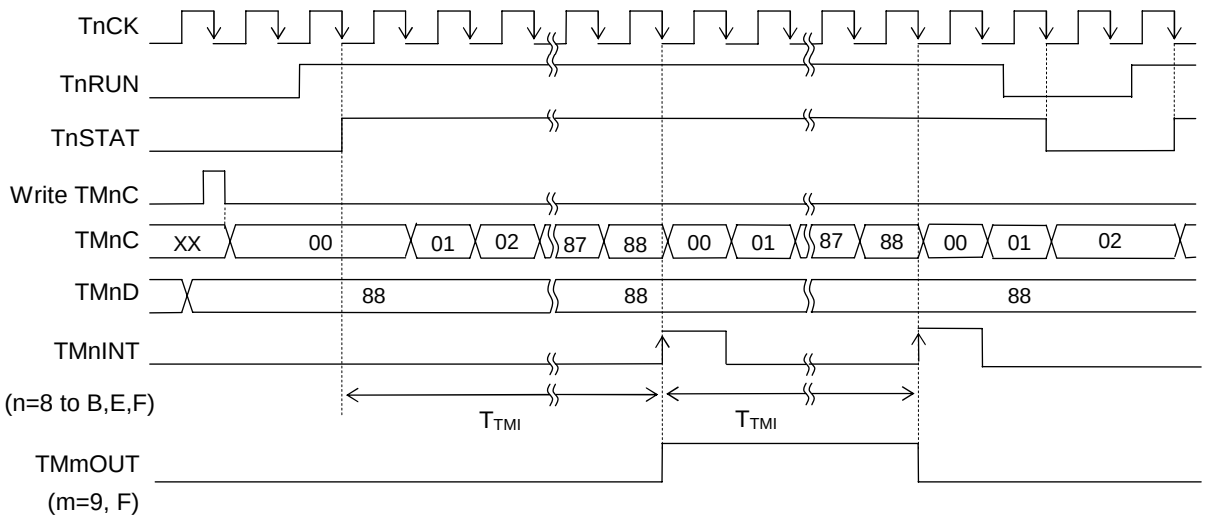


Figure 8-2 Auto-reload timer mode Operation Timing Diagram of Timer 8 to B,E,F

Note:
Even if "0" is written to the TnRUN bit, counting operation continues up to the falling edge (the timer 8 to B,E,F status flag (TnSTAT) is in a "1" state) of the next timer clock pulse. Therefore, the timer 8 to B,E,F interrupt (TMnINT) may occur.
During a timer stop, an external-triggering stop becomes invalid until TnSTAT will be set to "1", if a TnRUN bit is set "1". Moreover, when the timer is running, an external-triggering start becomes invalid until TnSTAT will be set to "0", if a TnRUN bit is set "0".

Figure 8-3 shows one-shot timer mode operation timing of timer 8 to B, E, F.
If timer out (TM9OUT and TMFOUT) is started with TnRUN of 1, timer out is inverted. Whenever the value of the count value of TMnC and the preset value of a timer n data register (TMnD) is matched , the output is returned to the initial value.

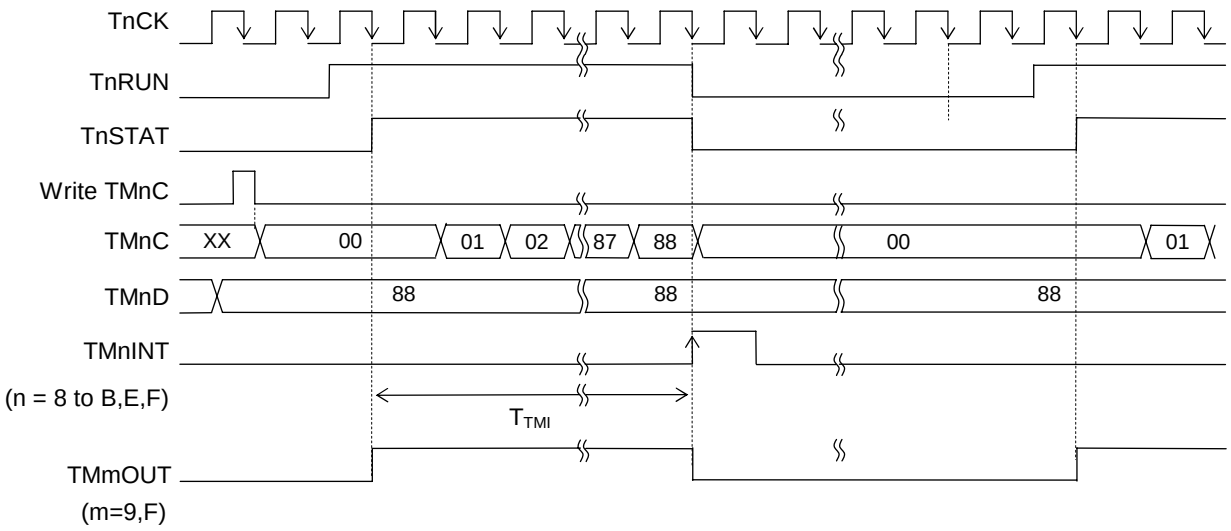
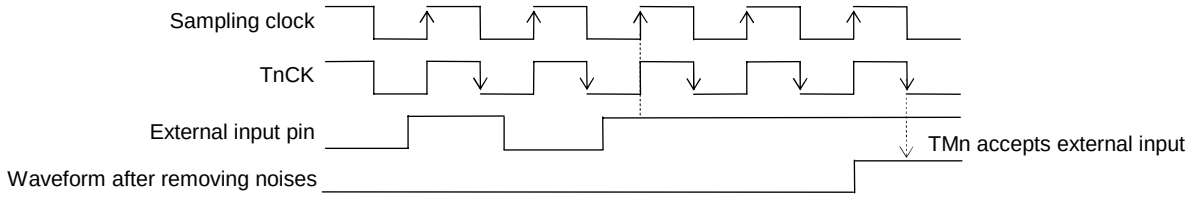


Figure 8-3 One-shot timer mode Operation Timing Diagram of Timer 8 to B,E,F

Note:
When the count value of TMnC and the value of a timer 8 to B,E,F data register (TMnD) are matched, a TnRUN bit is cleared automatically.

8.3.2 The external timer start/stop operation

For the external timer start/stop operation of the timer E,F, the external timer start/stop is enabled when the external input is selected on timer control register 2(TMnCON2) and the timer control register 3(TMnCON3) and TnTGEN bit of timer control register 1(TMnCON1) is set as "1".
Set the input pulse width to equal to or more three sampling clocks as the external input is sampled at timer clock (TnCK). From the external input, pulses shorter than one sampling clock are removed as noises, and pulses of 1 to 3 sampling clock may not be removed or be removed.



8.3.3 The external timer operation

For the external timer start/stop operation of the timer E,F, the external timer start/stop is enabled when the external input is selected on timer control register 2(TMnCON2) and the timer control register 3(TMnCON3) and TnTGEN bit of timer control register 1(TMnCON1) is set as "1". If the rising or falling of an external input pin occur in this state, the TnRUN bit of the timer control register 1 (TMnCON1) will be set to "1" by hardware.The timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer E,F control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.

When the count value of TMnC and the timer E,F data register (TMnD) coincide, timer E,F interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing. When stop timer by an external input is selected, if the rising edge/falling edge of the external input selected by TMnCON2 happen, TMnINT will be generated in the falling edge of the next timer clock, and the counting of TMnC will be stopped.

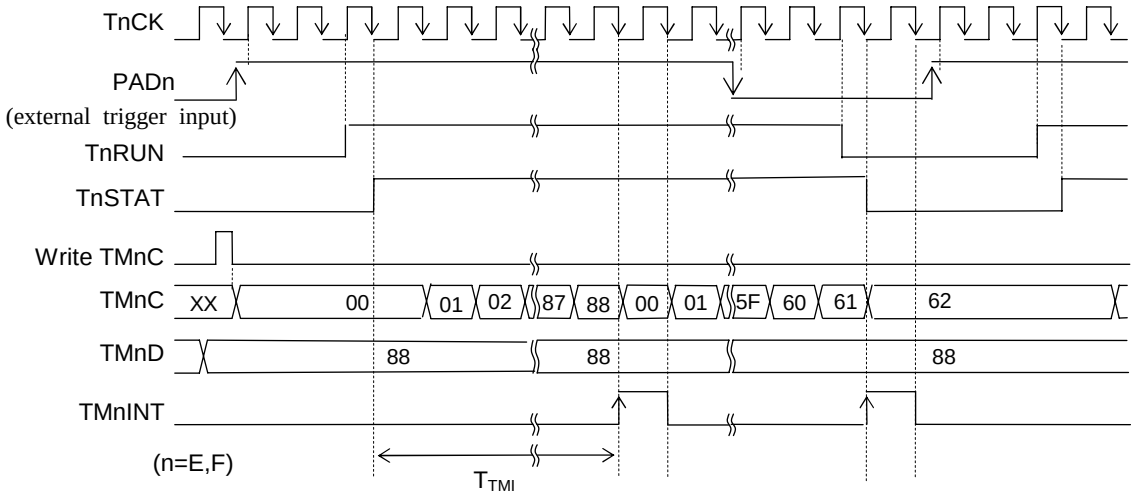


Figure 8-4(a) Normal mode Operation Timing Diagram of Timer E,F

**(timer count is started by the external input rising edge,
timer count is stopped by the external input falling edge.)**

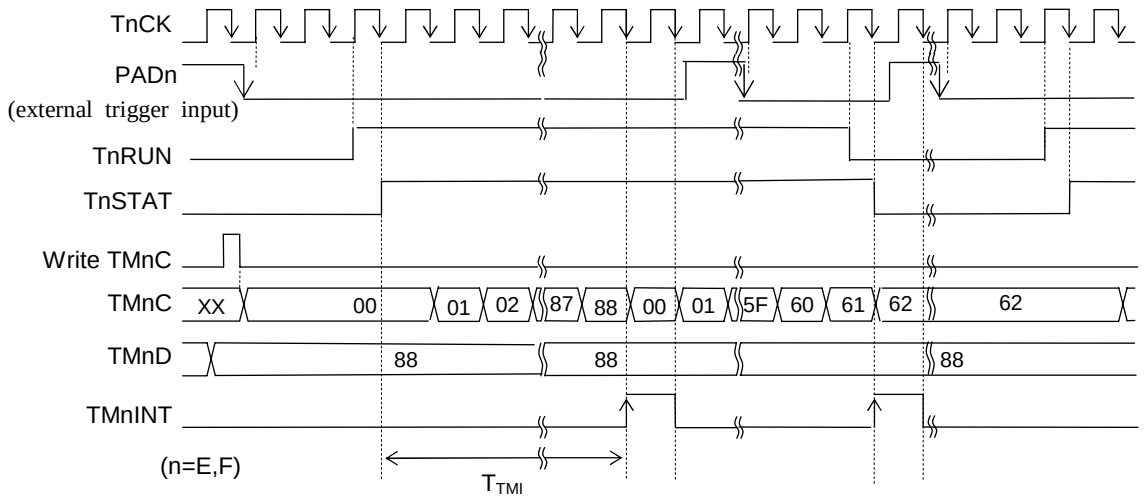


Figure 8-4(b) Normal mode Operation Timing Diagram of Timer E,F

**(timer count is started by the external input falling edge,
timer count is stopped by the external input falling edge.)**

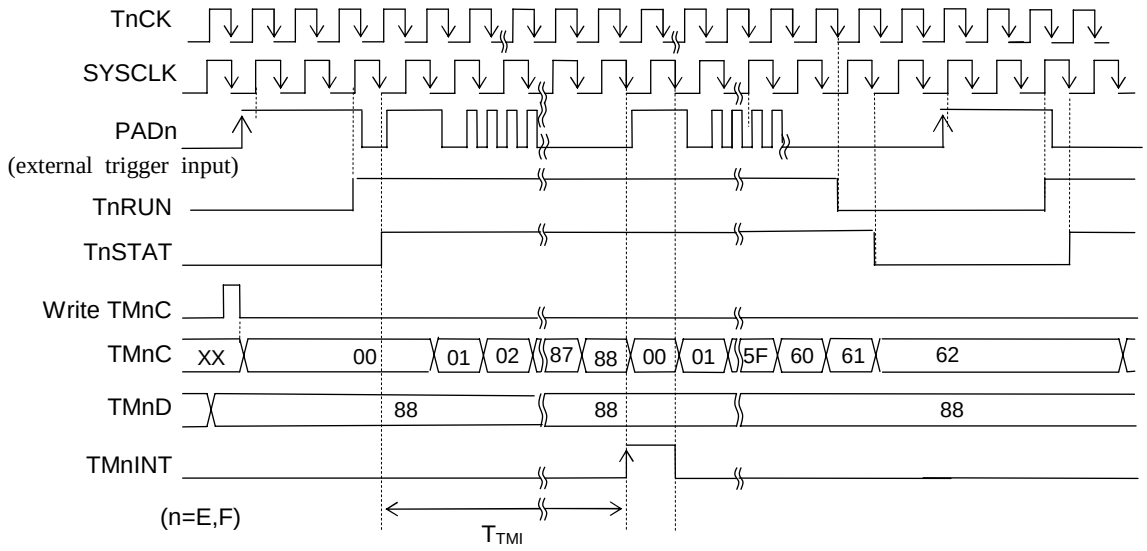


Figure 8-4(c) Normal mode Operation Timing Diagram of Timer E,F

**(timer count is started by the external input rising edge,
timer count is stopped by software.)**

Note:
Although "0" is written in TnRUN, since TnSTAT continues a counting operation to the falling edge of the next timer clock in the status of "1", TMnINT may occur.

8.4 Specifying port registers

For enable the timer output (TM9OUT, TMFOUT) function, each related port register needs to be set up. Refer to the Chapter 15, "Port A" , the Chapter 16 "Port B" and Chapter 17, "Port C" for details of each register.

8.4.1 Functioning PA0 (TM9OUT) as the timer output

Set PA0MD1 bit (bit0 of PAMOD1 register) to "1" and PA0MD0 bit (bit0 of PAMOD0 register) to "1" for specifying the timer output as the quaternary function of PA0.

Reg. name	PAMOD1 register (Address: 0F255H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2MD1	PA1MD1	**PA0MD1**
Data	—	—	—	—	—	*	*	**1**

Reg. name	PAMOD0 register (Address: 0F254H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2MD0	PA1MD0	**PA0MD0**
Data	—	—	—	—	—	*	*	**1**

Set PA0C1 bit (bit0 of PACON1 register) to "1" and set PA0C0 bit(bit0 of PACON0 register) to "1", and set PA0DIR bit(bit0 of PADIR register) to "0" for specifying the PA0 as CMOS output.

Reg. name	PACON1 register (Address: 0F253H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2C1	PA1C1	**PA0C1**
Data	—	—	—	—	—	*	*	**1**

Reg. name	PACON0 register (Address: 0F252H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2C0	PA1C0	**PA0C0**
Data	—	—	—	—	—	*	*	**1**

Reg. name	PADIR register (Address: 0F251H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2DIR	PA1DIR	**PA0DIR**
Data	—	—	—	—	—	*	*	**0**

Data of PA0D bit (bit0 of PAD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PAD register (Address: 0F250H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2D	PA1D	**PA0D**
Data	—	—	—	—	—	*	*	**

- : Bit does not exist.
* : Bit not related to the timer function
** : Don't care the data.

8.4.2 Functioning PC3 (TMFOUT) as the timer output

Set PC3MD1 bit (bit3 of PCMOD1 register) to "1" and PC7MD0 bit (bit3 of PCMOD0 register) to "1" for specifying the timer output as the quaternary function of PC3.

Reg. name	PCMOD1 register (Address: 0F265H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7MD1	PC6MD1	PC5MD1	PC4MD1	**PC3MD1**	PC2MD1	PC1MD1	PC0MD1
Data	*	*	*	*	**1**	*	*	*

Reg. name	PCMOD0 register (Address: 0F264H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7MD0	PC6MD0	PC5MD0	PC4MD0	**PC3MD0**	PC2MD0	PC1MD0	PC0MD0
Data	*	*	*	*	**1**	*	*	*

Set PC3C1 bit (bit3 of PCCON1 register) to "1" and set PC3C0 bit(bit3 of PCCON0 register) to "1", and set PC3DIR bit(bit3 of PCDIR register) to "0" for specifying the PC3 as CMOS output.

Reg. name	PCCON1 register (Address: 0F263H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7C1	PC6C1	PC5C1	PC4C1	**PC3C1**	PC2C1	PC1C1	PC0C1
Data	*	*	*	*	**1**	*	*	*

Reg. name	PCCON0 register (Address: 0F262H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7C0	PC6C0	PC5C0	PC4C0	**PC3C0**	PC2C0	PC1C0	PC0C0
Data	*	*	*	*	**1**	*	*	*

Reg. name	PCDIR register (Address: 0F261H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7DIR	PC6DIR	PC5DIR	PC4DIR	**PC3DIR**	PC2DIR	PC1DIR	PC0DIR
Data	*	*	*	*	**0**	*	*	*

Data of PC3D bit (bit3 of PCD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PCD register (Address: 0F260H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	PC7D	PC6D	PC5D	PC4D	**PC3D**	PC2D	PC1D	PC0D
Data	*	*	*	*	******	*	*	*

- : Bit does not exist.
* : Bit not related to the timer function
** : Don't care the data.

Chapter 9

Watchdog Timer

9 Watchdog Timer

9.1 Overview

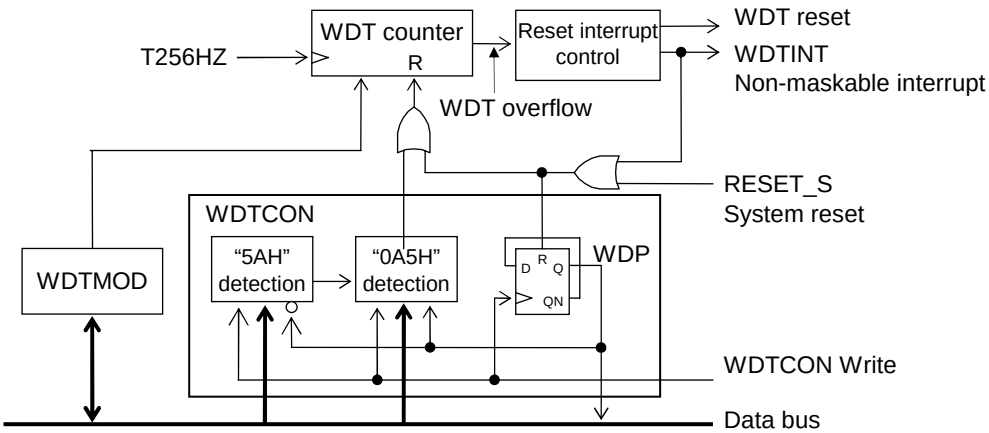
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, "Interrupts," and for WDT interrupt see Chapter 3, "Reset Function".

9.1.1 Features

- Free running (cannot be stopped)
- One of seven types of overflow periods (23.4ms, 31.25ms, 62.5ms, 125ms, 500ms, 2s, and 8s) selectable by software
- Non-maskable interrupt by the first overflow
- Reset generated by the second overflow

9.1.2 Configuration

Figure 9-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 9-1 Configuration of Watchdog Timer

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H

9.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. The WDP is reset to "0" at the system reset or the watchdog timer overflow and is inverted every writing to WDTCON.

- **d7-d0** (bits 7-0)
  This bit is used to write data to clear the WDT counter. Write "5AH" on the condition of WDP is "0" and write "0A5H" on the condition of WDP is "1".

Note:
When the WDT interrupt (WDTINT) occurs by the first WDT counter overflow, the counter and the internal pointer (WDP) are initialized for a half cycle of low speed clock (about 15.25us). During the time period that they are initialized, writing to WDTCON is disable and the logic of WDP does not change. Therefore, in the case of that you have program codes handle to clear the WDT when the first overflow WDT interrupt occurs and also the codes run at high-speed system clock, please check the WDP gets reversed after writing to WDTCON to see if the writing was surely successful. For example of the program code, see Section 9.3.1, "Handling example when you do not want to use the watchdog timer".

9.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: R/W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	—	—	—	—	—	WDT2	WDT1	WDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT2-0** (bits 2-0)

These bits are used to select an overflow period of the watchdog timer.
The WDT2, WDT1 and WDT0 bits set a overflow period (T_{WOV}) of the WDT counter. It is selectable from the following seven types of values.

WDT2	WDT1	WDT0	Description
0	0	0	125 ms
0	0	1	500 ms
0	1	0	2 s (initial value)
0	1	1	8 s
1	0	0	23.4 ms
1	0	1	31.25 ms
1	1	0	62. 5ms
1	1	1	Prohibited

Note:
When you perfome erase of a data-flash memory rewriting function, set WDT2-0 as either of "000b" to "011b".
Clear the WDT counter before chainging WDT-overflow-period.

9.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
Write "5AH" when the internal pointer (WDP) is "0" and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (T_{WOV}) of the WDT counter, it is selectable from the following seven types of values by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 9-1.

Table 9-1 Clear Period of WDT Counter

WDT2	WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	0	125 ms	Approx. 121 ms
0	0	1	500 ms	Approx. 496 ms
0	1	0	2000 ms	Approx. 1996 ms
0	1	1	8000 ms	Approx. 7996 ms
1	0	0	23.4 ms	Approx. 19.4 ms
1	0	1	31.25 ms	Approx. 27.25 ms
1	1	0	62.5 ms	Approx. 58.5 ms
1	1	1	Prohibited	Prohibited

Figure 9-2 shows an example of watchdog timer operation.

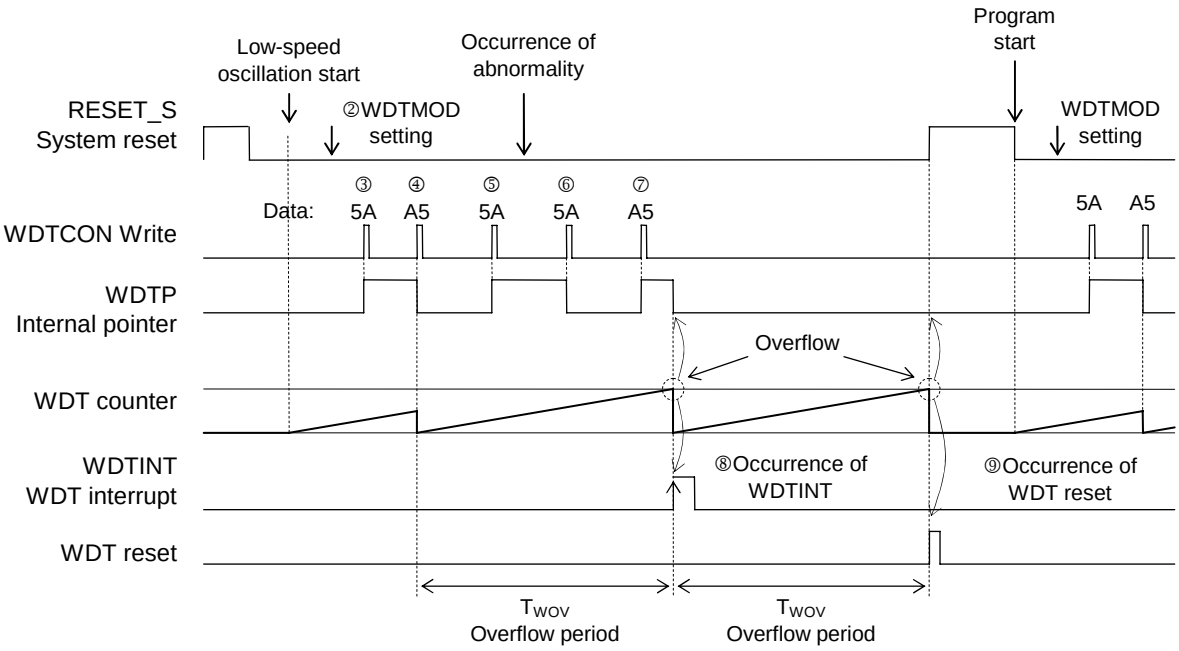


Figure 9-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
③ "5AH" is written to WDTCON. (Internal pointer 0→1)
④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1→0)
⑤ "5AH" is written o WDTCON. (Internal pointer 0→1)
⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1→0)
⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in ⑥. (Internal pointer 0→1)
⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case,, the WDT counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.26us).
⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Note:
– In STOP mode, the watchdog timer operation also stops.
– In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
– The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

9.3.1 Handling example when you do not want to use the watchdog timer

WDT counter is a free-run counter that starts count-up automatically after the system reset released and the low-speed clock (LSCLK) starts oscillating. If the WDT counter gets overflow, the WDT non-maskable interrupt occurs and then a system reset occurs. Therefore, it is needed to clear the WDT counter even if you do not want to use the WDT as a fail-safe function.
See following example programming codes to clear the WDT counter in the interrupt routine.

Example programming code:

```
__DI();                    // Disable multi-interrupts
do
{
   WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
__EI();
```

Chapter 10

PWM

10 PWM

10.1 Overview

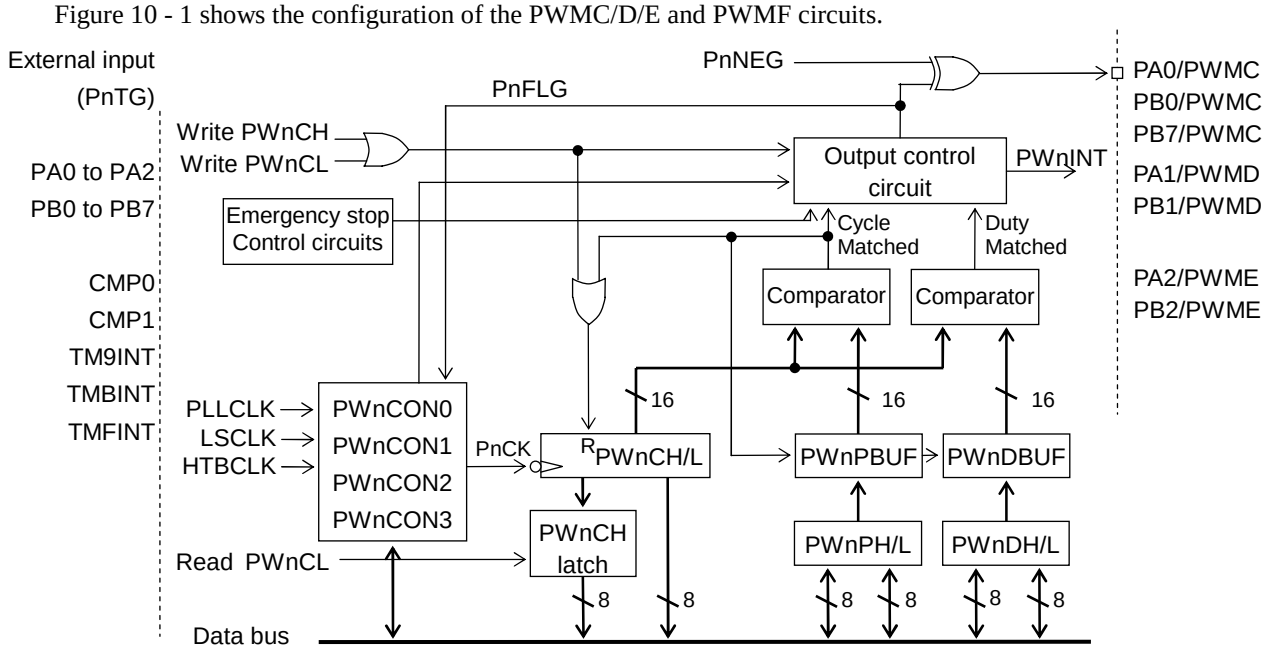
This LSI includes 4 channels of 16-bit PWM (Pulse Width Modulation).
The PWM output (PWMC) function is assigned to the secondary function of the PA0(Port A) or the secondary function of the PB0(Port B) or the fourthly function of the PB7(Port B).
The PWM output (PWMD) function is assigned to the secondary function of the PA1(Port A) or the secondary function of the PB1(Port B).
The PWM output (PWME) function is assigned to the secondary function of the PA2(Port A) or the secondary function of the PB2(Port B).
The PWM output (PWMF) can output three types of PWM with the same period and different duties, and PWMF0 output (PWMF0) function is assigned to the tertiary function of the PB7 (Port B) or PC0 (Port C), and PWMF1 output (PWMF1) function is assigned to the fourthly function of the PB6 (Port B) or the tertiary function of the PC1 (Port C), and PWMF2 output (PWMF2) is assigned to the fourthly function of the PB5 (Port B) or the tertiary function of the PC2 (Port C).
For the functions of port A, port B and port C, see Chapter 15, "Port A", Chapter 16, "Port B" and Chapter 17, "Port C".

10.1.1 Features

- The PWM signals with the periods of approximately 122 ns (@PLLCLK=16.384MHz) to 2s (@LSCLK=32.768kHz) can be generated and output outside of the LSI.
- The output logic of the PWM signal can be switched to the positive or negative logic.
- A PWM interruption (PWnINT) is caused at the time of a cycle & duty match at the time of a duty match at the time of a cycle match of a PWM signal.
- For the PWM clock, a low-speed clock (LSCLK), and a high-speed time base clock (HTBCLK), and a PLL oscillating clock (PLLCLK) are available.
- Supports one shot mode
- PWM start/stop can be controlled by the external input (an LSI pin, timer interrupt request, or comparator output can be selected as the external input. However, the minimum pulse width of the external input by the LSI pin is PWM clock 3ϕ.)
- An external input can generate an emergency stop and emergency stop interrupt.
- PWMF can output three types of PWM with the same period and different duties.

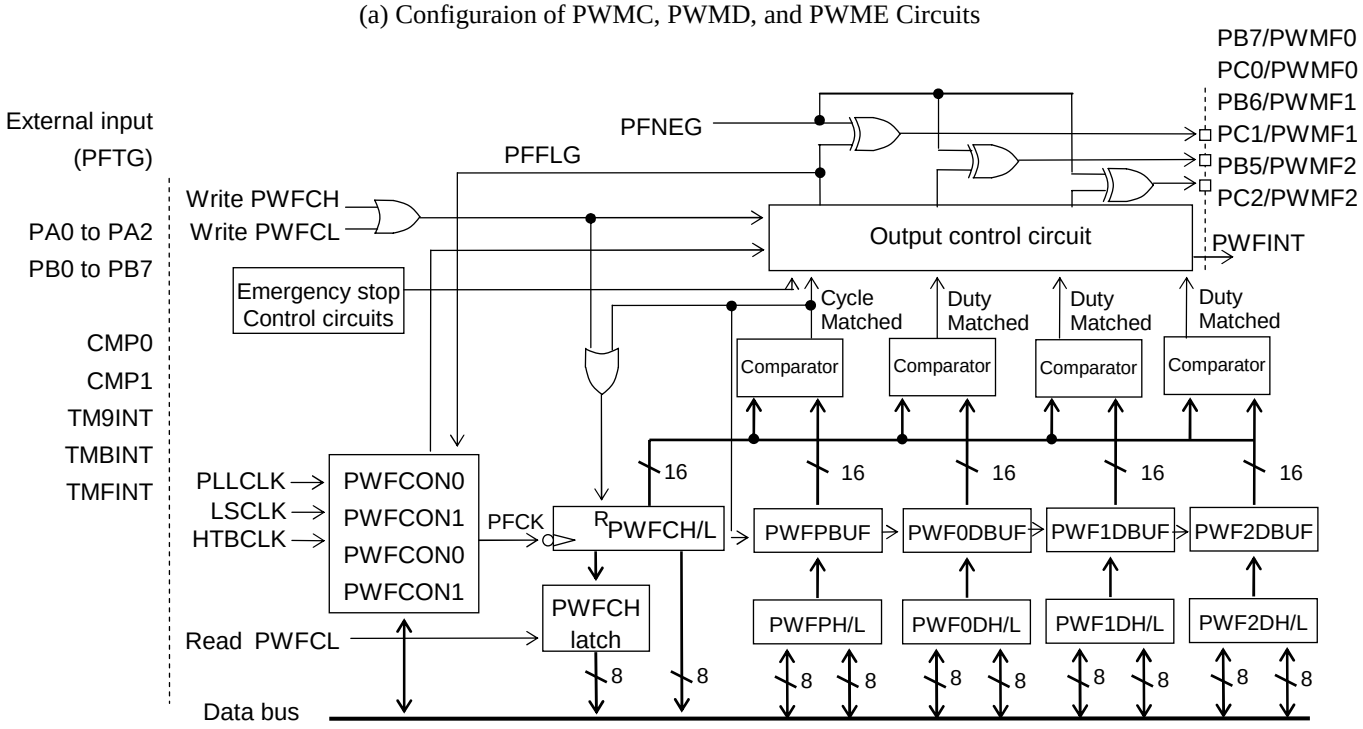
10.1.2 Configuration

Figure 10 - 1 shows the configuration of the PWMC/D/E and PWMF circuits.



PWnPL/H: PWMn period register L/H
PWnDL/H: PWMn duty register L/H
PWnCL: PWMn counter register L/H
PWnCON0/1/2/3: PWMn control register 0/1/2/3
PWnPBUF: PWMn period buffer
PWnDBUF: PWMn duty buffer
(n = C, D, E)

(a) Configuraion of PWMC, PWMD, and PWME Circuits



PWFPL/H: PWMF period register L/H
PWFmDL/H: PWMFm duty register L/H
PWFCL/H: PWMF counter register L/H
PWFCON0-5: PWMF control register 0-5
PWFPBUF: PWMF period buffer
PWFmDBUF: PWMFm duty buffer
(m = 0, 1, 2)

(b) Configuraion of PWMF Circuit

Figure 10-1 Configuration of PWM Circuit

10.1.3 List of Pins

Pin name	I/O	Description
PA0/ PnTG/ PWMC	I/O	External trigger input PWMC output pin: Used for the secondary function of the PA0 pin.
PA1/ PnTG/ PWMD	I/O	External trigger input PWMD output pin: Used for the secondary function of the PA1 pin.
PA2/ PnTG/ PWME	I/O	External trigger input PWME output pin: Used for the secondary function of the PA2 pin.
PB0/ PnTG/ PWMC	I/O	External trigger input Emergency stop input PWMC output pin: Used for the secondary function of the PB0 pin.
PB1/ PnTG/ PWMD	I/O	External trigger input PWMD output pin: Used for the secondary function of the PB1 pin.
PB2/ PnTG/ PWME	I/O	External trigger input PWME output pin: Used for the secondary function of the PB2 pin.
PB3/ PnTG	I	External trigger input
PB4/ PnTG	I	External trigger input
PB5/ PnTG/ PWMF2	I/O	External trigger input PWMF2 output pin: Used for the fourthly function of the PB5 pin.
PB6/ PnTG/ PWMF1	I/O	External trigger input PWMF1 output pin: Used for the fourthly function of the PB6 pin.
PB7/ PnTG/ PWMC/ PWMF0	I/O	External trigger input PWMF0 output pin: Used for the tertiary function of the PB7 pin. PWMC output pin: Used for the fourthly function of the PB7 pin.
PC0/ PWMF0	O	PWMF0 output pin: Used for the tertiary function of the PC0 pin.
PC1/ PWMF1	O	PWMF1 output pin: Used for the tertiary function of the PC1 pin.
PC2/ PWMF2	O	PWMF2 output pin: Used for the tertiary function of the PC2 pin.

(n = C, D, E, F)

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F910H	PWMC period register L	PWCPL	PWCP	R/W	8/16	0FFH
0F911H	PWMC period register H	PWCPH		R/W	8	0FFH
0F912H	PWMC duty register L	PWCDL	PWCD	R/W	8/16	00H
0F913H	PWMC duty register H	PWCDH		R/W	8	00H
0F914H	PWMC counter register L	PWCCL	PWCC	R/W	8/16	00H
0F915H	PWMC counter register H	PWCCH		R/W	8	00H
0F916H	PWMC control register 0	PWCCON0	PWCCON	R/W	8/16	00H
0F917H	PWMC control register 1	PWCCON1		R/W	8	00H
0F918H	PWMC control register 2	PWCCON2	PWCCON23	R/W	8/16	00H
0F919H	PWMC control register 3	PWCCON3		R/W	8	00H
0F920H	PWMD period register L	PWDPL	PWDP	R/W	8/16	0FFH
0F921H	PWMD period register H	PWDPH		R/W	8	0FFH
0F922H	PWMD duty register L	PWDDL	PWDD	R/W	8/16	00H
0F923H	PWMD duty register H	PWDDH		R/W	8	00H
0F924H	PWMD counter register L	PWDCL	PWDC	R/W	8/16	00H
0F925H	PWMD counter register H	PWDCH		R/W	8	00H
0F926H	PWMD control register 0	PWDCON0	PWDCON	R/W	8/16	00H
0F927H	PWMD control register 1	PWDCON1		R/W	8	00H
0F928H	PWMD control register 2	PWDCON2	PWDCON23	R/W	8/16	00H
0F929H	PWMD control register 3	PWDCON3		R/W	8	00H
0F930H	PWME period register L	PWEPL	PWEP	R/W	8/16	0FFH
0F931H	PWME period register H	PWEPH		R/W	8	0FFH
0F932H	PWME duty register L	PWEDL	PWED	R/W	8/16	00H
0F933H	PWME duty register H	PWEDH		R/W	8	00H
0F934H	PWME counter register L	PWECL	PWEC	R/W	8/16	00H
0F935H	PWME counter register H	PWECH		R/W	8	00H
0F936H	PWME control register 0	PWECON0	PWECON	R/W	8/16	00H
0F937H	PWME control register 1	PWECON1		R/W	8	00H
0F938H	PWME control register 2	PWECON2	PWECON23	R/W	8/16	00H
0F939H	PWME control register 3	PWECON3		R/W	8	00H
0F960H	PWMF period register L	PWFPL	PWFP	R/W	8/16	0FFH
0F961H	PWMF period register H	PWFPH		R/W	8	0FFH
0F962H	PWMF0 duty register L	PWF0DL	PWF0D	R/W	8/16	00H
0F963H	PWMF0 duty register H	PWF0DH		R/W	8	00H
0F964H	PWMF1 duty register L	PWF1DL	PWF1D	R/W	8/16	00H
0F965H	PWMF1 duty register H	PWF1DH		R/W	8	00H
0F966H	PWMF2 duty register L	PWF2DL	PWF2D	R/W	8/16	00H
0F967H	PWMF2 duty register H	PWF2DH		R/W	8	00H
0F970H	PWMF counter register L	PWFCL	PWFC	R/W	8/16	00H
0F971H	PWMF counter register H	PWFCH		R/W	8	00H
0F972H	PWMF control register 0	PWFCON0	PWFCON	R/W	8/16	00H
0F973H	PWMF control register 1	PWFCON1		R/W	8	00H
0F974H	PWMF control register 2	PWFCON2	PWFCON23	R/W	8/16	00H
0F975H	PWMF control register 3	PWFCON3		R/W	8	00H
0F976H	PWMF control register 4	PWFCON4	PWFCON45	R/W	8/16	10H
0F977H	PWMF control register 5	PWFCON5		R/W	8	00H

10.2.2 PWMC Period Registers (PWCPL, PWCPH)

Address: 0F910H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWCPL	PCP7	PCP6	PCP5	PCP4	PCP3	PCP2	PCP1	PCP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F911H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWCPH	PCP15	PCP14	PCP13	PCP12	PCP11	PCP10	PCP9	PCP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PWCPH and PWCPL are special function registers (SFRs) to set the PWMC periods.

Note:
When PWCPH or PWCPL is set to "0000H", the PWMC period buffer (PWCPBUF) is set to "0001H".
For PWCPH and PWCPL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.3 PWMC Duty Registers (PWCDL, PWCDH)

Address: 0F912H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCDL	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F913H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCDH	PCD15	PCD14	PCD13	PCD12	PCD11	PCD10	PCD9	PCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCDH and PWCDL are special function registers (SFRs) to set the duties of PWMC.

Note:
Set PWCDH and PWCDL to values smaller than those to which PWCPH and PWCPL are set.
For PWCDH and PWCDL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.4 PWMC Counter Registers (PWCCH, PWCCL)

Address: 0F914H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCL	PCC7	PCC6	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F915H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCH	PCC15	PCC14	PCC13	PCC12	PCC11	PCC10	PCC9	PCC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCCL and PWCCH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PWCCL or PWCCH, PWCCL and PWCCH is set to "0000H". The data that is written is meaningless. Operate this access while the PWM is stopped.
When data is read from PWCCL, the value of PWCCH is latched. When reading PWCCH and PWCCL, use a word type instruction or pre-read PWCCL.

The contents of PWCCH and PWCCL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 10-1 shows PWCCH and PWCCL read enable/disable for each combination of the PWM clock and system clock.

Table 10-1 PWCCH and PWCCL Read Enable/Disable during PWMC Operation

PWM clock PCCK	System clock SYSCLK	PWCCH and PWCCL read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PWCCH or PWCCL twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
	HSCLK	Read enabled
PLLCLK (16.384MHz)	LSCLK	Read disabled
	HSCLK	

10.2.5 PWMC Control Register 0 (PWCCON0)

Address: 0F916H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON0	—	—	PCSDN	PCNEG	PCIS1	PCIS0	PCCS1	PCCS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCCON0 is a special function register (SFR) to control PWM.
Rewrite bit 0 to 4 of PWCCON0 while the PWMC is stopped (PCRUN, PCTGEN and PCSTAT of the PWCCON1 register is "0").

[Description of Bits]

- **PCCS1, PCCS0** (bits 1, 0)
  The PCCS1 and PCCS0 bits are used to select the PWMC operation clocks. LSCLK, HTBCLK, or PLLCLK can be selected.

PCCS1	PCCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	PLLCLK (16.384MHz)
1	1	Prohibited

- **PCIS1, PCIS0** (bits 3, 2)
  The PCIS1 and PCIS0 bits are used to select the point at which the PWMC interrupt occurs. "When the periods match", "when the duties match", or "when the periods and duties match" can be selected.

PCIS1	PCIS0	Description
0	0	When the periods matched. (initial value)
0	1	When the duties matched.
1	*	When the periods and duties matched.

- **PCNEG** (bit 4)
  The PCNEG bit is used to select the output logic. When PCNEG="0", the initial value of PWMC output is "0", and when PCNEG="1", it is "1".

PCNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **PCSDN** (bit 5)
  The PCSDN bit is used to select the forced stop of PWMC. If "1" is written to the register, the output of PWMC is fixed to the value set by PCNEG register.

PCSDN	Description
0	PWMC normal operation (initial value)
1	PWMC forced stop

10.2.6 PWMC Control Register 1 (PWCCON1)

Address: 0F917H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON1	PCSTAT	PCFLG	PCSDST	—	—	—	PCTGEN	PCRUN
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCCON1 is a special function register (SFR) to control PWMC.

[Description of Bits]

- **PCRUN** (bit 0)
  The PCRUN bit is used to control count stop/start of PWMC.

PCRUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

- **PCTGEN** (bit 1)
  The PCTGEN is a enable flag of the count stop/start and emergency stop by the external input of PWMC.
  An interrupt occurs when the count stops by the external input.

PCTGEN	Description
0	Disables the count stop/start and the emergency stop by the external input. (initial value)
1	Enables the count stop/start and the emergency stop by the external input.

- **PCSDST** (bit 5)
  The PCSDST bit indicates that an emergency stop interrupt has occurred.
  Write "1" to this bit to clear it.

PCSDST	Description
0	An emergency stop interrupt has not occurred. (initial value)
1	An emergency stop interrupt has occurred.

- **PCFLG** (bit 6)
  The PCFLG bit is used to read the output flag of PWMC.

PCFLG	Description
0	PWMC output flag = "0" (initial value)
1	PWMC output flag = "1"

- **PCSTAT** (bit 7)
  The PCSTAT bit indicates "counting stopped or "counting in progress" of PWMC.

PCSTAT	Description
0	Counting stopped. (initial value)
1	Counting in progress.

Note:
When the PWM count is stopped by the external trigger and PCRUN bit shows "0", make sure to start the next operation after PCSTAT bit shows "0" as the PWM count is stopped.
For confirmation of the interrupt, see 10.3.4 "Interrupt of PWM".

10.2.7 PWMC Control Register 2 (PWCCON2)

Address: 0F918H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON2	PCOST	—	PCTRM1	PCTRM0	—	PCEXCL	PCST1	PCST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCCON2 is a special function register (SFR) to control PWM.
Rewrite PWCCON2 while the PWMC is stopped (PCRUN, PCTGEN and PCSTAT of the PWCCON1 register is "0").

[Description of Bits]

- **PCST1, PCST0** (bits 1, 0)

The PCST1 and PCST0 bits are used to select the start/stop mode of the PWMC counter.

PCST1	PCST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **PCEXCL** (bit 2)

The PCEXCL bit is used to select whether or not to clear the PWMC counter when stopped by the external input (PCST1 is set to "1"). Set PCEXCL to "1" to clear the counter when stopped by the external input.

PCEXCL	Description
0	Does not clear the counter when it is stopped by the external trigger. (initial value)
1	Clears the counter when it is stopped by the external trigger.

- **PCTRM1, PCTRM0** (bits 5, 4)

The PCTRM1 and PCTRM0 bits are used to select the count start/stop mode of PWMC.
This is valid only when the external input start and stop are selected.

PCTRM1	PCTRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

Note:
When the timer interrupt (TM9INT/TMBINT/TMFINT) is selected for the external input with the PWCCON3 register, be sure to select the rising edge start and the rising edge stop (set PCTRM1 to "0" and PCTRM0 "0"). Do not use other settings (The operation cannot be guaranteed because they may cause the count start/stop at timings other than interrupts).

- **PCOST** (bit 7)

The PCOST bit is used for the operation mode of the PWMC.

PCOST	Description
0	One-shot mode disabled (initial value)
1	One-shot mode enabled

10.2.8 PWMC Control Register 3 (PWCCON3)

Address: 0F919H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON3	—	—	PCSDE1	PCSDE0	PCSTSS	PCSTS2	PCSTS1	PCSTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWCCON3 is a special function register (SFR) to control PWM.
Rewrite PWCCON3 while the PWMC is stopped (PCRUN, PCTGEN and PCSTAT of the PWCCON1 register is "0").

[Description of Bits]

- **PCSTSS, PCSTS2, PCSTS1, PCSTS0** (bits 3 to 0)

The PCSTSS, PCSTS2, PCSTS1, and PCSTS0 bits are used to select the external input start/stop pins of PWMC.

PCSTS2	PCSTS1	PCSTS0	Description	
			When PCSTSS="0" (initial value)	When PCSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0 (Comparator 0)	PB3 pin
1	0	0	CMP1 (Comparator 1)	PB4 pin
1	0	1	TM9INT (Timer 9 interrupt)	PB5 pin
1	1	0	TMBINT (Timer B interrupt)	PB6 pin
1	1	1	TMFINT (Timer F interrupt)	PB7 pin

Note:
When a timer interrupt request is set as the external trigger signal, there are some restrictions on the edge selection of the PWM start/stop triggers. For details, see the description of the PWCCON2 register.
The timer interrupt requests (TM9INT/TMBINT/TMFINT) are interrupt request signals from the timer 9/timer B/timer F, independent of the interrupt enable/disable settings by the interrupt enable registers 3/5 (IE3/5).

- **PCSDE1, PCSDE0** (bits 5 to 4)

The PSDE1, PSDE0 bits are used to select the emergency stop input pins of PWMC.

PCSDE1	PCSDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge of the CMP0 (Comparator 0)
1	0	Rising edge of the CMP1 (Comparator 1)
1	1	Rising edge of PB0

Note:
The external trigger input pin and the emergency stop input pins aren't to select the same pin. When it is selected, PWM doesn't operate.

10.2.9 PWMD Period Registers (PWDPL, PWDPH)

Address: 0F920H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWDPL	PDP7	PDP6	PDP5	PDP4	PDP3	PDP2	PDP1	PDP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F921H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWDPH	PDP15	PDP14	PDP13	PDP12	PDP11	PDP10	PDP9	PDP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PWDPH and PWDPL are special function registers (SFRs) to set the PWMD periods.

Note:
When PWDPH or PWDPL is set to "0000H", the PWMD period buffer (PWDPBUF) is set to "0001H".
For PWDPH and PWDPL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.10 PWMD Duty Registers (PWDDL, PWDDH)

Address: 0F922H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDDL	PDD7	PDD6	PDD5	PDD4	PDD3	PDD2	PDD1	PDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F923H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDDH	PDD15	PDD14	PDD13	PDD12	PDD11	PDD10	PDD9	PDD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDDH and PWDDL are special function registers (SFRs) to set the duties of PWMD.

Note:
Set PWDDH and PWDDL to values smaller than those to which PWDPH and PWDPL are set.
For PWDDH and PWDDL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.11 PWMD Counter Registers (PWDCH, PWDCL)

Address: 0F924H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCL	PDC7	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F925H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCH	PDC15	PDC14	PDC13	PDC12	PDC11	PDC10	PDC9	PDC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDCL and PWDCH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PWDCL or PWDCH, PWDCL and PWDCH is set to "0000H". The data that is written is meaningless. Operate this access while the PWM is stopped.
When data is read from PWDCL, the value of PWDCH is latched. When reading PWDCH and PWDCL, use a word type instruction or pre-read PWDCL.

The contents of PWDCH and PWDCL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 10-2 shows PWDCH and PWDCL read enable/disable for each combination of the PWM clock and system clock.

Table 10-2 PWDCH and PWDCL Read Enable/Disable during PWMD Operation

PWM clock PDCK	System clock SYSCLK	PWDCH and PWDCL read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PWDCH or PWDCL twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
	HSCLK	Read enabled
PLLCLK (16.384MHz)	LSCLK	Read disabled
	HSCLK	

10.2.12 PWMD Control Register 0 (PWDCON0)

Address: 0F926H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCON0	—	—	PDSDN	PDNEG	PDIS1	PDIS0	PDCS1	PDCS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDCON0 is a special function register (SFR) to control PWM.
Rewrite bit 0 to 4 of PWDCON0 while the PWMD is stopped (PDRUN, PDTGEN and PDSTAT of the PWDCON1 register is "0").

[Description of Bits]

- **PDCS1, PDCS0** (bits 1, 0)
  The PDCS1 and PDCS0 bits are used to select the PWMD operation clocks. LSCLK, HTBCLK, or PLLCLK can be selected.

PDCS1	PDCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	PLLCLK (16.384MHz)
1	1	Prohibited

- **PDIS1, PDIS0** (bits 3, 2)
  The PDIS1 and PDIS0 bits are used to select the point at which the PWMD interrupt occurs. "When the periods match", "when the duties match", or "when the periods and duties match" can be selected.

PDIS1	PDIS0	Description
0	0	When the periods matched. (initial value)
0	1	When the duties matched.
1	*	When the periods and duties matched.

- **PDNEG** (bit 4)
  The PDNEG bit is used to select the output logic. When PDNEG="0", the initial value of PWMD output is "0", and when PDNEG="1", it is "1".

PDNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **PDSDN** (bit 5)
  The PDSDN bit is used to select the forced stop of PWMD. If "1" is written to the register, the output of PWMD is fixed to the value set by PDNEG register.

PDSDN	Description
0	PWMD normal operation (initial value)
1	PWMD forced stop

10.2.13 PWMD Control Register 1 (PWDCON1)

Address: 0F927H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCON1	PDSTAT	PDFLG	PDSDST	—	—	—	PDTGEN	PDRUN
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDCON1 is a special function register (SFR) to control PWMD.

[Description of Bits]

- **PDRUN** (bit 0)
  The PDRUN bit is used to control count stop/start of PWMD.

PDRUN	Description
0	Stops counting. (initial value)
1	Starts counting.

- **PDTGEN** (bit 1)
  The PDTGEN is a enable flag of the count stop/start and emergency stop by the external input of PWMD.
  An interrupt occurs when the count stops by the external input.

PDTGEN	Description
0	Disables the count stop/start and the emergency stop by the external input. (Initial value)
1	Enables the count stop/start and the emergency stop by the external input.

- **PDSDST** (bit 5)
  The PDSDST bit indicates that an emergency stop interrupt has occurred.
  Write "1" to this bit to clear it.

PDSDST	Description
0	An emergency stop interrupt has not occurred. (initial value)
1	An emergency stop interrupt has occurred.

- **PDFLG** (bit 6)
  The PDFLG bit is used to read the output flag of PWMD.

PDFLG	Description
0	PWMD output flag = "0" (initial value)
1	PWMD output flag = "1"

- **PDSTAT** (bit 7)
  The PDSTAT bit indicates "counting stopped or "counting in progress" of PWMD.

PDSTAT	Description
0	Counting stopped. (initial value)
1	Counting in progress.

Note:
When the PWM count is stopped by the external trigger and PDRUN bit shows "0", make sure to start the next operation after PDSTAT bit shows "0" as the PWM count is stopped.
For confirmation of the interrupt, see 10.3.4 "Interrupt of PWM".

10.2.14 PWMD Control Register 2 (PWDCON2)

Address: 0F928H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCON2	PDOST	—	PDTRM1	PDTRM0	—	PDEXCL	PDST1	PDST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDCON2 is a special function register (SFR) to control PWM.
Rewrite PWDCON2 while the PWMD is stopped (PDRUN, PDTGEN and PDSTAT of the PWDCON1 register is "0").

[Description of Bits]

• **PDST1, PDST0** (bits 1, 0)
The PDST1 and PDST0 bits are used to select the start/stop mode of the PWMD counter.

PDST1	PDST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

• **PDEXCL** (bit 2)
The PDEXCL bit is used to select whether or not to clear the PWMD counter when stopped by the external input (PDST1 is set to "1"). Set PDEXCL to "1" to clear the counter when stopped by the external input.

PDEXCL	Description
0	Does not clear the counter when it is stopped by the external trigger. (initial value)
1	Clears the counter when it is stopped by the external trigger.

• **PDTRM1, PDTRM0** (bits 5, 4)
The PDTRM1 and PDTRM0 bits are used to select the count start/stop mode of PWMD.
This is valid only when the external input start and stop are selected.

PDTRM1	PDTRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

Note:
When the timer interrupt (TM9INT/TMBINT/TMFINT) is selected for the external input with the PWDCON3 register, be sure to select the rising edge start and the rising edge stop (set PDTRM1 to "0" and PDTRM0 "0"). Do not use other settings (The operation cannot be guaranteed because they may cause the count start/stop at timings other than interrupts).

• **PDOST** (bit 7)
The PDOST bit is used for the operation mode of the PWMD.

PDOST	Description
0	One-shot mode disabled (initial value)
1	One-shot mode enabled

10.2.15 PWMD Control Register 3 (PWDCON3)

Address: 0F929H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWDCON3	—	—	PDSDE1	PDSDE0	PDSTSS	PDSTS2	PDSTS1	PDSTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWDCON3 is a special function register (SFR) to control PWM.
Rewrite PWDCON3 while the PWMD is stopped (PDRUN, PDTGEN and PDSTAT of the PWDCON1 register is "0").

[Description of Bits]

- **PDSTSS, PDSTS2, PDSTS1, PDSTS0** (bits 3 to 0)

The PDSTSS, PDSTS2, PDSTS1, and PDSTS0 bits are used to select the external input start/stop pins of PWMD.

PDSTS2	PDSTS1	PDSTS0	Description	
			When PDSTSS="0" (initial value)	When PDSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0 (Comparator 0)	PB3 pin
1	0	0	CMP1 (Comparator 1)	PB4 pin
1	0	1	TM9INT (Timer 9 interrupt)	PB5 pin
1	1	0	TMBINT (Timer B interrupt)	PB6 pin
1	1	1	TMFINT (Timer F interrupt)	PB7 pin

Note:
When a timer interrupt request is set as the external trigger signal, there are some restrictions on the edge selection of the PWM start/stop triggers. For details, see the description of the PWDCON2 register.
The timer interrupt requests (TM9INT/TMBINT/TMFINT) are interrupt request signals from the timer 9/timer B/timer F, independent of the interrupt enable/disable settings by the interrupt enable registers 3/5 (IE3/5).

- **PDSDE1, PDSDE0** (bits 5 to 4)

The PDSDE1, PDSDE0 bits are used to select the emergency stop input pins of PWMD.

PDSDE1	PDSDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge of the CMP0 (Comparator 0)
1	0	Rising edge of the CMP1 (Comparator 1)
1	1	Rising edge of PB0

Note:
The external trigger input pin and the emergency stop input pins aren't to select the same pin. When it is selected, PWM doesn't operate.

10.2.16 PWME Period Registers (PWEPL, PWEPH)

Address: 0F930H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWEPL	PEP7	PEP6	PEP5	PEP4	PEP3	PEP2	PEP1	PEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F931H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWEPH	PEP15	PEP14	PEP13	PEP12	PEP11	PEP10	PEP9	PEP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PWEPH and PWEPL are special function registers (SFRs) to set the PWME periods.

Note:
When PWEPH or PWEPL is set to "0000H", the PWME period buffer (PWEPBUF) is set to "0001H".
For PWEPH and PWEPL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.17 PWME Duty Registers (PWEDL, PWEDH)

Address: 0F932H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWEDL	PED7	PED6	PED5	PED4	PED3	PED2	PED1	PED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F933H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWEDH	PED15	PED14	PED13	PED12	PED11	PED10	PED9	PED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWEDH and PWEDL are special function registers (SFRs) to set the duties of PWME.

Note:
Set PWEDH and PWEDL to values smaller than those to which PWEPH and PWEPL are set.
For PWEDH and PWEDL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.18 PWME Counter Registers (PWECH, PWECL)

Address: 0F934H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECL	PEC7	PEC6	PEC5	PEC4	PEC3	PEC2	PEC1	PEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F935H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECH	PEC15	PEC14	PEC13	PEC12	PEC11	PEC10	PEC9	PEC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWECL and PWECH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PWECL or PWECH, PWECL and PWECH is set to "0000H". The data that is written is meaningless. Operate this access while the PWM is stopped.
When data is read from PWECL, the value of PWECH is latched. When reading PWECH and PWECL, use a word type instruction or pre-read PWECL.

The contents of PWECH and PWECL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 10-3 shows PWECH and PWECL read enable/disable for each combination of the PWM clock and system clock.

Table 10-3 PWECH and PWECL Read Enable/Disable during PWME Operation

PWM clock PECK	System clock SYSCLK	PWECH and PWECL read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PWECH or PWECL twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
	HSCLK	Read enabled
PLLCLK (16.384MHz)	LSCLK	Read disabled
	HSCLK	

10.2.19 PWME Control Register 0 (PWECON0)

Address: 0F936H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECON0	—	—	PESDN	PENEG	PEIS1	PEIS0	PECS1	PECS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWECON0 is a special function register (SFR) to control PWM.
Rewrite bit 0 to 4 of PWECON0 while the PWME is stopped (PERUN, PETGEN and PESTAT of the PWECON1 register is "0").

[Description of Bits]

- **PECS1, PECS0** (bits 1, 0)
  The PECS1 and PECS0 bits are used to select the PWME operation clocks. LSCLK, HTBCLK, or PLLCLK can be selected.

PECS1	PECS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	PLLCLK (16.384MHz)
1	1	Prohibited

- **PEIS1, PEIS0** (bits 3, 2)
  The PEIS1 and PEIS0 bits are used to select the point at which the PWME interrupt occurs. "When the periods match", "when the duties match", or "when the periods and duties match" can be selected.

PEIS1	PEIS0	Description
0	0	When the periods matched. (Initial value)
0	1	When the duties matched.
1	*	When the periods and duties matched.

- **PENEG** (bit 4)
  The PENEG bit is used to select the output logic. When PENEG="0", the initial value of PWME output is "0", and when PENEG="1", it is "1".

PENEG	Description
0	Positive logic (initial value)
1	Negative logic

- **PESDN** (bit 5)
  The PESDN bit is used to select the forced stop of PWME. If "1" is written to the register, the output of PWME is fixed to the value set by PENEG register.

PESDN	Description
0	PWME normal operation (initial value)
1	PWME forced stop

10.2.20 PWME Control Register 1 (PWECON1)

Address: 0F937H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECON1	PESTAT	PEFLG	PESDST	—	—	—	PETGEN	PERUN
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWECON1 is a special function register (SFR) to control PWME.

[Description of Bits]

• **PERUN** (bit 0)
The PERUN bit is used to control count stop/start of PWME.

PERUN	Description
0	Stops counting. (initial value)
1	Starts counting.

• **PETGEN** (bit 1)
The PETGEN is a enable flag of the count stop/start and emergency stop by the external input of PWME.
An interrupt occurs when the count stops by the external input.

PETGEN	Description
0	Disables the count stop/start and the emergency stop by the external input. (initial value)
1	Enables the count stop/start and the emergency stop by the external input.

• **PESDST** (bit 5)
The PESDST bit indicates that an emergency stop interrupt has occurred.
Write "1" to this bit to clear it.

PESDST	Description
0	An emergency stop interrupt has not occurred. (initial value)
1	An emergency stop interrupt has occurred.

• **PEFLG** (bit 6)
The PEFLG bit is used to read the output flag of PWME.

PEFLG	Description
0	PWME output flag = "0" (initial value)
1	PWME output flag = "1"

• **PESTAT** (bit 7)
The PESTAT bit indicates "counting stopped or "counting in progress" of PWME.

PESTAT	Description
0	Counting stopped. (initial value)
1	Counting in progress.

Note:
When the PWM count is stopped by the external trigger and PERUN bit shows "0", make sure to start the next operation after PESTAT bit shows "0" as the PWM count is stopped.
For confirmation of the interrupt, see 10.3.4 "Interrupt of PWM".

10.2.21 PWME Control Register 2 (PWECON2)

Address: 0F938H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECON2	PEOST	—	PETRM1	PETRM0	—	PEEXCL	PEST1	PEST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWECON2 is a special function register (SFR) to control PWME.
Rewrite PWECON2 while the PWME is stopped (PERUN, PETGEN and PESTAT of the PWECON1 register is "0").

[Description of Bits]

- **PEST1, PEST0** (bits 1, 0)

The PEST1 and PEST0 bits are used to select the start/stop mode of the PWME counter.

PEST1	PEST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **PEEXCL** (bit 2)

The PEEXCL bit is used to select whether or not to clear the PWME counter when stopped by the external input (PEST1 is set to "1"). Set PEEXCL to "1" to clear the counter when stopped by the external input.

PEEXCL	Description
0	Does not clear the counter when it is stopped by the external trigger. (initial value)
1	Clears the counter when it is stopped by the external trigger.

- **PETRM1, PETRM0** (bits 5, 4)

The PETRM1 and PETRM0 bits are used to select the count start/stop mode of PWME.
This is valid only when the external input start and stop are selected.

PETRM1	PETRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

Note:
When the timer interrupt (TM9INT/TMBINT/TMFINT) is selected for the external input with the PWECON3 register, be sure to select the rising edge start and the rising edge stop (set PETRM1 to "0" and PETRM0 "0"). Do not use other settings (The operation cannot be guaranteed because they may cause the count start/stop at timings other than interrupts).

- **PEOST** (bit 7)

The PEOST bit is used for the operation mode of the PWME.

PEOST	Description
0	One-shot mode disabled (initial value)
1	One-shot mode enabled

10.2.22 PWME Control Register 3 (PWECON3)

Address: 0F939H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWECON3	—	—	PESDE1	PESDE0	PESTSS	PESTS2	PESTS1	PESTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWECON3 is a special function register (SFR) to control PWME.
Rewrite PWECON3 while the PWME is stopped (PESTAT of the PWECON1 register is "0").

[Description of Bits]

- **PESTSS, PESTS2, PESTS1, PESTS0** (bits 3 to 0)

The PESTSS, PESTS2, PESTS1, and PESTS0 bits are used to select the external input start/stop pins of PWME.

PESTS2	PESTS1	PESTS0	Description	
			When PESTSS="0" (initial value)	When PESTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0 (Comparator 0)	PB3 pin
1	0	0	CMP1 (Comparator 1)	PB4 pin
1	0	1	TM9INT (Timer 9 interrupt)	PB5 pin
1	1	0	TMBINT (Timer B interrupt)	PB6 pin
1	1	1	TMFINT (Timer F interrupt)	PB7 pin

Note:
When a timer interrupt request is set as the external trigger signal, there are some restrictions on the edge selection of the PWM start/stop triggers. For details, see the description of the PWECON2 register.
The timer interrupt requests (TM9INT/TMBINT/TMFINT) are interrupt request signals from the timer 9/timer B/timer F, independent of the interrupt enable/disable settings by the interrupt enable registers 3/5 (IE3/5).

- **PESDE1, PESDE0** (bits 5 to 4)

The PESDE1, PESDE0 bits are used to select the emergency stop input pins of PWME.

PESDE1	PESDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge of the CMP0 (Comparator 0)
1	0	Rising edge of the CMP1 (Comparator 1)
1	1	Rising edge of PB0

Note:
The external trigger input pin and the emergency stop input pins aren't to select the same pin. When it is selected, PWM doesn't operate.

10.2.23 PWMF Period Registers (PWFPL, PWFPH)

Address: 0F960H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWFPL	PFP7	PFP6	PFP5	PFP4	PFP3	PFP2	PFP1	PFP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F961H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWFPH	PFP15	PFP14	PFP13	PFP12	PFP11	PFP10	PFP9	PFP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

PWFPH and PWFPL are special function registers (SFRs) to set the PWMF0 to 2 periods.
The settable value is "0001H" to "FFFFH".

Note:
For PWFPH and PWFPL updates during PWM operation, see Section 10.3 "Description of Operation".
Don't set the value to "0000H".

10.2.24 PWMF0 Duty Registers (PWF0DL, PWF0DH)

Address: 0F962H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF0DL	PF0D7	PF0D6	PF0D5	PF0D4	PF0D3	PF0D2	PF0D1	PF0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F963H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF0DH	PF0D15	PF0D14	PF0D13	PF0D12	PF0D11	PF0D10	PF0D9	PF0D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWF0DH and PWF0DL are special function registers (SFRs) to set the duties of PWMF0.

Note:
Set PWF0DH and PWF0DL to values smaller than those to which PWFPH and PWFPL are set.
For PWF0DH and PWF0DL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.25 PWMF1 Duty Registers (PWF1DL, PWF1DH)

Address: 0F964H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF1DL	PF1D7	PF1D6	PF1D5	PF1D4	PF1D3	PF1D2	PF1D1	PF1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F965H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF1DH	PF1D15	PF1D14	PF1D13	PF1D12	PF1D11	PF1D10	PF1D9	PF1D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWF1DH and PW1FDL are special function registers (SFRs) to set the duties of PWMF1.

Note:
Set PWF1DH and PWF1DL to values smaller than those to which PWFPH and PWFPL are set.
For PWF1DH and PWF1DL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.26 PWMF2 Duty Registers (PWF2DL, PWF2DH)

Address: 0F966H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF2DL	PF2D7	PF2D6	PF2D5	PF2D4	PF2D3	PF2D2	PF2D1	PF2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F967H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWF2DH	PF2D15	PF2D14	PF2D13	PF2D12	PF2D11	PF2D10	PF2D9	PF2D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWF2DH and PWF2DL are special function registers (SFRs) to set the duties of PWMF2.

Note:
Set PWF2DH and PWF2DL to values smaller than those to which PWFPH and PWFPL are set.
For PWF2DH and PWF2DL updates during PWM operation, see Section 10.3 "Description of Operation".

10.2.27 PWMF Counter Registers (PWFCH, PWFCL)

Address: 0F970H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCL	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F971H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCH	PFC15	PFC14	PFC13	PFC12	PFC11	PFC10	PFC9	PFC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCL and PWFCH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PWFCL or PWFCH, PWFCL and PWFCH is set to "0000H". The data that is written is meaningless. Operate this access while the PWM is stopped.
When data is read from PWFCL, the value of PWFCH is latched. When reading PWFCH and PWFCL, use a word type instruction or pre-read PWFCL.

The contents of PWFCH and PWFCL during PWMF0 to 2 operation cannot be read depending on the combination of the PWM clock and system clock. Table 10-4 shows PWFCH and PWFCL read enable/disable for each combination of the PWM clock and system clock.

Table 10-4 PWFCH and PWFCL Read Enable/Disable during PWMF Operation

PWM clock PFCK	System clock SYSCLK	PWFCH and PWFCL read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PWFCH or PWFCL twice until the last data matched the previous data.
HTBCLK	LSCLK	Read disabled
	HSCLK	Read enabled
PLLCLK (16.384MHz)	LSCLK	Read disabled
	HSCLK	

10.2.28 PWMF Control Register 0 (PWFCON0)

Address: 0F972H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCON0	—	—	PFSDN	PFNEG	PFIS1	PFIS0	PFCS1	PFCS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCON0 is a special function register (SFR) to control PWM.
Rewrite bit 0 to 4 of PWFCON0 while the PWMF is stopped (PFRUN, PFTGEN and PFSTAT of the PWFCON1 register is "0").

[Description of Bits]

- **PFCS1, PFCS0** (bits 1, 0)
  The PFCS1 and PFCS0 bits are used to select the PWMF0 to 2 operation clocks. LSCLK, HTBCLK, or PLLCLK can be selected.

PFCS1	PFCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	PLLCLK (16.384MHz)
1	1	Prohibited

- **PFIS1, PFIS0** (bits 3, 2)
  The PFIS1 and PFIS0 bits are used to select the point at which the PWMF interrupt occurs. "When the periods match", "when the duties match", or "when the periods and duties match" can be selected.

PFIS1	PFIS0	Description
0	0	When the periods matched. (initial value)
0	1	When the duties matched. *1
1	*	When the periods and duties matched.

*1: Select on which duty of PWMF0 to 2 an interrupt occurs using PWFCON5 PFDISL1 and PFDISL0.

- **PFNEG** (bit 4)
  The PFNEG bit is used to select the output logic. When PFNEG="0", the initial value of PWMF0 to 2 output is "0", and when PFNEG="1", it is "1".

PFNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **PFSDN** (bit 5)
  The PFSDN bit is used to select the forced stop of PWMF0 to 2. If "1" is written to the register, the output of PWMF0 to 2 is fixed to the value set by PFNEG register and PFnPOL (n=0 to 2) of PWFCON4.

PFSDN	Description
0	PWMF normal operation (initial value)
1	PWMF forced stop

10.2.29 PWMF Control Register 1 (PWFCON1)

Address: 0F973H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCON1	PFSTAT	PFFLG	PFSDST	—	—	—	PFTGEN	PFRUN
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCON1 is a special function register (SFR) to control PWMF.

[Description of Bits]

- **PFRUN** (bit 0)
  The PFRUN bit is used to control count stop/start of PWMF0 to 2.

PFRUN	Description
0	Stops counting. (initial value)
1	Starts counting.

- **PFTGEN** (bit 1)
  The PFTGEN is a enable flag of the count stop/start and emergency stop by the external input of PWMF0 to 2.
  An interrupt occurs when the count stops by the external input.

PFTGEN	Description
0	Disables the count stop/start and the emergency stop by the external input. (initial value)
1	Enables the count stop/start and the emergency stop by the external input.

- **PFSDST** (bit 5)
  The PFSDST bit indicates that an emergency stop interrupt of PWMF0 to 2 has occurred.
  Write "1" to this bit to clear it.

PFSDST	Description
0	An emergency stop interrupt has not occurred. (initial value)
1	An emergency stop interrupt has occurred.

- **PFFLG** (bit 6)
  The PFFLG bit is used to read the output flag of PWMF0.

PFFLG	Description
0	PWMF0 output flag = "0" (initial value)
1	PWMF0 output flag = "1"

- **PFSTAT** (bit 7)
  The PFSTAT bit indicates "counting stopped or "counting in progress" of PWMF0 to 2.

PFSTAT	Description
0	Counting stopped. (initial value)
1	Counting in progress.

Note:
When the PWM count is stopped by the external trigger and PFRUN bit shows "0", make sure to start the next operation after PFSTAT bit shows "0" as the PWM count is stopped.
For confirmation of the interrupt, see 10.3.4 "Interrupt of PWM".

10.2.30 PWMF Control Register 2 (PWFCON2)

Address: 0F974H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCON2	PFOST	—	PFTRM1	PFTRM0	—	PFEXCL	PFST1	PFST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCON2 is a special function register (SFR) to control PWMF0 to 2.
Rewrite PWFCON2 while the PWMF is stopped (PFRUN, PFTGEN and PFSTAT of the PWFCON1 register is "0").

[Description of Bits]

• **PFST1, PFST0** (bits 1, 0)
The PFST1 and PFST0 bits are used to select the start/stop mode of the PWMF0 to 2 counter.

PFST1	PFST0	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

• **PFEXCL** (bit 2)
The PFEXCL bit is used to select whether or not to clear the PWMF0 to 2 counter when stopped by the external input (PFST1 is set to "1"). Set PFEXCL to "1" to clear the counter when stopped by the external input.

PFEXCL	Description
0	Does not clear the counter when it is stopped by the external trigger. (initial value)
1	Clears the counter when it is stopped by the external trigger.

• **PFTRM1, PFTRM0** (bits 5, 4)
The PFTRM1 and PFTRM0 bits are used to select the count start/stop mode of PWMF0 to 2.
This is valid only when the external input start and stop are selected.

PFTRM1	PFTRM0	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

Note:
When the timer interrupt (TM9INT/TMBINT/TMFINT) is selected for the external input with the PWFCON3 register, be sure to select the rising edge start and the rising edge stop (set PFTRM1 to "0" and PFTRM0 "0"). Do not use other settings (The operation cannot be guaranteed because they may cause the count start/stop at timings other than interrupts).

• **PFOST** (bit 7)
The PFOST bit is used for the operation mode of the PWMF0 to 2.

PFOST	Description
0	One-shot mode disabled (initial value)
1	One-shot mode enabled

10.2.31 PWMF Control Register 3 (PWFCON3)

Address: 0F975H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCON3	—	—	PFSDE1	PFSDE0	PFSTSS	PFSTS2	PFSTS1	PFSTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCON3 is a special function register (SFR) to control PWMF0 to 2.
Rewrite PWFCON3 when PFRUN, PFTGEN, and PFSTAT of PWFCON1 register are "0".

[Description of Bits]

- **PFSTSS, PFSTS2, PFSTS1, PFSTS0** (bits 3 to 0)

The PFSTSS, PFSTS2, PFSTS1, and PFSTS0 bits are used to select the external input start/stop pins of PWMF0 to 2.

PFSTS2	PFSTS1	PFSTS0	Description	
			When PFSTSS="0" (initial value)	When PFSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	CMP0 (Comparator 0)	PB3 pin
1	0	0	CMP1 (Comparator 1)	PB4 pin
1	0	1	TM9INT (Timer 9 interrupt)	PB5 pin
1	1	0	TMBINT (Timer B interrupt)	PB6 pin
1	1	1	TMFINT (Timer F interrupt)	PB7 pin

Note:
When a timer interrupt request is set as the external trigger signal, there are some restrictions on the edge selection of the PWM start/stop triggers. For details, see the description of the PWFCON2 register.
The timer interrupt requests (TM9INT/TMBINT/TMFINT) are interrupt request signals from the timer 9/timer B/timer F, independent of the interrupt enable/disable settings by the interrupt enable registers 3/5 (IE3/5).

- **PFSDE1, PFSDE0** (bits 5 to 4)

The PFSDE1, PFSDE0 bits are used to select the emergency stop input pins of PWMF0 to 2.

PFSDE1	PFSDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge of the CMP0 (Comparator 0)
1	0	Rising edge of the CMP1 (Comparator 1)
1	1	Rising edge of PB0

Note:
The external trigger input pin and the emergency stop input pins aren't to select the same pin. When it is selected, PWM doesn't operate.

10.2.32 PWMF Control Register 4 (PWFCON4)

Address: 0F976H
Access: R/W
Access size: 8/16 bits
Initial value: 10H

	7	6	5	4	3	2	1	0
PWFCON4	—	PF2EN	PF1EN	PF0EN	—	PF2POL	PF1POL	PF0POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

PWFCON4 is a special function register (SFR) to control PWMF0 to 2.
Rewrite PWFCON4 while the PWMF0 to 2 is stopped (PFTGEN and PFSTAT of the PWFCON1 register are "0").

[Description of Bits]

- **PF2POL, PF1POL, PF0POL** (bits 2 to 0)
  The PF2POL, PF1POL, and PF0POL bits are used to select the output polarity of PWMF0 to 2.

PFnPOL	Description
0	Output the polarity set by PFNEG of PWFCON0. (Initial value)
1	Output the reverse of the polarity set by PFNEG of PWFCON0.

(n = 2 to 0)

- **PF2EN**, **PF1EN, PF0EN** (bits 6 to 4)
  The PF2EN, PF1EN, and PF0EN are output enable bits of PWMF0 to 2.

PFnEN	Description
0	Does not output PWMFn. (Initial value is Output PWMF0 only) Fixed to a value set by PFNEG of PWFCON0 and PFnPOL (n=2 to 0) of PWFCON4.
1	PWMFn outputs PWM.

(n = 2 to 0)

10.2.33 PWMF Control Register 5 (PWFCON5)

Address: 0F977H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWFCON5	—	PF2FLG	PF1FLG	PF0FLG	PFDISL1	PFDISL0	—	PFUD
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PWFCON5 is a special function register (SFR) to control PWMF0 to 2.

[Description of Bits]

- **PFUD** (bit 0)

The PFUD bit is used to update the period register and the duty register during operation. When updating the period register and the duty register during operation, write "1" to this bit after setting values for the period register and the duty register. By writing "1" to this bit, values set for the period register and the duty register are transferred to the period buffer and the duty buffer simultaneously. When the transfer completes, this bit is cleared automatically.

PFUD	Description
0	The period register and the duty register are not updated during operation. (initial value)
1	The period register and the duty register are updated during operation.

Note:
If you write "1" to this bit (to update register value), do so after reading this bit and confirm that the value is "0" (update is completed).

- **PFDISL1, PFDISL0** (bit 3 to 2)

The PFDISL1 and PFDISL0 registers are used to select PWM output which generates an interrupt cause when the duty match interrupt is selected by PFIS1 and PFIS0 of PWFCON0 register.

PFDISL1	PFDISL0	Description
0	0	Generate an interrupt at duty match of PWMF0 (initial value)
0	1	Generate an interrupt at duty match of PWMF1
1	0	Generate an interrupt at duty match of PWMF2
1	1	Setting prohibited

The setting of this bit is enabled only when the PFIS1, PFIS0 of PWFCON0 register = "01", "1x" (x=don't care).

- **PF2FLG, PF1FLG, PF0FLG** (bits 6 to 4)

The PF2FLG, PF1FLG, and PF0FLG bits are used to read the output flags of PWMF2 to 0.

PFnFLG	Description
0	PWMFn output flag = "0" (initial value)
1	PWMFn output flag = "1"

(n=2 to 0) The PF0FLG is the same as the PFFLG of PWFCON1.

10.3 Description of Operation

When the PnRUN bit of the PWMn control register 1 (PWnCON1) is set to "1", the PWMn counters (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWMn clock (PnCK) that is selected by the PWMn control register 0 (PWnCON0) and increment the count value on the 2nd falling edge.

When the count value of the PWnCH and PWnCL counter registers coincides the value of the PWMn duty buffer (PWnDBUF), the PWMn flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the PWnCH and PWnCL count values coincide the PWMn period buffer value (PWnPBUF), the PnFLG becomes "1" at the next PnCK falling edge, and the PWnCH and PWnCL are reset to "0000H" to continue counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the PnRUN bit is set to "0", the PWnCH and PWnCL counter registers stop counting after counting once the falling of the PWMn clock (PnCK). To confirm that PWnCH and PWnCL are stopped, check that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, the PWnCH and PWnCL counter registers restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWnCH and PWnCL counter registers to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWMn clock, the point at which an interrupt of PWMn occurs, and the logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

The period of the PWMn signal (T_{PWP}) and the first half duration (T_{PWD}) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWD} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency selected by the PWMn control register 0 (PWnCON0)

(n=C, D, E, F)

After the PnRUN bit is set to "1", counting starts in synchronization with the PWMn clock. This causes an error of up to 1 clock pulse to the time the first PWMn interrupt is issued. The PWMn interrupt period from the second time is fixed.
Figure 10-2 shows the operation timing of PWMn.

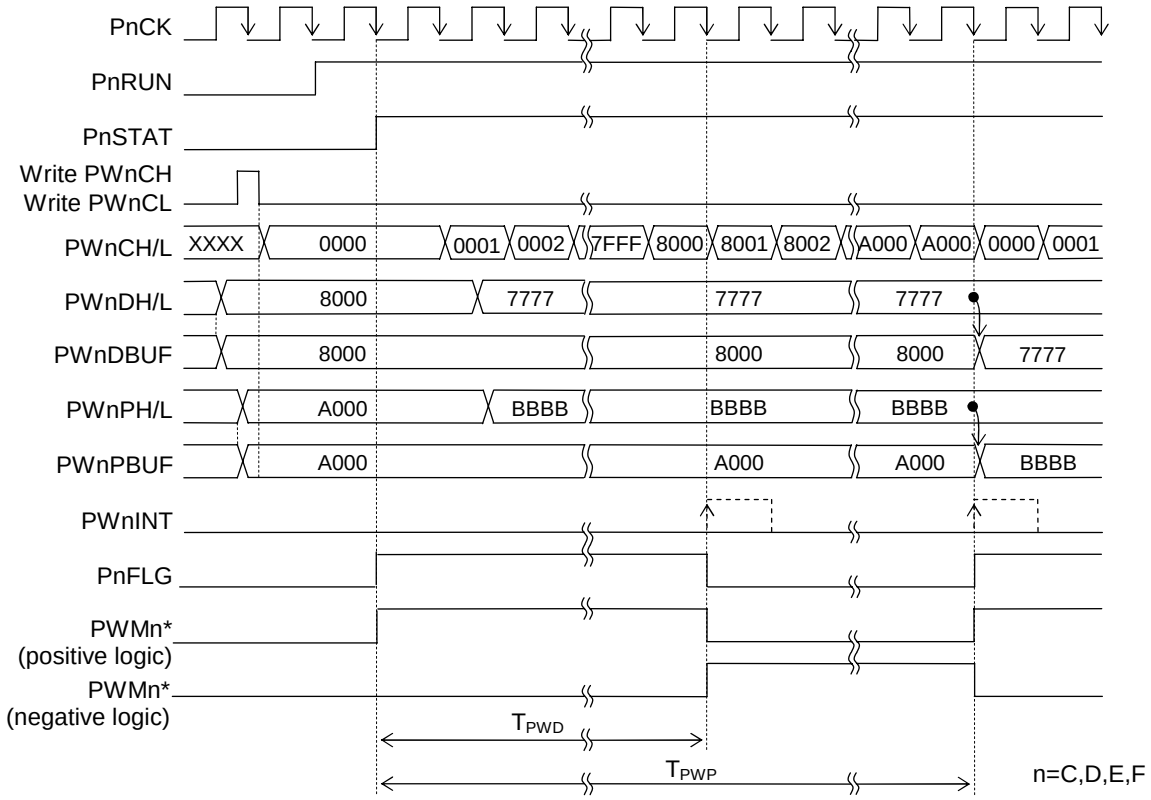


Figure 10-2 Operation Timing Diagram of PWMn

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWMn clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.
An external-triggering stop becomes invalid after setting a PnRUN bit during a PWM stop "1" until PnSTAT is set to "1." Moreover, an external-triggering start becomes invalid after making a PnRUN bit a PWM busy "0" until PnSTAT is set to "0."

10.3.1 Start, Stop, and Clear Operations of PWM by External Input Control

Setting the PnTRM1, PnTRM0, PnST1, PnST0 bits of the PWMn Control Register 2 (PWnCON2) enables the start/stop/clear control of the PWM counters (PWnCH and PWnCL) using the external input that is selected by the PnSTSS, PnSTS2 to PnSTS0 bits of the PWMn Control Register 3 (PWnCON3). Set the input pulse width to equal to or more three sampling clocks as the external input is sampled at PWM clock (PnCK). Pulses shorter than one sampling clock are removed as noises, and pulses of 1 to 3 clocks may not be removed or be removed. Note that if TM9INT, TMBINT, or TMFINT is selected as the external input, sampling is not performed. When the PnTGEN register of the PWnCON1 bit is "0", the sampling circuit does not operate.
Figure 10-3 shows the timing of sampling of the external input.

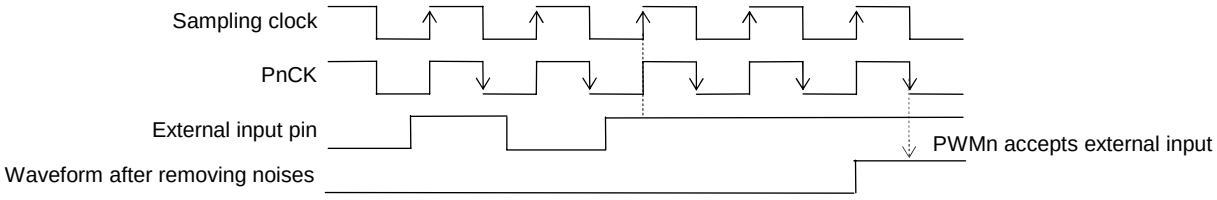


Figure 10-3 Timing Diagram of sampling of the external input

10.3.2 Emergency Stop Operation

Setting the PnSDE1 and PnSDE0 bits of the PWMn control register 3 (PWnCON3) enables the emergency stop function with the selected external input.
When the selected external input gets a rising edge input, the emergency stop flag (PnSDST) is set to "1", an emergency stop interrupt (PWnINT) is generated, and the PWM counter is stopped/cleared. Because the PWM flag output (PnFLG) is cleared, the PWMn outputs become initial status.
To release the emergency stop flag, write "1" to PnSDST of the PWMn control register 1 (PWnCON1). When the PnTGEN register of PWnCON1 is "0", the emergency stop does not operate.
Figure 10-4 shows the operation timing by emergency stop.

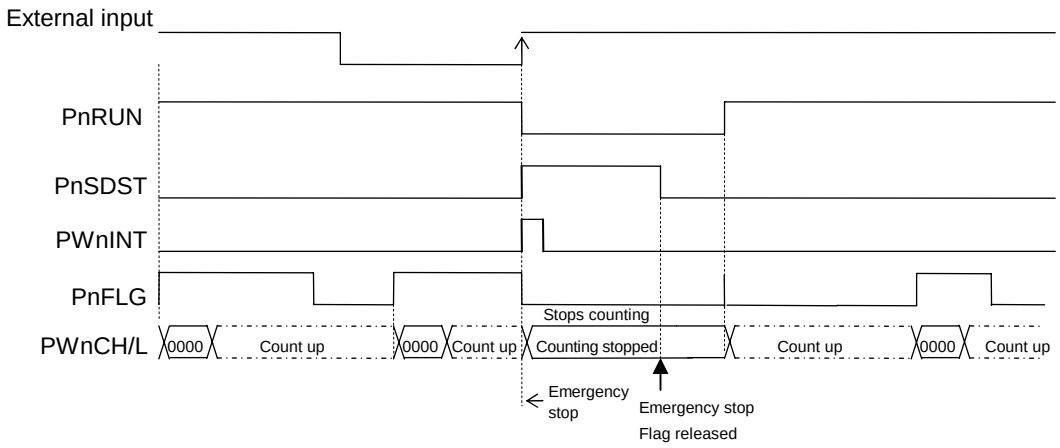


Figure 10-4 Operation Timing Diagram by Emergency Stop

10.3.3 PWMF Operation

PWMF can perform three types of output with the same period and different duties.
Polarity of each output can be set individually by the combination of PFNEG and PFnPOL.

PFNEG	PFnPOL	PWFn initial value
0	0	0
0	1	1
1	0	1
1	1	0

The following shows a PWM waveform when PFNEG="1", PF2POL="0", PF1POL="1", and PF0POL="0".

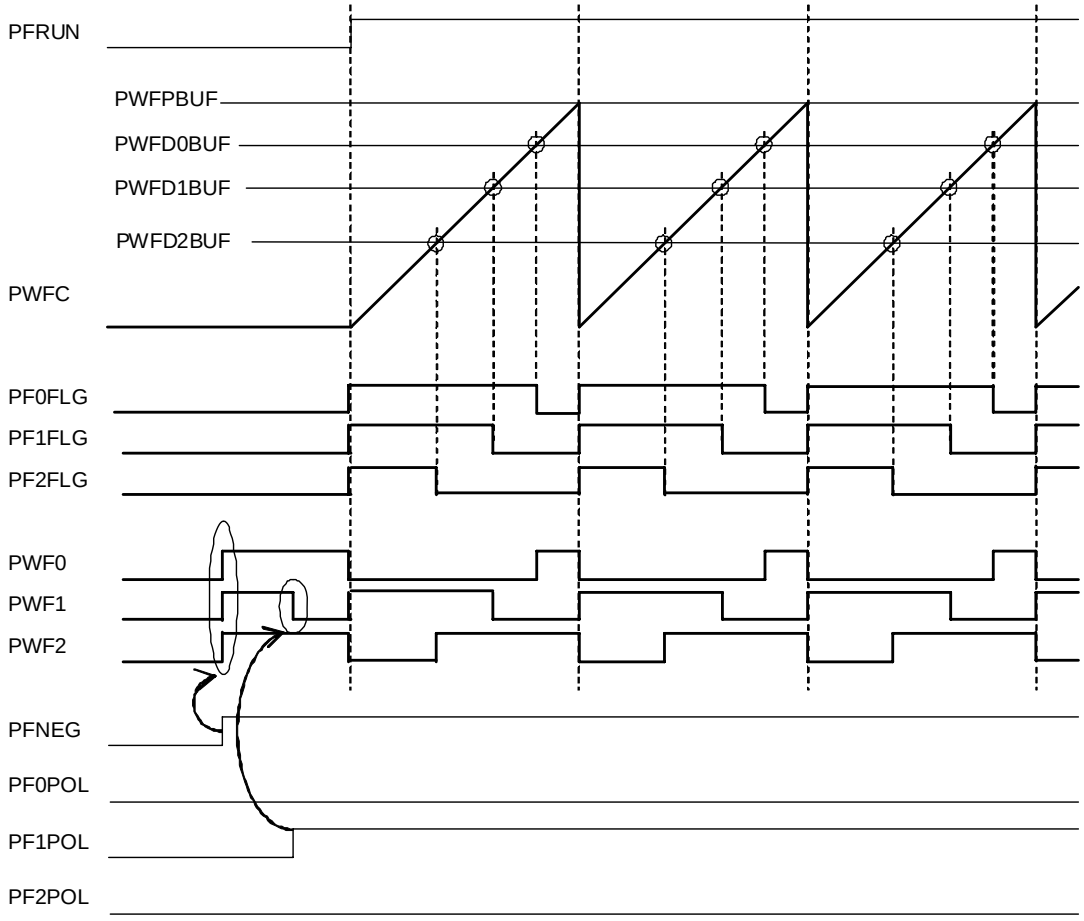
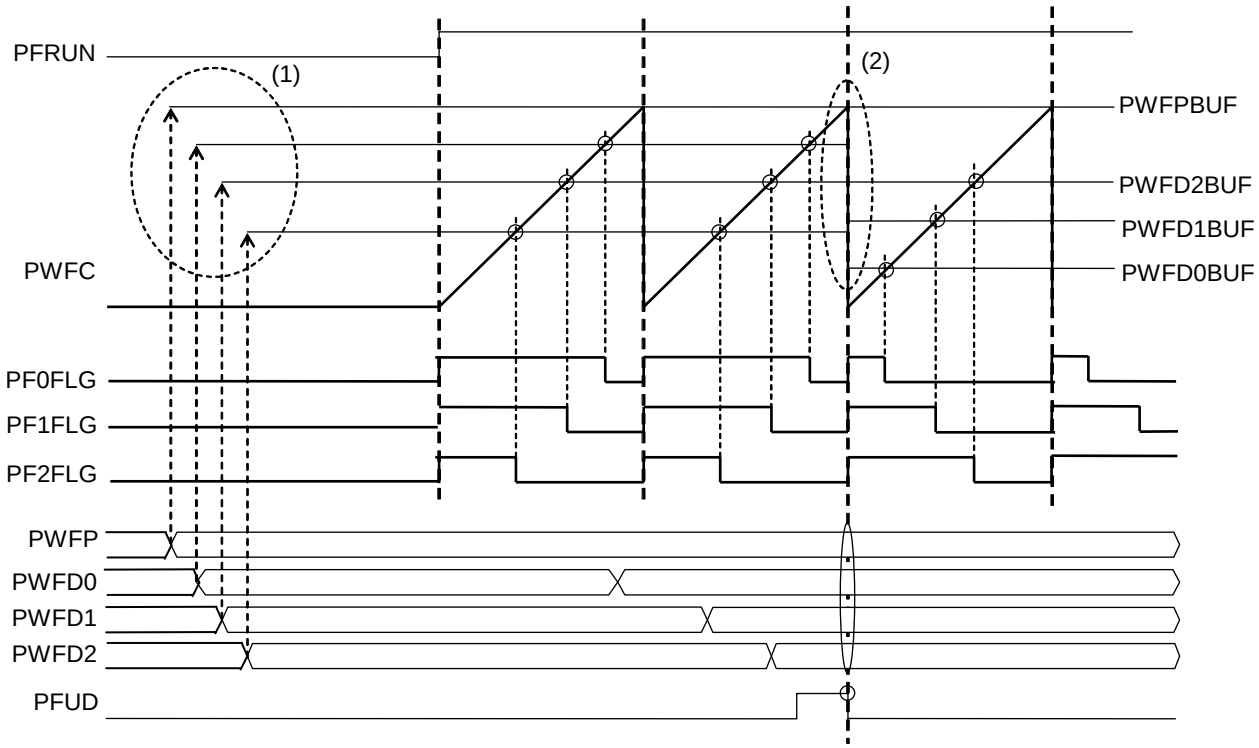


Figure 10-5 PWMF Operation Example

As PWMF has three duty registers, there is a setting update register to synchronize these changes. If you change the duty during PWMF operation, confirm that PFUD bit of PWFCON5 is "0" and then write "1" to it after setting as desired.



(1) Each buffer is updated at set timing during operation stopped.
(2) Each buffer is updated at the beginning of the next period where PFUD is set to "1" during operation.

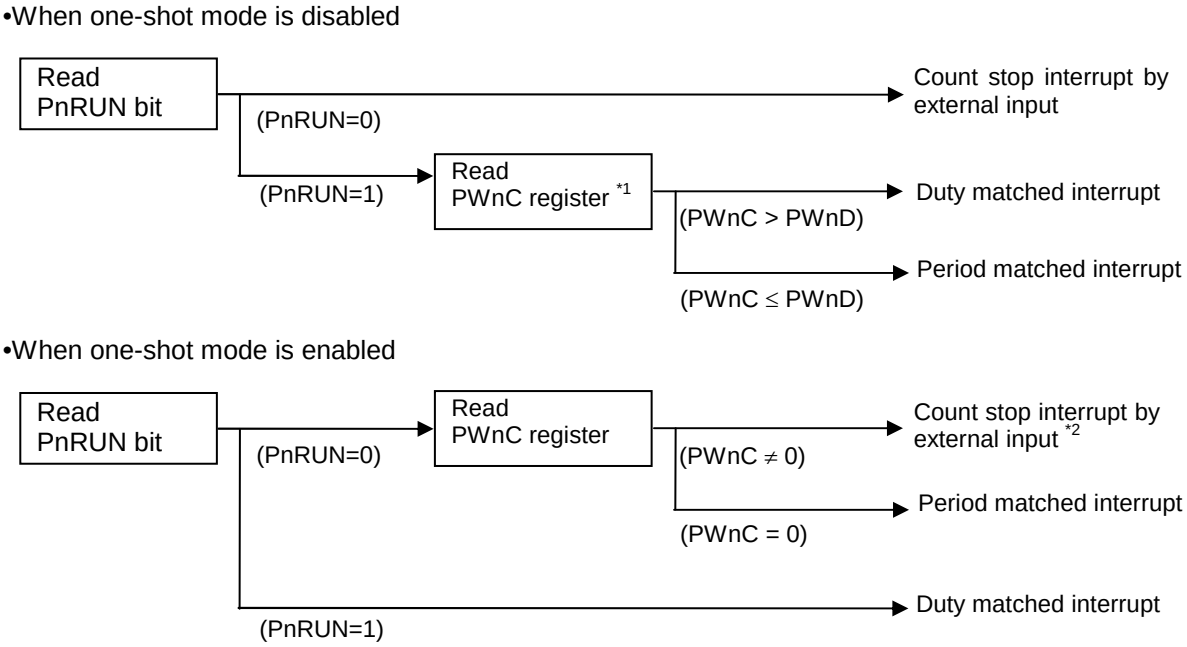
Figure 10-6 Update Timing Diagram During PWMF Operation

10.3.4 Interrupt of PWM

Interrupts of PWM contain the following four types:

- Period match interrupt
- Duty match interrupt
- Count stop interrupt by external input
- Emergency stop interrupt

Figure 10-7 shows how to identify these interrupts when one-shot mode is disabled and enabled. For emergency stop interrupt, confirm that PnSDST bit of the PWnCON1 register is set to "1" regardless of the mode.



*1 : In some settings such as when the set period is short, and when the PWM clock is selected where PWnC cannot be read, interrupts cannot be identified.
*2 : They can be identified only when PnEXCL bit of the PWnCON2 register is set to 0.

Figure 10-7 Identifying PWM Interrupt

10.4 Specifying port registers

To enable the PWM function, the applicable bit of each related port register needs to be set. See Chapter 15, "Port A", Chapter 16, "Port B" and Chapter 17, "Port C" for detail about the port registers.

10.4.1 Functioning PA0 (PWMC) as the PWM output

Set PA0MD1 bit (bit0 of PAMOD1 register) to "0", and set PA0MD0 bit (bit0 of PAMOD0 register) to "1" and set PA0DIR bit(bit0 of PADIR register) to "0", for specifying the PWM output as the secondary function of PA0.

Reg. name	PAMOD1 register (Address: 0F255H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2MD1	PA1MD1	**PA0MD1**
Data	—	—	—	—	—	*	*	**0**

Reg. name	PAMOD0 register (Address: 0F254H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2MD0	PA1MD0	**PA0MD0**
Data	—	—	—	—	—	*	*	**1**

Set PA0C1 bit (bit0 of PACON1 register) to "1" and set PA0C0 bit(bit0 of PACON0 register) to "1", for specifying the PA0 as CMOS output.

Reg. name	PACON1 register (Address: 0F253H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2C1	PA1C1	**PA0C1**
Data	—	—	—	—	—	*	*	**1**

Reg. name	PACON0 register (Address: 0F252H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2C0	PA1C0	**PA0C0**
Data	—	—	—	—	—	*	*	**1**

Reg. name	PADIR register (Address: 0F251H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2DIR	PA1DIR	**PA0DIR**
Data	—	—	—	—	—	*	*	**0**

Data of PA0D bit (bit0 of PAD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PAD register (Address: 0F250H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	—	—	—	—	—	PA2D	PA1D	**PA0D**
Data	—	—	—	—	—	*	*	**

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

10.4.2 Functioning PB0 (PWMC) as the PWM output

Set PB0MD1 bit (bit0 of PBMOD1 register) to "0", and set PB0MD0 bit (bit0 of PBMOD0 register) to "1" for specifying the PWM output as the secondary function of PB0

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	**PB0MD1**
Data	*	*	*	*	*	*	*	**0**

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	**PB0MD0**
Data	*	*	*	*	*	*	*	**1**

Set PB0C1 bit (bit0 of PBCON1 register) to "1", set PB0C0 bit(bit0 of PBCON0 register) to "1" and set PB0DIR bit(bit0 of PBDIR register) to "0", for specifying the PB0 as CMOS output.

Reg. name	PBCON1 register (Address: 0F23BH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C1	PB6C1	P35C1	PB4C1	PB3C1	PB2C1	PB1C1	**PB0C1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBCON0 register (Address: 0F23AH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	**PB0C0**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBDIR register (Address: 0F239H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PBBDIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	**PB0DIR**
Data	*	*	*	*	*	*	*	**0**

Data of PB0D bit (bit0 of PBD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F238H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	**PB0D**
Data	*	*	*	*	*	*	*	******

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

10.4.3 Functioning PB7 (PWMC) as the PWM output

Set PB7MD1 bit (bit7 of PBMOD1 register) to "1", and set PB7MD0 bit (bit7 of PBMOD0 register) to "1" for specifying the PWM output as the fourthly function of PB7

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	**1**	*	*	*	*	*	*	*

Set PB7C1 bit (bit7 of PBCON1 register) to "1", set PB7C0 bit(bit7 of PBCON0 register) to "1" and set PB7DIR bit(bit7 of PBDIR register) to "0", for specifying the PB7 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C1**	PB6C1	P35C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PBBDIR**	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	**0**	*	*	*	*	*	*	*

Data of PB7D bit (bit7 of PBD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
Data	******	*	*	*	*	*	*	*

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

Chapter 11

Synchronous Serial Port

11 Synchronous Serial Port

11.1 Overview

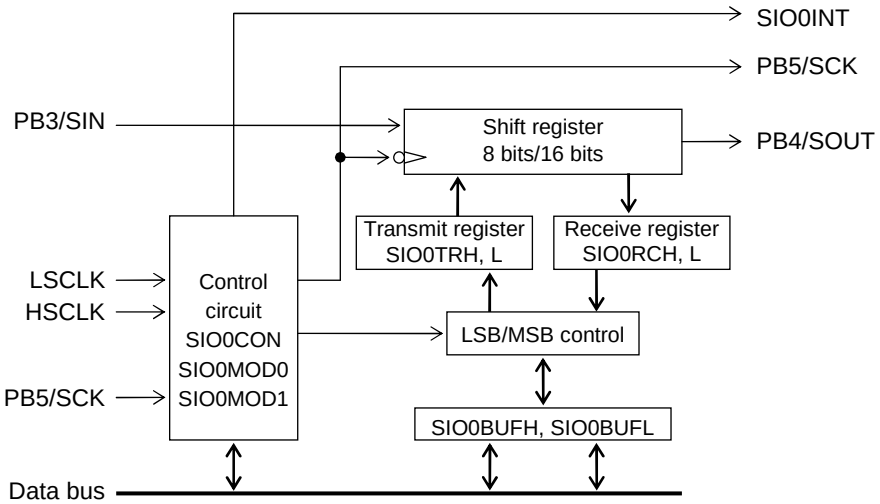
This LSI includes one channel of the 8/16-bit synchronous serial port (SSIO) and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
When the synchronous serial port is used, the secondary functions of port B must be set. For the secondary functions of port B, see Chapter 16, "Port B".

11.1.1 Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable for the data length

11.1.2 Configuration

Figure 11-1 shows the configuration of the synchronous serial port.



SIO0BUFL: Serial port transmit/receive buffer L
SIO0BUFH: Serial port transmit/receive buffer H
SIO0CON: Serial port control register
SIO0MOD0: Serial port mode register 0
SIO0MOD1: Serial port mode register 1

Figure 11-1 Configuration of Synchronous Serial Port

11.1.3 List of Pins

Pin name	I/O	Description
PB3/SIN	I	Receive data input. Used for the secondary function of the PB3 pin.
PB5/SCK	I/O	Synchronous clock input/output. Used for the secondary function of the PB5 pin.
PB4/SOUT	O	Transmit data output. Used for the secondary function of the PB4 pin.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	—	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H

11.2.2 Serial Port Transmit/Receive Buffers (SIO0BUFL, SIO0BUFH)

Address: 0F280H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F281H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUFL and SIO0BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port.
When data is written in SIO0BUFL and SIO0BUFH, the data is written in the transmit registers (SIO0TRL and SIO0TRH) and when data is read from SIO0BUFL and SIO0BUFH, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

11.2.3 Serial Port Control Register (SIO0CON)

Address: 0F282H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0CON	—	—	—	—	—	—	—	S0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port.

[Description of Bits]

- **S0EN** (bit 0)

  The S0EN bit is used to specify start of synchronous serial communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated.
  The S0EN bit is set to "0" at a system reset.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

11.2.4 Serial Port Mode Register 0 (SIO0MOD0)

Address: 0F284H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	—	—	—	—	S0LG	S0MD1	S0MD0	S0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD0 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

• **S0DIR** (bit 0)
The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

• **S0MD1, S0MD0** (bits 2, 1)
The S0MD1 and S0MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

• **S0LG** (bit 3)
The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
The S0LG bit is set to "0" at a system reset.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

Note:
– Do not change any of the SIO0MOD0 register settings during transmission/reception.
– When the synchronous serial port is used, the secondary functions of port B must be set. For the secondary functions of Port B, see Chapter 16, "Port B".

11.2.5 Serial Port Mode Register 1 (SIO0MOD1)

Address: 0F285H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD1	—	—	—	S0CKT	S0CK3	S0CK2	S0CK1	S0CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD1 is a special function register (SFR) to set mode of the synchronous serial port.

[Description of Bits]

• **S0CK3 to S0CK0** (bits 3 to 0)

The S0CK3 to S0CK0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK3	S0CK2	S0CK1	S0CK0	Description
0	0	0	0	1/1 LSCLK (initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	External clock 0 (PB5/SCK)
0	1	1	1	Prohibited
1	0	*	*	Prohibited
1	1	0	0	1/1 HSCLK
1	1	0	1	1/2 HSCLK
1	1	1	*	Prohibited

Note:
– In slave mode, the maximum input frequency of the SCK is 2MHz.
– In master mode, the maximum output frequency of the SCK is 4.2MHz.
If you select the 1/1 HSCLK(S0CK3-0 is set to "1100b"), you must set the HSCLK less than 4.2MHz.
For exsample:
– If you use the PLL(in case of OSCM0 bit is "0"), you must set except for 1/1 HSCLK(SYSC1-0 is set the "00b").
– If you use the CLKIN(in case of OSCM0 bit is "1"), you must set 1/1 HSCLK(SYSC1-0 is set the "00b") and CLKIN is inputted clock cycle of 4MHz.

• **S0CKT** (bit 4)

The S0CKT bit is used to select a tansfer clock output phase.

S0CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

Note:
– Do not change the value of the SIO0MOD1 register during transmission or reception.

11.3 Description of Operation

11.3.1 Transmit Operation

When "1" is written to the S0MD1 bit and "0" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a transmit mode.
When transmit data is written to the serial port transmit /receive buffer (SIO0BUFL and H) and the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0NT) occurs and the S0EN bit is set to "0".
Transmit data is output from the secondary function pins (PB4/SOUT) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MOD1), the LSI is set to a master mode and when an external clock (PB5/SCK) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first/LSB first.
The transmit data output pin (PB4/SOUT) and transfer clock input/output pin (PB5/SCK) must be set to the secondary functions.
Figures 11-2 and 11-3 show the transmit operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, LSB first, clock types 0 and 1).

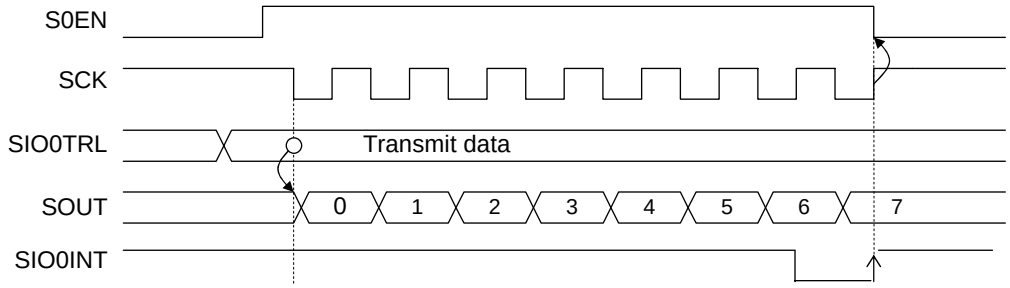


Figure 11-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first)

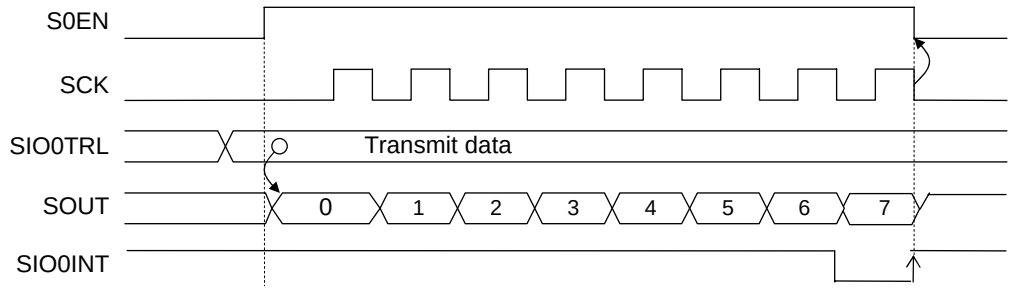


Figure 11-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first)

11.3.2 Receive Operation

When "0" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the secondary function pins (PB3/SIN) of GPIO.
When an internal clock is selected in the serial port mode register (SIO0MD1), the LSI is set to a master mode and when an external clock (PB5/SCK) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first or LSB first.
The receive data input pin (PB3/SIN) and transfer clock input/output pin (PB5/SCK) must be set to the secondary function.
Figures 11-4 and 11-5 show the receive operation waveforms of the synchronous serial ports for clock type 0 and clock type 1, respectively (8-bit length, MSB first, clock types 0 and 1).

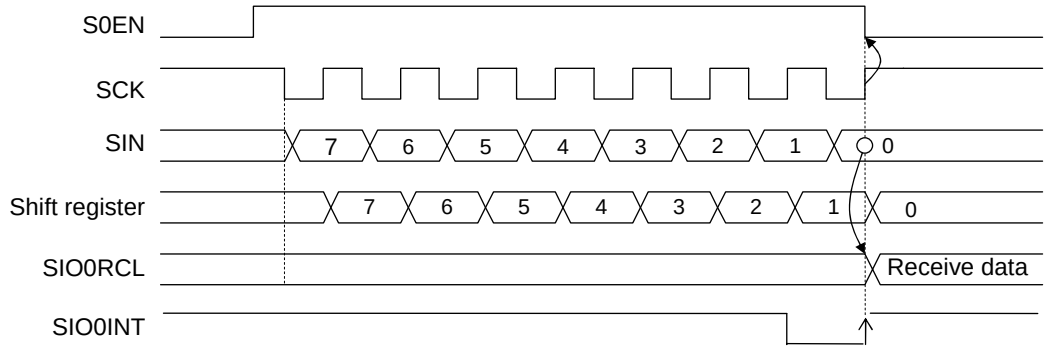


Figure 11-4 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, MSB first)

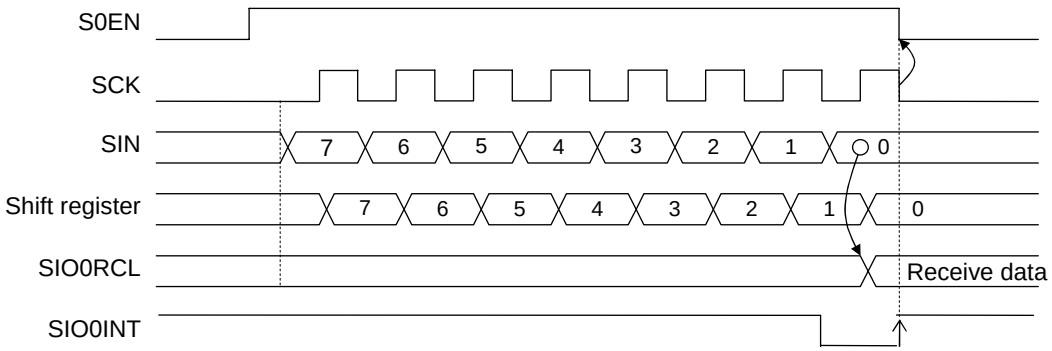


Figure 11-5 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, MSB first)

Note:
When the SOUT pin is set to the secondary function output in receive mode, a "H" level is output from the SOUT output pin.

11.3.3 Transmit/Receive Operation

When "1" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD0), this LSI is set to a transmit/receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the secondary function pins (PB3/SIN) of GPIO, and transmit data is output from the secondary function pins (PB4/SOUT) of GPIO
When an internal clock is selected in the serial port mode register (SIO0MD1), the LSI is set to a master mode and when an external clock (PB5/SCK) is selected, the LSI is set ot a slave mode.
The serial port mode register (SIO0MOD0) enables selection of MSB first or LSB first.
The receive data input pin (PB3/SIN), the transmit data output pin (PB4/SOUT), and transfer clock input/output pin (PB5/SCK) must be set to the secondary function.
Figure 11-6 shows the transmit/receive operation waveforms of the synchronous serial port (16-bit length, LSB first, clock types 0).

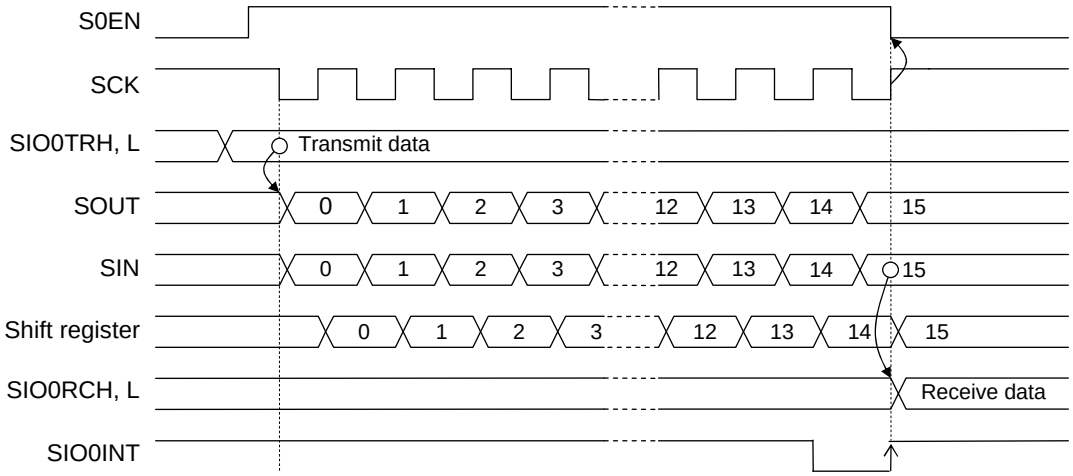


Figure 11-6 Transmit/Receive Operation Waveforms of Synchronous Serial Port (16-bit Length, LSB first, Clock Type 0)

11.4 Specifying port registers

For enable the SSIO function, each related port register needs to be set up. Refer to the Chapter 16, "Port B" for details of each register.

11.4.1 Functioning as the SSIO master mode

SSIO is selected as the secondary function of PB5, PB4, and PB3 by setting PB5MD1-PB3MD1 bit (PBMOD1 register: bit5-3) to "0" and setting PB5MD0-PB3MD0 bit (PBMOD0 register: bit5-3) to "1".

reg. name	PBMOD1 register (Address:0F25DH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7MD1	PB6MD1	**PB5MD1**	**PB4MD1**	**PB3MD1**	PB2MD1	PB1MD1	PB0MD1
value	*	*	**0**	**0**	**0**	*	*	*

reg. name	PBMOD0 register (Address:0F25CH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7MD0	PB6MD0	**PB5MD0**	**PB4MD0**	**PB3MD0**	PB2MD0	PB1MD0	PB0MD0
value	*	*	**1**	**1**	**1**	*	*	*

The state of the PB5 and PB4 pin is selected as CMOS output mode by setting PB5C1-PB4C1 bit (PBCON1 register:bit5-4) to "1" , setting PB5C0-PB4C0 bit (PBCON0 register:bit5-4) to "1" and setting PB5DIR-PB4DIR bit (PBDIR register:bit5-4) to "0". Additionally, the PB3 pin is selected as input pin by setting PB3DIR bit (PBDIR register: bit3) to "1"
The setting value of PB3C1 bit and PB3C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the PB3 pin is connected.

reg. name	PBCON1 register (Address:0F25BH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7C1	PB6C1	**PB5C1**	**PB4C1**	**PB3C1**	PB2C1	PB1C1	PB0C1
value	*	*	**1**	**1**	**$**	*	*	*

reg. name	PBCON0 register (Address:0F25AH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7C0	PB6C0	**PB5C0**	**PB4C0**	**PB3C0**	PB2C0	PB1C0	PB0C0
value	*	*	**1**	**1**	**$**	*	*	*

reg. name	PBDIR register (Address:0F259H)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7DIR	PB6DIR	**PB5DIR**	**PB4DIR**	**PB3DIR**	PB2DIR	PB1DIR	PB0DIR
value	*	*	**0**	**0**	**1**	*	*	*

As for PB5D-PB3D bit (PBD register:bit5-3), neither "0" nor "1" is problematic.

reg. name	PBD register (Address:0F258H)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7D	PB6D	**PB5D**	**PB4D**	**PB3D**	PB2D	PB1D	PB0D
value	*	*	****	****	****	*	*	*

* : no relation to the SSIO function **: Don't care $: Optional

11.4.2 Functioning as the SSIO slave mode

SSIO is selected as the secondary function of PB5, PB4, and PB3 by setting PB5MD1-PB3MD1 bit (PBMOD1 register: bit5-3) to "0" and setting PB5MD0-PB3MD0 bit (PBMOD0 register: bit5-3) to "1". It is the same setup as the case of master mode.

reg. name	PBMOD1 register (Address:0F25DH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7MD1	PB6MD1	**PB5MD1**	**PB4MD1**	**PB3MD1**	PB2MD1	P4BMD1	PB0MD1
value	*	*	**0**	**0**	**0**	*	*	*

reg. name	PBMOD0 register (Address:0F25CH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7MD0	PB6MD0	**PB5MD0**	**PB4MD0**	**PB3MD0**	PB2MD0	PB1MD0	PB0MD0
value	*	*	**1**	**1**	**1**	*	*	*

The state of the PB4 pin is selected as CMOS output mode by setting PB4C1 bit (PBCON1 register:bit4) to "1" , setting PB4C0 bit (PBCON0 register:bit4) to "1" and setting PB4DIR bit (PBDIR register:bit4) to "0". Additionally, the PB5 and PB3 pin is selected as input pin by setting PB5DIR,PB3DIR bit (PBDIR register: bit5,3) to "1"
The setting value of PB5C1,PB3C1 bit and PB5C0,PB3C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the PB5 and PB3 pin is connected.

reg. name	PBCON1 register (Address:0F25BH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7C1	PB6C1	**PB5C1**	**PB4C1**	**PB3C1**	PB2C1	PB1C1	PB0C1
value	*	*	**$**	**1**	**$**	*	*	*

reg. name	PBCON0 register (Address:0F25AH)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7C0	PB6C0	**PB5C0**	**PB4C0**	**PB3C0**	PB2C0	PB1C0	PB0C0
value	*	*	**$**	**1**	**$**	*	*	*

reg. name	PBDIR register (Address:0F259H)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7DIR	PB6DIR	**PB5DIR**	**PB4DIR**	**PB3DIR**	PB2DIR	PB1DIR	PB0DIR
value	*	*	**1**	**0**	**1**	*	*	*

As for PB5D-PB3D bit (PBD register:bit5-3), neither "0" nor "1" is problematic.

reg. name	PBD register (Address:0F258H)							
bit	7	6	**5**	**4**	**3**	2	1	0
bit name	PB7D	PB6D	**PB5D**	**PB4D**	**PB3D**	PB2D	PB1D	PB0D
value	*	*	**	**	**	*	*	*

* : no relation to the SSIO function **: Don't care $: Optional

Chapter 12

UART

12 UART

12.1 Overview

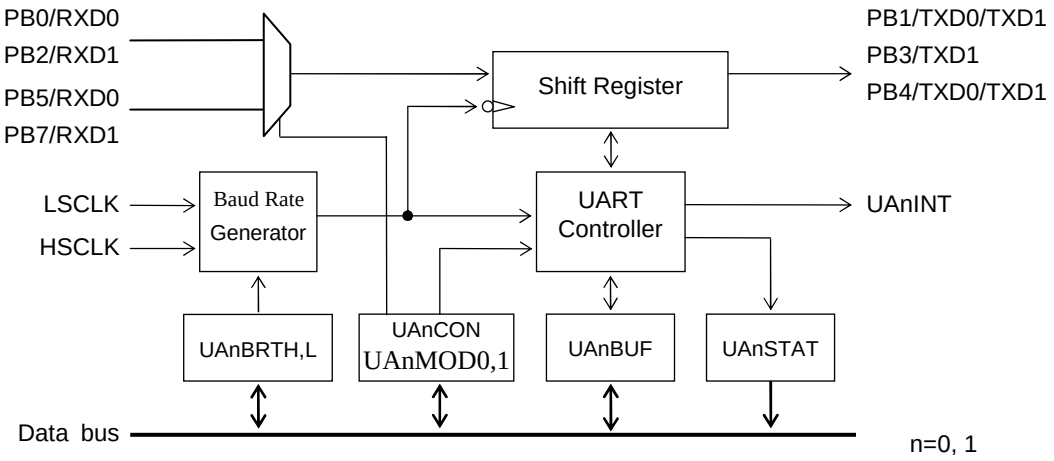
This LSI includes 2 channels of UART (Universal Asynchronous Receiver Transmitter) which is an asynchronous serial interface of a half-duplex. (A full-duplex is also possible by using 2 channels.)
The use of UART requires setting of the tertiary/fourthly functions of Port B. For the tertiary/fourthly functions of Port B, see Chapter 16, "Port B".

12.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bits selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 2400bps to 115200bps.
- Built-in baud rate generator.

12.1.2 Configuration

Figure 12-1 shows the configuration of the UART.



UAnBUF : UARTn transmit/receive buffer
UAnBRTH,L : UARTn baud rate H and L are:
UAnCON : UARTn control register
UAnMOD0,1 : UARTn mode registers 0 and 1
UAnSTAT : UARTn status register

Figure 12-1 Configuration of UART

12.1.3 List of Pins

Pin name	I/O	Function
PB0/RXD0	I	UART0 data input pin Used for the primary function of the PB0 pin.
PB5/RXD0	I	UART0 data input pin Used for the primary function of the PB5 pin.
PB1/TXD0/TXD1	O	UART0/UART1 data output pin Used for the tertiary/fourthly function of the PB1 pin.
PB4/TXD0/TXD1	O	UART0/UART1 data output pin Used for the tertiary/fourthly function of the PB4 pin.
PB2/RXD1	I	UART1 data input pin Used for the primary function of the PB2 pin.
PB7/RXD1	I	UART1 data input pin Used for the primary function of the PB7 pin.
PB3/TXD1	O	UART1 data output pin Used for the tertiary function of the PB3 pin.

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F298H	UART1 transmit/receive buffer	UA1BUF	—	R/W	8	00H
0F299H	UART1 control register	UA1CON	—	R/W	8	00H
0F29AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F29BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F29CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F29DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F29EH	UART1 status register	UA1STAT	—	R/W	8	00H

12.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmitted/received data of the UART.
In transmit mode, write transmission data to UA0BUF. To transmit the data consecutively, confirm the U0FUL flag of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to the UA0BUF. Any value written to UA0BUF can be read.
In receive mode, since data received at termination of reception is stored in UA0BUF, read the contents of UA0BUF using the UART0 interrupt at termination of reception. At continuous reception, UA0BUF is updated whenever reception terminates. Any write to UA0BUF is disabled in receive mode.
The bits, which are not required when any of the 5 to 7-bit data length is selected, become invalid in transmit mode and are set to "0" in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting the transmitted data in UA0BUF.

12.2.3 UART1 Transmit/Receive Buffer (UA1BUF)

Address: 0F298H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1BUF	U1B7	U1B6	U1B5	U1B4	U1B3	U1B2	U1B1	U1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1BUF is a special function register (SFR) to store the transmitted/received data of the UART.
In transmit mode, write transmission data to UA1BUF. To transmit the data consecutively, confirm the U1FUL flag of the UART1 status register (UA1STAT) becomes "0", then write the next transmitted data to the UA1BUF. Any value written to UA1BUF can be read.
In receive mode, since data received at termination of reception is stored in UA1BUF, read the contents of UA1BUF using the UART1 interrupt at termination of reception. At continuous reception, UA1BUF is updated whenever reception terminates. Any write to UA1BUF is disabled in receive mode.
The bits, which are not required when any of the 5 to 7-bit data length is selected, become invalid in transmit mode and are set to "0" in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA1MOD0 and UA1MOD1) before setting the transmitted data in UA1BUF.

12.2.4 UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)

  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

12.2.5 UART1 Control Register (UA1CON)

Address: 0F299H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1CON	—	—	—	—	—	—	—	U1EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA1CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U1EN** (bit 0)

  The U1EN bit is used to specify the UART communication operation start. When U1EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U1EN	Description
0	Stops communication. (Initial value)
1	Starts communication

12.2.6 UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	—	—	U0RSS	U0RSEL	—	U0CK1	U0CK0	U0IO
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U0CK1, U0CK0** (bits 2, 1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited
1	*	HSCLK

- **U0RSEL** (bit 4)
  The U0RSEL bit is used to select the received data input pin for the UART0.

U0RSEL	Description
0	Selects the PB0 pin. (Initial value)
1	Selects the PB5 pin.

- **U0RSS** (bit 5)
  The U0RSS bit is used to select the received data input sampling timing for the UART0.

U0RSS	Description
0	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 (Initial value)
1	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 – 1

Note:
Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.

12.2.7 UART1 Mode Register 0 (UA1MOD0)

Address: 0F29AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	—	—	U1RSS	U1RSEL	—	U1CK1	U1CK0	U1IO
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U1IO** (bit 0)
  The U1IO bit is used to select transmit or receive mode.

U1IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U1CK1, U1CK0** (bits 2, 1)
  The U1CK1 and U1CK0 bits are used to select the clock to be input to the baud rate generator of the UART1.

U1CK1	U1CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited
1	*	HSCLK

- **U1RSEL** (bit 4)
  The U1RSEL bit is used to select the received data input pin for the UART1.

U1RSEL	Description
0	Selects the PB2 pin. (Initial value)
1	Selects the PB7 pin.

- **U1RSS** (bit 5)
  The U1RSS bit is used to select the received data input sampling timing for the UART1.

U1RSS	Description
0	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 (Initial value)
1	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 – 1

Note:
Always set the UA1MOD0 register while communication is stopped, and do not rewrite it during communication.

12.2.8 UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	—	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0LG1, U0LG0** (bits 1, 0)

The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1, U0PT0** (bits 3, 2)

The U0PT1 and U0PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 4)

The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U0NEG** (bit 5)

The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 6)

The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

12.2.9 UART1 Mode Register 1 (UA1MOD1)

Address: 0F29BH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1MOD1	—	U1DIR	U1NEG	U1STP	U1PT1	U1PT0	U1LG1	U1LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U1LG1, U1LG0** (bits 1, 0)

The U1LG1 and U1LG0 bits are used to specify the data length in the communication of the UART.

U1LG1	U1LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U1PT1, U1PT0** (bits 3, 2)

The U1PT1 and U0PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART.

U1PT1	U1PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U1STP** (bit 4)

The U1STP bit is used to select the stop bit length in the communication of the UART.

U1STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U1NEG** (bit 5)

The U1NEG bit is used to select positive logic or negative logic in the communication of the UART.

U1NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U1DIR** (bit 6)

The U1DIR bit is used to select LSB first or MSB first in the communication of the UART.

U1DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA1MOD1 register while communication is stopped, and do not rewrite it during communication.

12.2.10 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8-bit
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 12.3.2, "Baud Rate".

Note:
Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

12.2.11 UART1 Baud Rate Registers L, H (UA1BRTL, UA1BRTH)

Address: 0F29CH
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA1BRTL	U1BR7	U1BR6	U1BR5	U1BR4	U1BR3	U1BR2	U1BR1	U1BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F29DH
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA1BRTH	—	—	—	—	U1BR11	U1BR10	U1BR9	U1BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA1BRTL and UA1BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 12.3.2, "Baud Rate".

Note:
Always set the UA1BRTL and UA1BRTH registers while communication is stopped, and do not rewrite them during communication.

12.2.12 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	—	—	—	—	U0FUL	U0PER	U0OER	U0FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

- **U0FER** (bit 0)

  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	With framing error

- **U0OER** (bit 1)

  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" if the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)

  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

- **U0FUL** (bit 3)

  The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When the transmitted data is written in UA0BUF in transmit mode, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U0FUL flag becomes "0", then write the next transmitted data to the UA0BUF.
  The U0FUL bit is fixed to "0" in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

12.2.13 UART1 Status Register (UA1STAT)

Address: 0F29EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1STAT	—	—	—	—	U1FUL	U1PER	U1OER	U1FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA1STAT, all the flags are initialized to "0".

[Description of Bits]

- **U1FER** (bit 0)

  The U1FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U1FER bit is set to "1". This bit is updated each time reception is completed.
  The U1FER bit is fixed to "0" in transmit mode.

U1FER	Description
0	No framing error (initial value)
1	With framing error

- **U1OER** (bit 1)

  The U1OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA1BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U1EN bit and then reception is restarted, this bit is set to "1" if the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U1OER bit is fixed to "0" in transmit mode.

U1OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U1PER** (bit 2)

  The U1PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U1PER is updated whenever data is received.
  The U1PER bit is fixed to "0" in transmit mode.

U1PER	Description
0	No parity error (initial value)
1	Parity error

- **U1FUL** (bit 3)

  The U1FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When the transmitted data is written in UA1BUF in transmit mode, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U1FUL flag becomes "0", then write the next transmitted data to the UA1BUF.
  The U1FUL bit is fixed to "0" in receive mode.

U1FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

12.3 Description of Operation

12.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UARTn mode register 1 (UAnMOD1).
Figure 12-2 and Figure 12-3 show the positive logic input/output format and negative logic input/output format, respectively.

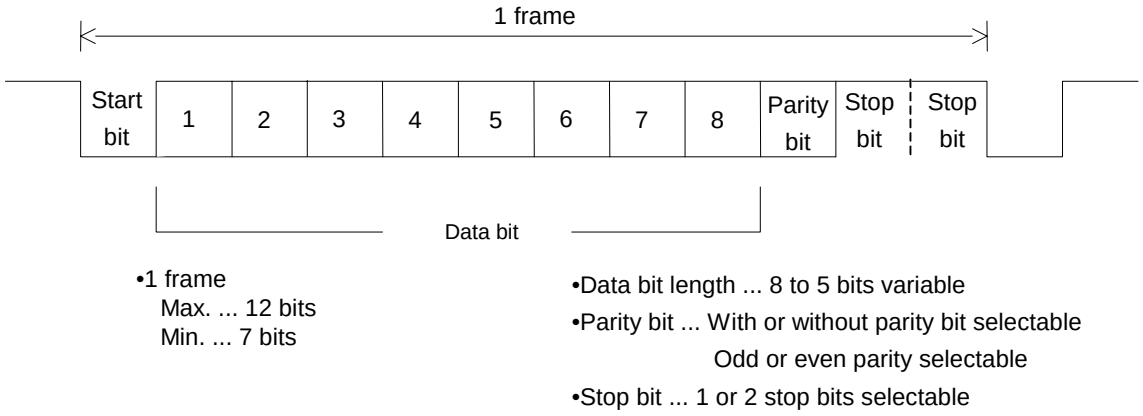


Figure 12-2 Positive Logic Input/Output Format

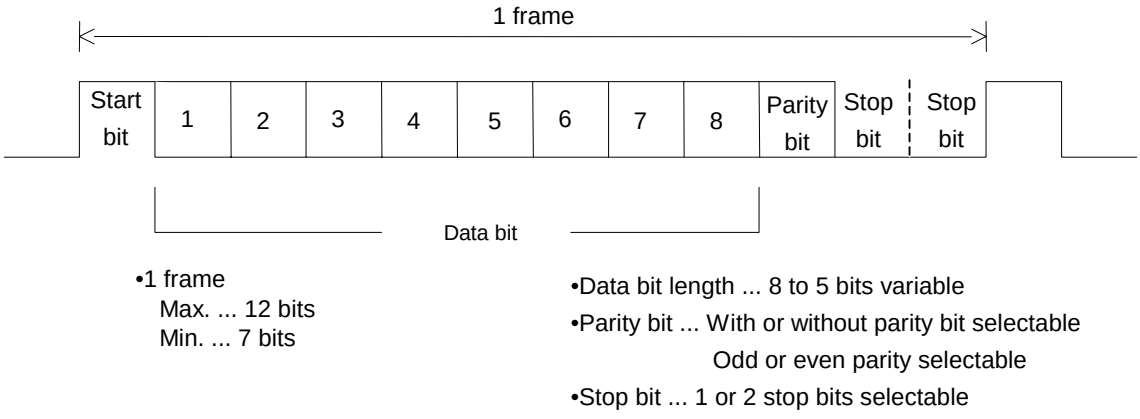


Figure 12-3 Negative Logic Input/Output Format

12.3.2 Baud rate

Baud rates are generated by the baud generator.

The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (UnCK1, UnCK0) of the UARTn mode register 0 (UAnMOD0). The count value of the baud rate generator can be set by writing it in the UARTn baud rate register H or L (UAnBRTH, UAnBRTL). The maximum count is 4096.

The setting values of UAnBRTH and UAnBRTL are expressed by the following equation.

$$\text{UAnBRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 12-1 lists the count values for typical baud rates.

Table 12-1 Count Values for Typical Baud Rates

Baud rate	Baud rate generator Clock selection	Baud rate generator counter value				Error [%]
	Baud rate Clock	Count value	Period of one bit	UAnBRTH	UAnBRTL	
2400bps	8.192MHz	3413	Approximately 417us	0DH	054H	0.01
4800bps		1707	Approximately 208us	06H	0AAH	-0.02
9600bps		853	Approximately 104us	03H	054H	0.04
19200bps		427	Approximately 52us	01H	0AAH	-0.08
38400bps		213	Approximately 26us	00H	0D4H	0.16
57600bps		142	Approximately 17.4us	00H	08DH	0.16
115200bps		71	Approximately 8.7us	00H	046H	0.16

12.3.3 Transmitted Data Direction

Figure 12-4 shows the relationship between the transmit/receive buffer and the transmitted/received data.

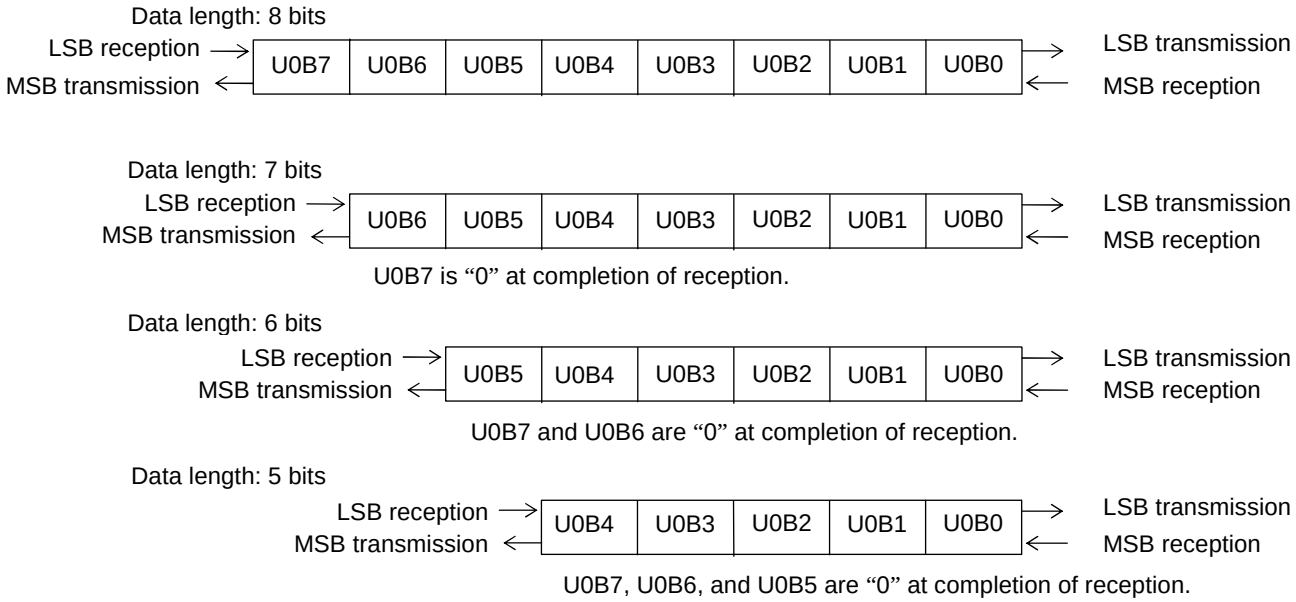


Figure 12-4 Relationship between Transmit/Receive Buffer and Transmitted/Received Data

Note:
When the TXDn pin is set to serve the secondary function output in receive mode, "H" level is output from the TXDn output.

12.3.4 Transmit Operation

Transmission is started by setting the UnIO bit of the UARTn mode register 0 (UA0MOD0) to "0" to select transmit mode and setting the UnEN bit of the UARTn control register (UAnCON) to "1".
Figure 12-5 shows the operation timing for transmission.

When the UnEN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmission.
The start bit is output to the TXDn pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UARTn interrupt is requested. In the UARTn interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UAnBUF).
When the next data to be transmitted is written to the transmit/receive buffer (UAnBUF), the transmit buffer status flag (UnFUL) is set to "1" (③) and a UARTn interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. If the UARTn interrupt routine is terminated without writing the next data to the transmit/receive buffer, the UnFUL bit is not set to "1" (⑤) and transmission continues up to the transmission of the stop bit, then the UnEN bit is reset to "0" and a UARTn interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

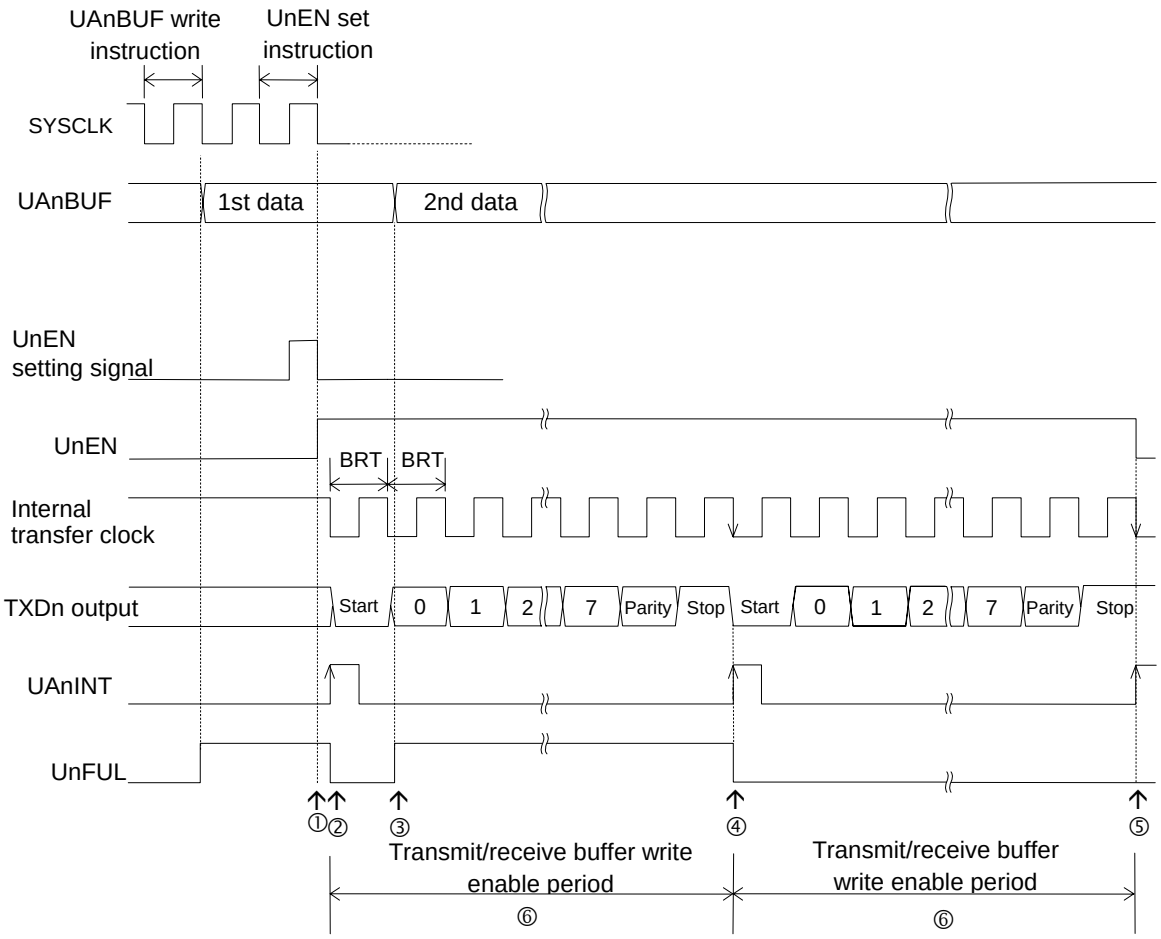


Figure 12-5 Operation Timing in Transmission

12.3.5 Receive Operation

Select the received data pin using the UnRSEL bit of the UARTn mode register 0 (UAnMOD0). Select the receive mode by setting the UnIO bit of the UARTn mode register 0 (UAnMOD0) to "1". Then, set the UnEN bit of the UARTn control register (UAnCON) to "1" to start receiving data.
Figure 12-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXDn and waits for the arrival of a start bit. When detecting a start bit (①), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXDn on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the transmit/receive buffer (UAnBUF) concurrently with the fall of the internal transfer clock of ③.
The LSI requests a UARTn interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UARTn status register (UAnSTAT) to "1".

Parity error : SnPER = "1"
Overrun error : SnOER = "1"
Framing error : SnFER = "1"

As shown in Figure 12-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the UnEN bit is reset to "0" by the program. When the UnEN bit is reset to "0" during reception, the received data may be destroyed. When the UnEN bit is reset to "0" during the "UnEN reset enable period" in Figure 12-6, the received data is protected.

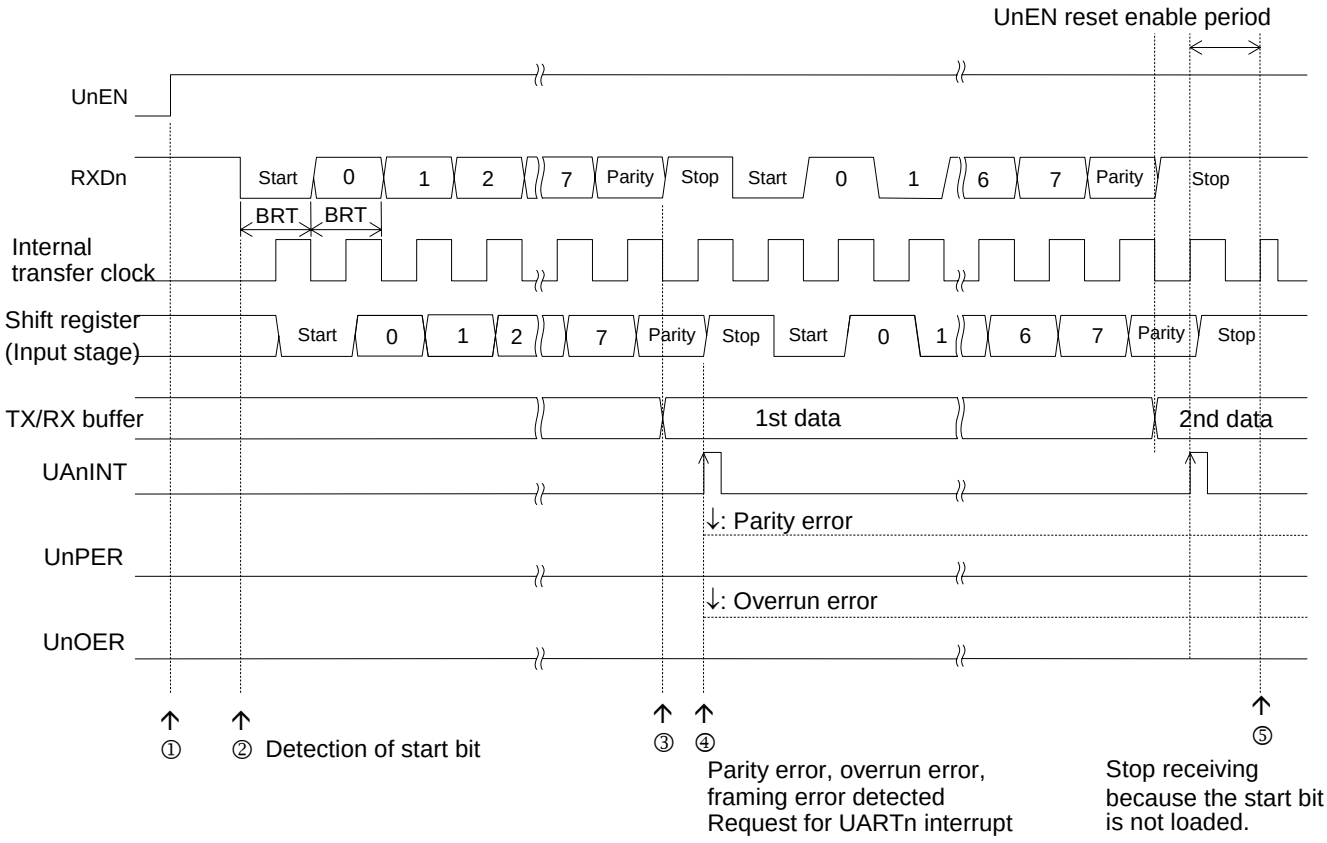


Figure 12-6 Operation Timing in Reception

12.3.5.1 Detection of Start Bit

The Start bit is sampled using the baud rate generator clock HSCLK). Therefore, the start bit detection may be delayed for one cycle of the baud rate generate clock at the maximum.
Figure 12-7 shows the start bit detection timing.

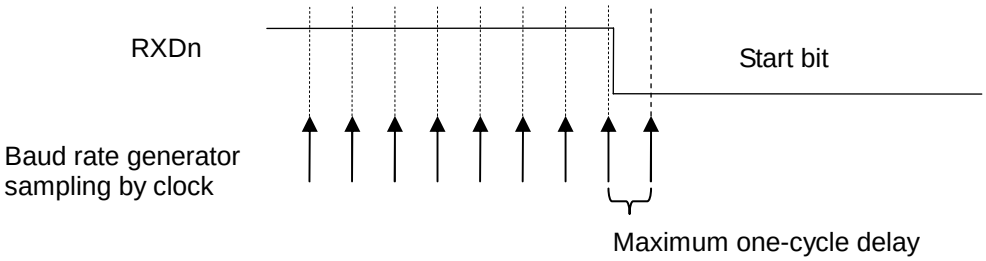
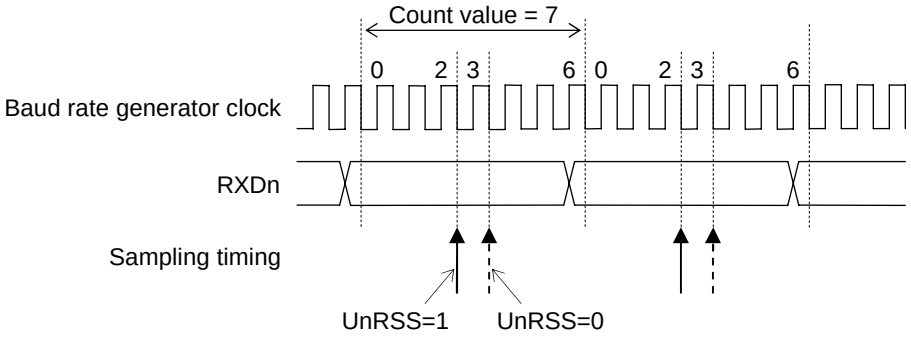


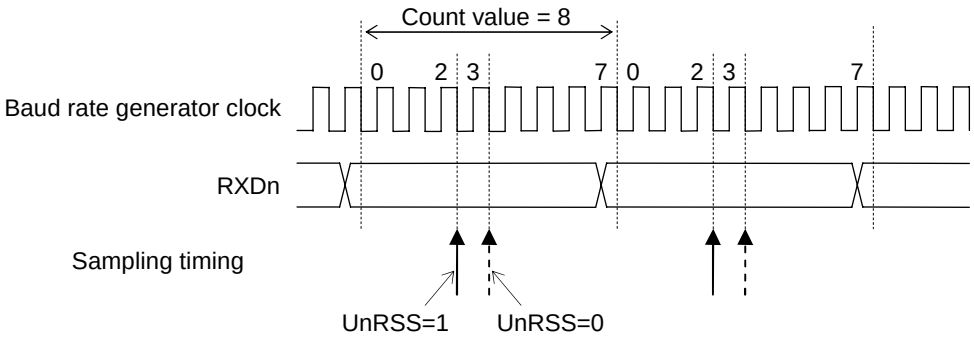
Figure 12-7 Start Bit Detection Timing (Positive Logic)

12.3.5.2 Sampling Timing

When the start bit is detected, the receive data that has been input to RXDn is sampled roughly at the middle of the baud rate and shifted into the shift register.
This sampling timing, where the receive data is sampled to be shifted into the shift register, can be adjusted by one clock pulse of the baud rate generator clock by using the UnRSS bit of the UARTn mode register 0 (UAnMOD0). Figure 12-8 shows the relationship between the UnRSS bit and sampling timing.



(1) When the baud rate generator count value is "7" (odd number)



(2) When the baud rate generator count value is "8" (even number)

Figure 12-8 Relationship between UnRSS Bit and Sampling Timing

12.3.5.3 Reception Margin

If there are any errors between the baud rate on the transmitter side and the baud rate to be generated by the baud rate generator of the LSI, those errors will be accumulated until the last stop bit in one frame is shifted in, causing the reception margin to be reduced.
Figure 12-9 shows the waveform indicating baud rate errors and reception margin.

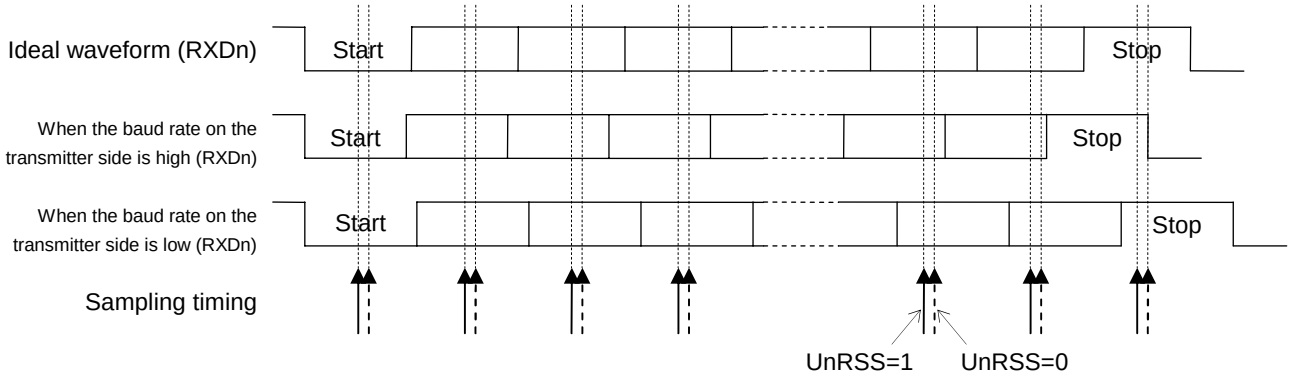


Figure 12-9 Baud Rate Errors and Reception Margin

Note:
When doing system design, ensure enough reception margin taking into account the effects of noise and receive data rounding as well as the difference in baud rate between the transmitter side and receiver side and a delay in the detection of start bit.

12.4 Specifying port registers

To enable the UART function, the applicable bit of each related port register needs to be set. See Chapter 16, "Port B" for detail about the port registers.

12.4.1 Functioning PB1(TXD0) and PB0(RXD0) as the UART

Set the PB1MD1 bit(bit1 of PBMOD1 register) to "1" and set the PB0MD1(bit0 of PBMOD1 register) to "0", and set the PB1MD0-PB0MD0 bits(bit1-0 of PBMOD0 register) to "0", for specifying the UART as the tertiary function of PB1 and the primary function of PB0.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	**PB1MD1**	**PB0MD1**
Setting value	*	*	*	*	*	*	**1**	**0**

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	**PB1MD0**	**PB0MD0**
Setting value	*	*	*	*	*	*	**0**	**0**

Set the PB1C1 bit (bit1 of PBCON1 register) to "1", the PB1C0 bit (bit1 of PBCON0 register) to "1", and the PB1DIR bit (bit1 of PBDIR register) to "0" for specifying the state mode of the PB1 pin to CMOS output.
Set the PB0DIR bit (bit0 of PBDIR register) to "1" for specifying the PB0 as an input pin.
The set value ($) is arbitrary for the PB0C1 and PB0C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB0 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	**PB1C1**	**PB0C1**
Setting value	*	*	*	*	*	*	**1**	**$**

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	**PB1C0**	**PB0C0**
Setting value	*	*	*	*	*	*	**1**	**$**

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	**PB1DIR**	**PB0DIR**
Setting value	*	*	*	*	*	*	**0**	**1**

The PB1D, PB0D bits (bit1-0 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	**PB1D**	**PB0D**
Setting value	*	*	*	*	*	*	****	****

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.2 Functioning PB4(TXD0) and PB5(RXD0) as the UART

Set the PB4MD1(bit4 of PBMOD1 register) to "1" and set the PB5MD1 bit (bit5 of PBMOD1 register) to "0", and set the PB5MD0-PB4MD0 bits(bit5-4 of PBMOD0 register) to "0", for specifying the UART as the primary function of PB5 and the tertiary function of PB4.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7MD1	PB6MD1	**PB5MD1**	**PB4MD1**	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Setting value	*	*	**0**	**1**	*	*	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7MD0	PB6MD0	**PB5MD0**	**PB4MD0**	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Setting value	*	*	**0**	**0**	*	*	*	*

Set the PB4C1 bit (bit4 of PBCON1 register) to "1", the PB4C0 bit (bit4 of PBCON0 register) to "1", and the PB4DIR bit (bit4 of PBDIR register) to "0" for specifying the state mode of the PB4 pin to CMOS output.
Set the PB5DIR bit (bit5 of PBDIR register) to "1" for specifying the PB5 as an input pin.
The set value ($) is arbitrary for the PB5C1 and PB5C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB5 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7C1	PB6C1	**PB5C1**	**PB4C1**	PB3C1	PB2C1	PB1C1	PB0C1
Setting value	*	*	**$**	**1**	*	*	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7C0	PB6C0	**PB5C0**	**PB4C0**	PB3C0	PB2C0	PB1C0	PB0C0
Setting value	*	*	**$**	**1**	*	*	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7DIR	PB6DIR	**PB5DIR**	**PB4DIR**	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Setting value	*	*	**1**	**0**	*	*	*	*

The PB5D, PB4D bit (bit5-4 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7D	PB6D	**PB5D**	**PB4D**	PB3D	PB2D	PB1D	PB0D
Setting value	*	*	**	**	*	*	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

Note:
– The receive pin (RXD) is selected by U0RSEL bit (bit4 of UA0MOD0 register). The initial value "0" selects the PB0 and the value "1" selects the PB5.
– Even if the PB5 pin is selected as RXD0 by the PB5MD1, PB5MD0, PB5C1, PB5C0, and PB5IDR bits, the PB0 pin will be selected as RXD0 when the U0RSEL bit of the UA0MOD0 register is "0".

12.4.3 Functioning PB1(TXD1) and PB2(RXD1) as the UART

Set the PB1MD1 bit(bit1 of PBMOD1 register) to "1" and set the PB2MD1(bit2 of PBMOD1 register) to "0", and set the PB1MD0 bit(bit1 of PBMOD0 register) to "1" and set the PB2MD0(bit2 of PBMOD0 register) to "0", for specifying the UART as the fourthly function of PB1 and the primary function of PB2.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	**PB2MD1**	**PB1MD1**	PB0MD1
Setting value	*	*	*	*	*	**0**	**1**	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	**PB2MD0**	**PB1MD0**	PB0MD0
Setting value	*	*	*	*	*	**0**	**1**	*

Set the PB1C1 bit (bit1 of PBCON1 register) to "1", the PB1C0 bit (bit1 of PBCON0 register) to "1", and the PB1DIR bit (bit1 of PBDIR register) to "0" for specifying the state mode of the PB1 pin to CMOS output.
Set the PB2DIR bit (bit2 of PBDIR register) to "1" for specifying the PB2 as an input pin.
The set value ($) is arbitrary for the PB2C1 and PB2C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB2 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	**PB2C1**	**PB1C1**	PB0C1
Setting value	*	*	*	*	*	**$**	**1**	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	**PB2C0**	**PB1C0**	PB0C0
Setting value	*	*	*	*	*	**$**	**1**	*

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	**PB2DIR**	**PB1DIR**	PB0DIR
Setting value	*	*	*	*	*	**1**	**0**	*

The PB1D, PB2D bits (bit1-2 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	3	**2**	**1**	0
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	**PB2D**	**PB1D**	PB0D
Setting value	*	*	*	*	*	******	******	*

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.4 Functioning PB3(TXD1) and PB2(RXD1) as the UART

Set the PB3MD1 bit (bit3 of PBMOD1 register) to "1" and set the PB2MD1(bit2 of PBMOD1 register) to "0", and set the PB3MD0-PB2MD0 bits(bit3-2 of PBMOD0 register) to "0", for specifying the UART as the tertiary function of PB3 and the primary function of PB2.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	**PB3MD1**	**PB2MD1**	PB1MD1	PB0MD1
Setting value	*	*	*	*	**1**	**0**	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	**PB3MD0**	**PB2MD0**	PB1MD0	PB0MD0
Setting value	*	*	*	*	**0**	**0**	*	*

Set the PB3C1 bit (bit3 of PBCON1 register) to "1", the PB3C0 bit (bit3 of PBCON0 register) to "1", and the PB3DIR bit (bit3 of PBDIR register) to "0" for specifying the state mode of the PB3 pin to CMOS output.
Set the PB2DIR bit (bit2 of PBDIR register) to "1" for specifying the PB2 as an input pin.
The set value ($) is arbitrary for the PB2C1 and PB2C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB2pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	**PB3C1**	**PB2C1**	PB1C1	PB0C1
Setting value	*	*	*	*	**1**	**$**	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	**PB3C0**	**PB2C0**	PB1C0	PB0C0
Setting value	*	*	*	*	**1**	**$**	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	**PB3DIR**	**PB2DIR**	PB1DIR	PB0DIR
Setting value	*	*	*	*	**0**	**1**	*	*

The PB3D, PB2D bit (bit3-2 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	**3**	**2**	1	0
Bit name	PB7D	PB6D	PB5D	PB4D	**PB3D**	**PB2D**	PB1D	PB0D
Setting value	*	*	*	*	******	******	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.5 Functioning PB4(TXD1) and PB2(RXD1) as the UART

Set the PB4MD1 bit(bit4 of PBMOD1 register) to "1" and set the PB2MD1(bit2 of PBMOD1 register) to "0", and set the PB4MD0 bit(bit4 of PBMOD0 register) to "1" and set the PB2MD0(bit2 of PBMOD0 register) to "0", for specifying the UART as the fourthly function of PB4 and the primary function of PB2.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7MD1	PB6MD1	PB5MD1	**PB4MD1**	PB3MD1	**PB2MD1**	PB1MD1	PB0MD1
Setting value	*	*	*	**1**	*	**0**	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7MD0	PB6MD0	PB5MD0	**PB4MD0**	PB3MD0	**PB2MD0**	PB1MD0	PB0MD0
Setting value	*	*	*	**1**	*	**0**	*	*

Set the PB4C1 bit (bit4 of PBCON1 register) to "1", the PB4C0 bit (bit4 of PBCON0 register) to "1", and the PB4DIR bit (bit4 of PBDIR register) to "0" for specifying the state mode of the PB4 pin to CMOS output.
Set the PB2DIR bit (bit2 of PBDIR register) to "1" for specifying the PB2 as an input pin.
The set value ($) is arbitrary for the PB2C1 and PB2C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB2 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7C1	PB6C1	PB5C1	**PB4C1**	PB3C1	**PB2C1**	PB1C1	PB0C1
Setting value	*	*	*	**1**	*	**$**	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7C0	PB6C0	PB5C0	**PB4C0**	PB3C0	**PB2C0**	PB1C0	PB0C0
Setting value	*	*	*	**1**	*	**$**	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7DIR	PB6DIR	PB5DIR	**PB4DIR**	PB3DIR	**PB2DIR**	PB1DIR	PB0DIR
Setting value	*	*	*	**0**	*	**1**	*	*

The PB4D, PB2D bits (bit4 and bit2 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	5	**4**	3	**2**	1	0
Bit name	PB7D	PB6D	PB5D	**PB4D**	PB3D	**PB2D**	PB1D	PB0D
Setting value	*	*	*	******	*	******	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.6 Functioning PB1(TXD1) and PB7(RXD1) as the UART

Set the PB1MD1 bit (bit1 of PBMOD1 register) to "1" and set the PB7MD1(bit7 of PBMOD1 register) to "0", and set the PB1MD0 bit(bit1 of PBMOD0 register) to "1" and set the PB7MD0(bit7 of PBMOD0 register) to "0", for specifying the UART as the fourthly function of PB1 and the primary function of PB7.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	**PB1MD1**	PB0MD1
Setting value	**0**	*	*	*	*	*	**1**	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	**PB1MD0**	PB0MD0
Setting value	**0**	*	*	*	*	*	**1**	*

Set the PB1C1 bit (bit1 of PBCON1 register) to "1", the PB1C0 bit (bit1 of PBCON0 register) to "1", and the PB1DIR bit (bit1 of PBDIR register) to "0" for specifying the state mode of the PB1 pin to CMOS output.
Set the PB7DIR bit (bit7 of PBDIR register) to "1" for specifying the PB7 as an input pin.
The set value ($) is arbitrary for the PB7C1 and PB7C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB7pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7C1**	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	**PB1C1**	PB0C1
Setting value	**$**	*	*	*	*	*	**1**	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	**PB1C0**	PB0C0
Setting value	**$**	*	*	*	*	*	**1**	*

Register name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7DIR**	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	**PB1DIR**	PB0DIR
Setting value	**1**	*	*	*	*	*	**0**	*

The PB1D, PB7D bit (bit1and bit7 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	3	2	**1**	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	PB3D	PB2D	**PB1D**	PB0D
Setting value	******	*	*	*	*	*	******	*

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.7 Functioning PB3(TXD1) and PB7(RXD1) as the UART

Set the PB3MD1 bit(bit3 of PBMOD1 register) to "1" and set the PB7MD1(bit7 of PBMOD1 register) to "0", and set the PB3MD0, PB7MD0 bits(bit3 and bit7 of PBMOD0 register) to "0", for specifying the UART as the tertiary function of PB3 and the primary function of PB7.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	**PB3MD1**	PB2MD1	PB1MD1	PB0MD1
Setting value	**0**	*	*	*	**1**	*	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	**PB3MD0**	PB2MD0	PB1MD0	PB0MD0
Setting value	**0**	*	*	*	**0**	*	*	*

Set the PB3C1 bit (bit3 of PBCON1 register) to "1", the PB3C0 bit (bit3 of PBCON0 register) to "1", and the PB3DIR bit (bit3 of PBDIR register) to "0" for specifying the state mode of the PB3 pin to CMOS output.
Set the PB7DIR bit (bit7 of PBDIR register) to "1" for specifying the PB7 as an input pin.
The set value ($) is arbitrary for the PB7C1 and PB7C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB7 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7C1**	PB6C1	PB5C1	PB4C1	**PB3C1**	PB2C1	PB1C1	PB0C1
Setting value	**$**	*	*	*	**1**	*	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	**PB3C0**	PB2C0	PB1C0	PB0C0
Setting value	**$**	*	*	*	**1**	*	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7DIR**	PB6DIR	PB5DIR	PB4DIR	**PB3DIR**	PB2DIR	PB1DIR	PB0DIR
Setting value	**1**	*	*	*	**0**	*	*	*

The PB3D, PB7D bits (bit3 and bit7 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	**3**	2	1	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	**PB3D**	PB2D	PB1D	PB0D
Setting value	******	*	*	*	******	*	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

12.4.8 Functioning PB4(TXD1) and PB7(RXD1) as the UART

Set the PB4MD1 bit (bit4 of PBMOD1 register) to "1" and set the PB7MD1(bit7 of PBMOD1 register) to "0", and set the PB4MD0 bit(bit4 of PBMOD0 register) to "1" and set the PB7MD0(bit7 of PBMOD0 register) to "0", for specifying the UART as the fourthly function of PB4 and the primary function of PB7.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	**PB4MD1**	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Setting value	**0**	*	*	**1**	*	*	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	**PB4MD0**	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Setting value	**0**	*	*	**1**	*	*	*	*

Set the PB4C1 bit (bit4 of PBCON1 register) to "1", the PB4C0 bit (bit4 of PBCON0 register) to "1", and the PB4DIR bit (bit4 of PBDIR register) to "0" for specifying the state mode of the PB4 pin to CMOS output.
Set the PB7DIR bit (bit7 of PBDIR register) to "1" for specifying the PB7 as an input pin.
The set value ($) is arbitrary for the PB7C1 and PB7C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB7pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7C1**	PB6C1	PB5C1	**PB4C1**	PB3C1	PB2C1	PB1C1	PB0C1
Setting value	**$**	*	*	**1**	*	*	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	**PB4C0**	PB3C0	PB2C0	PB1C0	PB0C0
Setting value	**$**	*	*	**1**	*	*	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7DIR**	PB6DIR	PB5DIR	**PB4DIR**	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Setting value	**1**	*	*	**0**	*	*	*	*

The PB4D, PB7D bit (bit4and bit7 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	**4**	3	2	1	0
Bit name	**PB7D**	PB6D	PB5D	**PB4D**	PB3D	PB2D	PB1D	PB0D
Setting value	******	*	*	******	*	*	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

Note:
– The receive pin (RXD) is selected by U1RSEL bit (bit4 of UA1MOD0 register). The initial value "0" selects the PB2 and the value "1" selects the PB7.
– Even if the PB7 pin is selected as RXD1 by the PB7MD1, PB7MD0, PB7C1, PB7C0, and PB7IDR bits, the PB2 pin will be selected as RXD1 when the U1RSEL bit of the UA1MOD0 register is "0".

Chapter 13

I^2C Bus Interface Master

13 I²C Bus Interface Master

13.1 Overview

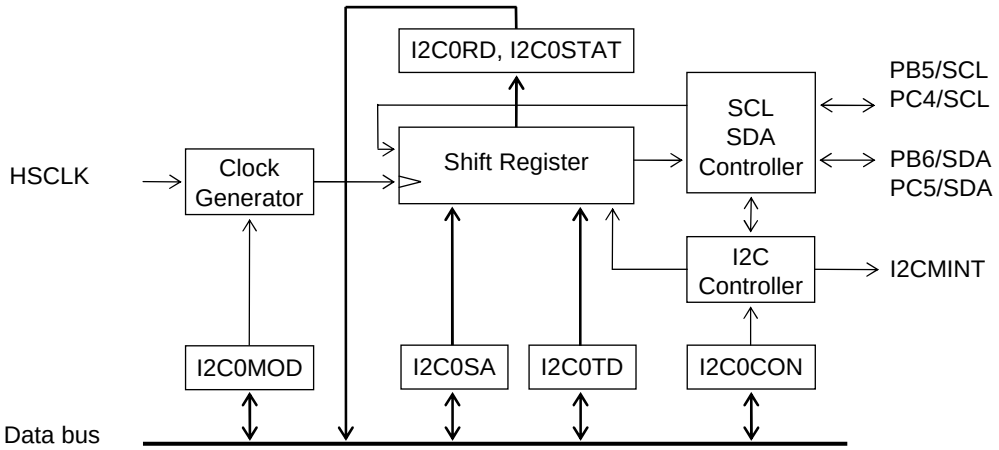
This LSI includes 1 channel of I²C bus interface (master).
The tertiary functions of Port B or the secondary functions of Port C are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For PortB, see Chapter 16, "PortB". For PortC see Chapter 17 "PortC".

13.1.1 Features

- Master function
- Communication speeds supported include standard mode (100kbps @8MHz HSCLK) and fast mode (400kbps @8MHz HSCLK).
- Allows support for arbitration function (multi-master) and clock synchronization (handshake).
- 7-bit address format (10-bit address can be supported)

13.1.2 Configuration

Figure 13-1 shows the configuration of the I²C bus interface.



I2C0RD : I²C bus 0 receive register
I2C0SA : I²C bus 0 slave address register
I2C0TD : I²C bus 0 transmit data register
I2C0CON : I²C bus 0 control register
I2C0MOD : I²C bus 0 mode register
I2C0STAT : I²C bus 0 status register

Figure 13-1 Configuration of I²C Bus Interface

13.1.3 List of Pins

Pin name	I/O	Description
PB6/SDA	I/O	I²C bus interface data input/output pin. Used for the tertiary function of the PB6 pin.
PB5/SCL	I/O	I²C bus interface clock input/output pin. Used for the tertiary function of the PB5 pin.
PC5/SDA	I/O	I²C bus interface data input/output pin. Used for the secondary function of the PC5 pin.
PC4/SCL	I/O	I²C bus interface clock input/output pin. Used for the secondary function of the PC4 pin.

PC4/PC5 are only used by ML610Q112.

13.2 OverviewDescription of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A0H	I^2C bus 0 receive register	I2C0RD	—	R	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H

13.2.2 I²C Bus 0 Receive Register (I2C0RD)

Address: 0F2A0H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0RD	I20R7	I20R6	I20R5	I20R4	I20R3	I20R2	I20R1	I20R0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0RD is a read-only special function register (SFR) to store receive data.
I2C0RD is updated after completion of each reception.

[Description of Bits]

- **I20R7-I20R0** (bits 7 to 0)

  The I20R7 to I20R0 bits are used to store receive data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

13.2.3 I²C Bus 0 Slave Address Register (I2C0SA)

Address: 0F2A1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0SA	I20A6	I20A5	I20A4	I20A3	I20A2	I20A1	I20A0	I20RW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

- **I20RW** (bit 0)
  The I20RW bit is used to select the data transmit mode (write) or data receive mode (read).

I20RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

- **I20A6-I20A0** (bits 7 to 1)
  The I20A6 to I20A0 bits are used to set the address of the communication destination.

13.2.4 I²C Bus 0 Transmit Data Register (I2C0TD)

Address: 0F2A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0TD	I20T7	I20T6	I20T5	I20T4	I20T3	I20T2	I20T1	I20T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0TD is a special function register (SFR) to set transmit data.

[Description of Bits]

- **I20T7-0** (bits 7 to 0)
  The I20T7 to 0 bits are used to set transmit data.

13.2.5 I²C Bus 0 Control Register (I2C0CON)

Address: 0F2A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0CON	I20ACT	—	—	—	—	I20RS	I20SP	I20ST
R/W	R/W	R	R	R	R	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I20ST** (bit 0)

The I20ST bit is used to control the communication operation of the I²C bus interface. When the I20ST bit is set to "1", communication starts. When "1" is overwritten to the I20ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication starts again. When the I20ST bit is set to "0", communication is stopped forcibly.
The I20ST bit can be set to "1" only when the I2C bus interface is in an operation enable state (I20EN = "1").
When the I20SP bit is set to "1", the I20ST bit is set to "0".

I20ST	Description
0	Stops communication (initial value)
1	Starts communication

- **I20SP** (bit 1)

The I20SP bit is a write-only bit used to request a stop condition. When the I20SP bit is set to "1", the I²C bus shifts to the stop condition and communication stops. When the I20SP bit is read, "0" is always read.

I20SP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I20RS** (bit 2)

The I20RS bit is a write-only bit used to request a repeated start. When this bit is set to "1" during data communication, the I²C bus shifts to the repeated start condition and communication restarts from the slave address. I20RS can be set to "1" only while communication is active (I20ST ="1"). When the I20RS bit is read, "0" is always read.

I20RS	Description
0	No repeated start request (initial value)
1	Repeated start request

- **I20ACT** (bit 7)

The I20ACT bit is used to set the acknowledge signal to be output at completion of reception.

I20ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

Note:
When another master is connected to the I²C-bus, please check the bus is free with the I20BB flag of I2C0STAT before starting communication.

13.2.6 I²C Bus 0 Mode Register (I2C0MOD)

Address: 0F2A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0MOD	—	—	—	I20SYN	I20DW1	I20DW0	I20MD	I20EN
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

- **I20EN** (bit 0)

The I20EN bit is used to enable the operation of the I²C bus interface. Only when the I20EN bit is set to "1", the I20ST bit can be set and the I20BB flag starts operation. When the I20EN bit is set to "0", all the SFRs related to the I²C bus 0 are initialized.

I20EN	Description
0	Stops I²C operation. (Initial value)
1	Enables I²C operation.

- **I20MD** (bit 1)

The I20MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected.

I20MD	Description
0	Standard mode (initial value)/ 100kbps@8MHz HSCLK
1	Fast mode / 400kbps@8MHz HSCLK

- **I20DW1, I20DW0** (bits 3, 2)

The I20DW1 and I20DW0 bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kpbs/400kpbs.

I20DW1	I20DW0	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

- **I20SYN** (bit 4)

The I20SYN bit is used to select whether or not to use the clock synchronization function (handshake function). When using the clock synchronization function or using a multi-master, set this bit to "1"

I20SYN	Description
0	Clock synchronization is not used. (Initial value)
1	Clock synchronization is used.

Note:
The I²C bus is set so that the communication speed may become 100kbps/400kbps when HSCLK is 8 MHz.

13.2.7 I²C Bus 0 Status Register (I2C0STAT)

Address: 0F2A5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0STAT	—	—	—	—	—	I20ER	I20ACR	I20BB
R/W	R	R	R	R	R	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C0STAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

[Description of Bits]

- **I20BB** (bit 0)

The I20BB bit is used to indicate the state of use of the I²C bus interface. When the start condition is generated on the I²C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". In multi-master mode, this bit is set to "1" even if another master device is using the I²C bus. The I20BB bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20BB	Description
0	I²C bus-free state (Initial value)
1	I²C bus-busy state

- **I20ACR** (bit 1)

The I20ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I20ACR bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

- **I20ER** (bit 2)

The I20ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". When clock synchronization is used (I20SYN = "1"), if the I20ER bit is set to "1", the SDA pin output is disabled until the subsequent byte data communication terminates. When clock synchronization is not used (I20SYN = "0"), The SDA pin remains the output until the subsequent byte data communication terminates even if I20ER is set to "1".
The I20ER bit is set to "0" when a write operation to I2C0CON is performed. The I20ER bit is set to "0" when the I20EN bit of I2C0MOD is set to "0".

I20ER	Description
0	No transmit error (initial value)
1	Transmit error

13.3 Description of Operation

13.3.1 Communication Operating Mode

Communication is started when communication mode is selected by using the I²C bus 0 mode register (I2C0MOD), the I²C function is enabled by using the I20EN bit, a slave address and a data communication direction are set in the I²C bus 0 slave address register, and "1" is written to the I20ST bit of the I2C bus 0 control register (I2C0CON).

13.3.1.1 Start Condition

When "1" is written to the I20ST bit of the I²C bus 0 control register ((I2C0CON) while communication is stopped (the I20ST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to slave address transmit mode.

13.3.1.2 Repeated Start Condition

When "1" is written to the I20RS and I20ST bits of the I²C bus 0 control register ((I2C0CON) during communication (the I20ST bit is "0"), the repeated start condition waveform is output to the SDA and SCL pins.
After execution of the repeated start condition, the LSI shifts to slave address transmit mode.

13.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus 0 slave address register (I2C0SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0SA output from the SDA pin is stored in I2C0RD.

13.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C0TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0TD output from the SDA pin is stored in I2C0RD.

13.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I20ACT bit of the I2C bus 0 control register (I2C0CON) is output as an acknowledge signal. At completion of acknowledgment transmission, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The data received is stored in I2C0RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).

13.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I²C bus interface interrupt (I2CMINT) is generated.
In the control register setting wait state, the transmit flag (I20ER) of the I²C bus 0 status register (I2C0STAT) and acknowledgment receive data (I20ACR) are confirmed and at data reception, the contents of I2C0RD are read in the CPU and the next operation mode is selected.
When "1" is written to the I20ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I20SP bit, the LSI shifts to the stop condition. When "1" is written to the I20RS bit and I20ST bit, the operation shifts to the repeated start condition.

13.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I²C bus interface interrupt (I2CMINT) is generated.

13.3.2 Communication Operation Timing

Figures 13-2 to 13-4 show the operation timing and control method for each communication mode.

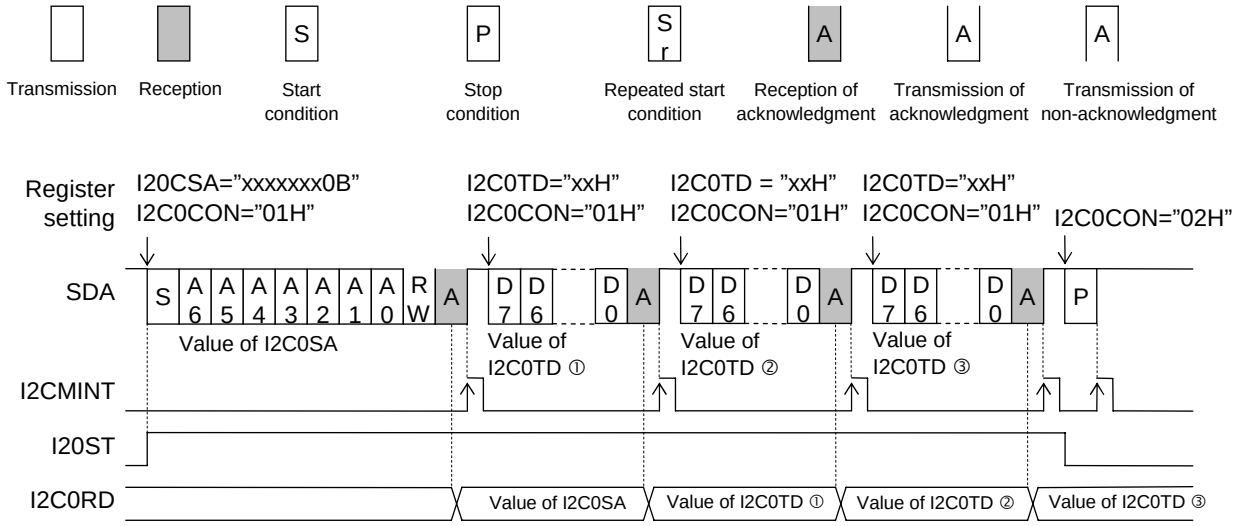


Figure 13-2 Operation Timing in Data Transmit (Write)

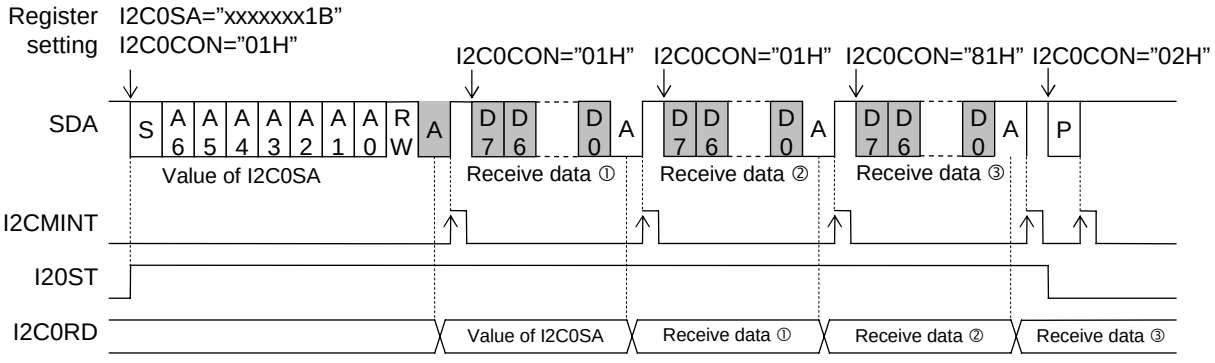


Figure 13-3 Operation Timing in Data Receive (Read)

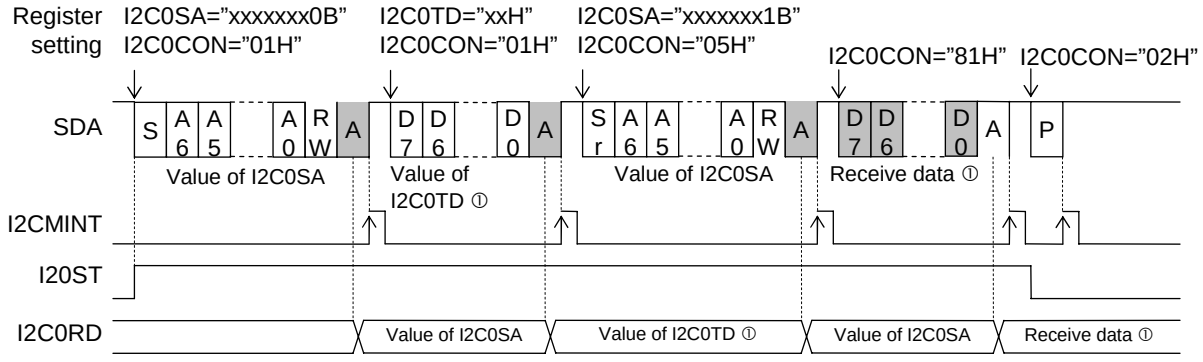


Figure 13-4 Operation Timing at Data Transmit/Receive (Write/Read) Switching

Figure 13-5 shows the operation timing and control method when an acknowledgment error occurs.

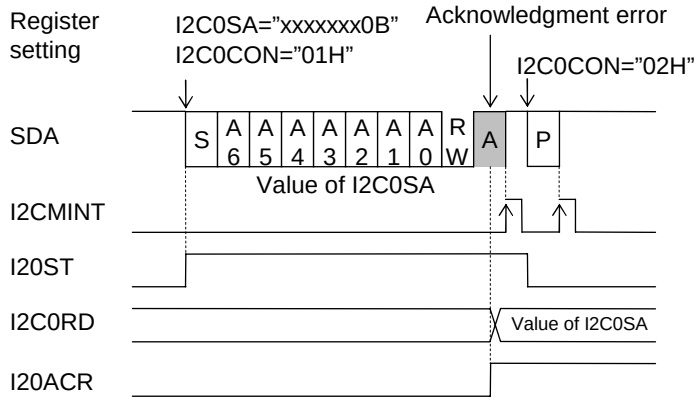


Figure 13-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide (transmit failure due to arbitration when a multi-masters is used), the I20ER bit of the I2C bus 0 status register (I2C0STAT) is set to "1" and SDA pin remains the output until termination of the subsequent byte data communication.
Figure 13-6 shows the operation timing and control method when transmission fails.

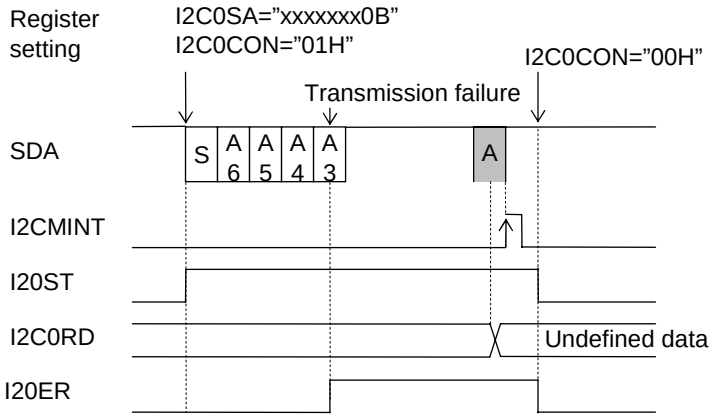


Figure 13-6 Operation Timing When Transmission Fails

13.3.3 Operation Waveforms

Figure 13-7 shows the operation waveforms of the SDA and SCL signals and the I20BB flag. Table 13-1 shows the relationship between communication speeds and HSCLK clock counts.

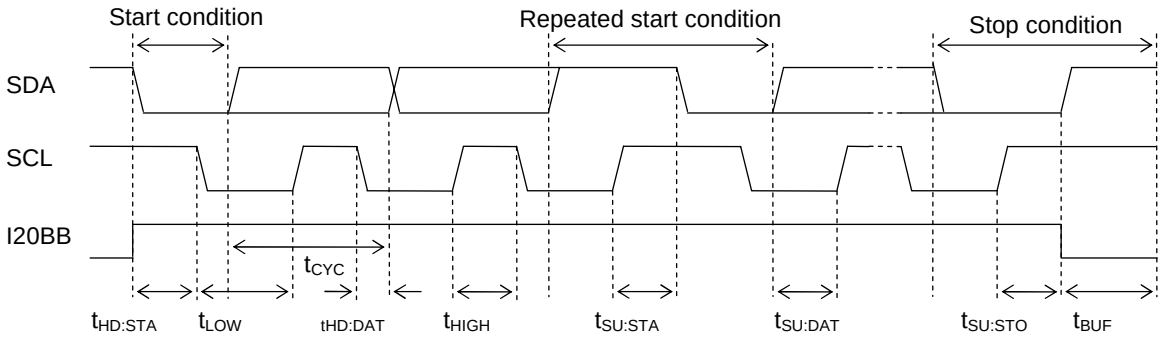


Figure 13-7 Operation Waveforms of SDA and SCL Signals and I20BB Flag

Table 13-1 Relationship between Communication Speeds and HSCLK Clock Counts

Communication speed (I20SP)	Speed reduction (I20DW1, 0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100 kbps	No reduction	80ϕ	36ϕ	44ϕ	8ϕ	36ϕ	44ϕ	36ϕ	36ϕ	44ϕ
	10% reduction	88ϕ	40ϕ	48ϕ	8ϕ	40ϕ	48ϕ	40ϕ	40ϕ	48ϕ
	20% reduction	96ϕ	44ϕ	52ϕ	8ϕ	44ϕ	52ϕ	44ϕ	44ϕ	52ϕ
	30% reduction	104ϕ	48ϕ	56ϕ	8ϕ	48ϕ	56ϕ	48ϕ	48ϕ	56ϕ
Fast mode 400 kbps	No reduction	20ϕ	8ϕ	12ϕ	4ϕ	8ϕ	12ϕ	8ϕ	8ϕ	12ϕ
	10% reduction	22ϕ	8ϕ	14ϕ	4ϕ	8ϕ	14ϕ	10ϕ	8ϕ	14ϕ
	20% reduction	24ϕ	10ϕ	14ϕ	4ϕ	10ϕ	14ϕ	10ϕ	10ϕ	14ϕ
	30% reduction	26ϕ	10ϕ	16ϕ	4ϕ	10ϕ	16ϕ	12ϕ	10ϕ	16ϕ

ϕ: Period of high-speed clock (HSCLK)

Note
The HSCLK clock count is set so that the communication speed may be set to 100kbps/400kbps when HSCLK is 8 MHz. When the high-speed clock frequency is not 8 MHz, select an I2C0MOD communication speed reduction rate and an FCON0 HSCLK frequency so that the communication speed may not exceed 100kbps/400kbps.
When the slave device is used to the clock synchronization function(handshake) which is hold to "L" level to the SCL signal, the t_{CYC} and t_{LOW} period is extended.

13.4 Specifying port registers

To enable the I²C function, the applicable bit of each related port register needs to be set. See Chapter 16, "Port B" and Chapter 17, "Port C" for detail about the port registers.

13.4.1 Functioning PB5(SCL) and PB6(SDA) as the I2C

Set PB6MD1 to PB5MD1 bit (bit6-5 of PBMOD1 register) to "1", and PB6MD0 to PB5MD0 bit (bit6-5 of PBMOD0 register) to "0", for specifying the I2C as the tertiary function of PB5 and PB6.

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7MD1	**PB6MD1**	**PB5MD1**	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	*	**1**	**1**	*	*	*	*	*

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7MD0	**PB6MD0**	**PB5MD0**	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	*	**0**	**0**	*	*	*	*	*

Set PB6C1-PB5C1 bit(bit6-5 of PBCON1 register) to "1", set PB6C0-PB5C0 bit(bit6-5 of PBCON0 register) to "0", and set PB6DIR-PB5DIR bit(bit6-5 of PBDIR register) to "0", for specifying the PB6 and PB5 as Nch open-drain output. The open-drain/open-collector outputs are required on the I2C bus line to avoid collision between H level and L level.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7C1	**PB6C1**	**PB5C1**	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	*	**1**	**1**	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7C0	**PB6C0**	**PB5C0**	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	*	**0**	**0**	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7DIR	**PB6DIR**	**PB5DIR**	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	*	**0**	**0**	*	*	*	*	*

Data of PB6D-PB5D bits (bit6-5 of PBD register) do not affect to the I2C function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7D	**PB6D**	**PB5D**	PB4D	PB3D	PB2D	PB1D	PB0D
Data	*	******	******	*	*	*	*	*

* : Bit not related to the I2C bus interface function
** : Don't care the data

Chapter 14

I^2C Bus Interface Slave

14 I²C Bus Interface Slave

14.1 Overview

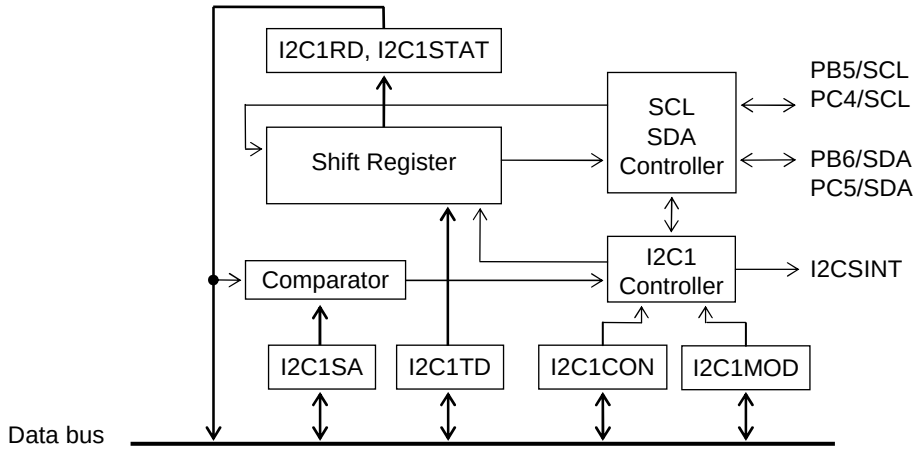
This LSI includes 1 channel of I²C bus interface (slave).
The tertiary functions of Port B or the secondary functions of Port C are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For PortB, see Chapter 16, "Port B". For PortC see Chapter 17 "PortC".

14.1.1 Features

- Slave function
- Communication speeds supported include standard mode (100 kbps)
- Support for clock synchronization (handshake).

14.1.2 Configuration

Figure 14-1 shows the configuration of the I²C bus interface.



I2C1RD : I²C bus 1 receive register
I2C1SA : I²C bus 1 slave address register
I2C1TD : I²C bus 1 transmit data register
I2C1CON : I²C bus 1 control register
I2C1MOD : I²C bus 1 mode register
I2C1STAT : I²C bus 1 status register

Figure 14-1 Configuration of I²C Bus Interface

14.1.3 List of Pins

Pin name	I/O	Description
PB6/SDA	I/O	I²C bus interface data input/output pin. Used for the tertiary function of the PB6 pin.
PB5/SCL	I/O	I²C bus interface clock input/output pin. Used for the tertiary function of the PB5 pin.
PC5/SDA	I/O	I²C bus interface clock input/output pin. Used for the secondary function of the PC5 pin.
PC4/SCL	I/O	I²C bus interface clock input/output pin. Used for the secondary function of the PC4 pin.

Note:
The PC5/SDA and PC4/SCL pins are only used by ML610Q112.

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A8H	I^2C bus 1 receive register	I2C1RD	—	R	8	00H
0F2A9H	I^2C bus 1 slave address register	I2C1SA	—	R/W	8	00H
0F2AAH	I^2C bus 1 transmit data register	I2C1TD	—	R/W	8	00H
0F2ABH	I^2C bus 1 control register	I2C1CON	—	R/W	8	00H
0F2ACH	I^2C bus 1 mode register	I2C1MOD	—	R/W	8	00H
0F2ADH	I^2C bus 1 status register	I2C1STAT	—	R	8	00H

14.2.2 I²C Bus 1 Receive Register (I2C1RD)

Address: 0F2A8H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1RD	I21R7	I21R6	I21R5	I21R4	I21R3	I21R2	I21R1	I21R0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C1RD is a read-only special function register (SFR) to store receive data.
I2C1RD is updated after completion of each reception.

[Description of Bits]

- **I21R7-I21R0** (bits 7 to 0)

  The I21R7 to I21R0 bits are used to store receive data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

14.2.3 I²C Bus 1 Slave Address Register (I2C1SA)

Address: 0F2A9H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1SA	I21A6	I21A5	I21A4	I21A3	I21A2	I21A1	I21A0	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

I2C1SA is a special function register (SFR) to set the slave address.

[Description of Bits]

- **I21A6-I21A0** (bits 7 to 1)
  The I21A6 to I21A0 bits are used to set the slave address of the communication destination.

14.2.4 I²C Bus 1 Transmit Data Register (I2C1TD)

Address: 0F2AAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1TD	I21T7	I21T6	I21T5	I21T4	I21T3	I21T2	I21T1	I21T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C1TD is a special function register (SFR) to set transmit data.

[Description of Bits]

- **I21T7-I21T0** (bits 7 to 0)
  The I21T7 to I21T0 bits are used to set transmit data.

14.2.5 I²C Bus 1 Control Register (I2C1CON)

Address: 0F2ABH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1CON	I21ACT	—	I21WT	—	—	—	—	—
R/W	R/W	R/W	W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C1CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I21WT** (bit 5)

The I21WT bit is a write-only bit used to cancel the waiting status for communication (output "L" level to SCL pin). When this bit is set to "1" during the waiting status for communication, it cancel the waiting status. This bit always returns "0" for read.

I21WT	Description
0	Do not cancel the wait (initial value)
1	Cancel the wait

- **I21ACT** (bit 7)

The I21ACT bit is used to set the acknowledge signal to be output at completion of reception.

I21ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

14.2.6 I²C Bus 1 Mode Register (I2C1MOD)

Address: 0F2ACH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1MOD	—	I21SIE	I21PIE	—	—	—	—	I21EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C1MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

- **I21EN** (bit 0)

The I21EN bit is used to enable the operation of the I²C bus interface. When the I21EN bit is set to "1", it enables the operation of I²C bus 1. When the I21EN bit is set to "0", all bits of I²C bus 1 status register (I2C1STAT) is initialized by "0", and I²C bus 1 stop the operation.

I21EN	Description
0	Stops I²C operation. (Initial value)
1	Enables I²C operation.

- **I21PIE** (bit 5)

The I21PIE bit is used to select enable or disable the stop condition interrupt.

I21PIE	Description
0	Disables the stop condition interrupt. (Initial value)
1	Enables the stop condition interrupt.

- **I21SIE** (bit 6)

The I21SIE bit is used to select enable or disable of start condition interrupt.

I21SIE	Description
0	Disables the start condition interrupt. (Initial value)
1	Enables the start condition interrupt.

14.2.7 I²C Bus 1 Status Register (I2C1STAT)

Address: 0F2ADH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1STAT	—	—	—	I21TR	I21SAA	I21ER	I21ACR	I21BB
R/W	R	R	R	R	R	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C1STAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

[Description of Bits]

- **I21BB** (bit 0)

The I21BB bit is used to indicate the state of use of the I²C bus interface. When the start condition is generated on the I²C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". The I21BB bit is set to "0" when the I21EN bit of I2C1MOD is "0".

I21BB	Description
0	I²C bus-free state (Initial value)
1	I²C bus-busy state

- **I21ACR** (bit 1)

The I21ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I21ACR bit is set to "0" when the I21EN bit of I2C1MOD is "0".

I21ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

- **I21ER** (bit 2)

The I21ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". When the I21ER bit is set to "1", the SDA pin output is disabled until the subsequent byte data communication terminates.
The I21ER bit is set to "0" when a write operation to I2C1CON is performed. The I21ER bit is set to "0" when the I21EN bit of I2C1MOD is set to "0".

I21ER	Description
0	No transmit error (initial value)
1	Transmit error

- **I21SAA** (bit 3)

The I21SAA bit indicates that this device is specified as a slave address. The I21SAA bit is set to "1" if the slave address that a master device outputs, and content of I2C1SA register are the same. The I21SAA bit is set to "0" if I21EN bit of I2C1MOD registers is cleared.

I21SAA	Description
0	Contents of I2C1SA register did Not match to slave address specified by master device (initial value)
1	Contents of I2C1SA register matched to slave address specified by master device

- **I21TR** (bit 4)

The I21TR bit indicates status of transmission and receive. The I21TR bit is set to "1" when detecting data direction bit is "1". The I21TR bit is reset to "0" when detecting stop condition, start condition, data direction bit is "0" and when I21EN bit of I2C1MOD0 is "0".

I21TR	Description
0	Receive state. (initial value)
1	Transmit state.

14.3 Description of Operation

14.3.1 Communication Operating Mode

The receive starts enabled after a slave address is specified to I2C1SA register, start and stop condition interrupts are set to enabled by using I2C1MOD register and set the I21EN bit to "1".

14.3.1.1 Start Condition

When a start condition data comes to the SDA and SCL pin, the I21BB bit of I2C1STAT register is set to "1" and the LSI starts the receive operation. It goes to slave address receive mode after the start condition completed. I2C bus 1 interface iterrupt (I2CSINT) occurs if the start condition interrupt is enabled by setting the I21SIE bit of I2C1MOD.

14.3.1.2 Slave Address Receive Mode

In slave address receive mode, the values (slave address and data communication direction) provided to the SDA pin is received synchronizing at the rising edge of serial clock provided to the SCL pin.
If the received slave address and data set to I2C1SA register matched, the I21SAA bit gets to "1" and latches the data direction bit to the I21TR bit of I2C1STAT register, then return the acknowledge data ("L" level).
After detecting a falling edge of the SCL pin, it moves to the communication wait mode and makes the I2C bus 1 interface interrupt (I2CSINT).
When the received slave addess and data set to I2C1SA register does not match, the I21AA bit remains "0" and no operation starts.

14.3.1.3 Communication Wait State

The LSI ties the SCL pin to "L" level and makes the communication waiting status.
In data receive mode after preparation for the next data is completed, it cancel the communication wait state by setting the I21WT bit of I2C1CON register.
In data transmit mode, after setting the next data to I2C1RD register, the I21WT bit is set to "1" and cancel the communication wait state.

14.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C1TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I21ACR bit of the I2C bus 1 status register (I2C1STAT).
The device go into the communication wait state after detecting a falling edge of clock provided to the SCL pin while receiving the acknowledge data, and at the same time the I2C bus 1 interface interrupt (I2CSINT) occurs.
The value of I2C1TD output from the SDA pin is stored in I2C1RD.

14.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I21ACT bit of the I2C bus 1 control register (I2C1CON) is output as an acknowledge signal.
The device go into the communication wait state after detecting a falling edge of clock provided to the SCL pin while receiving the acknowledge data, and at the same time the I2C bus 1 interface interrupt (I2CSINT) occurs.
The received data is stored to I2C1RD register and the acknowledge output is received to the I21ACR bit of the I2C bus 1 status register (I2C1STAT).

14.3.1.6 Stop Condition

When the stop condition data is proveided to the SDA and SCL pin, the I21BB bit of the I2C bus 1 status register (I2C1STAT) is get to "0", and the device stop operation. Also, if the stop condition interrupt is enabled by setting the I21PIE bit of the I2C bus 1 mode register (I2C1MOD), the I2C bus interface (slave) interrupt (I2CSINT) occurs.

14.3.2 Communication Operation Timing

Figures 14-2 to 14-4 show the operation timing and control method for each communication mode.

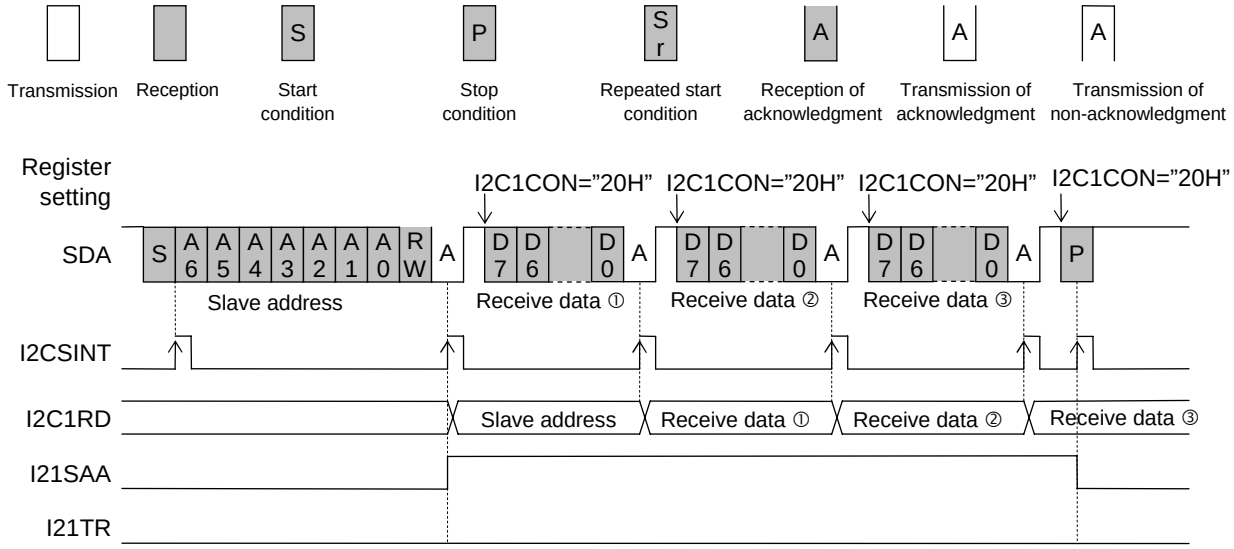


Figure 14-2 Operation Timing in Data Receive (Read)

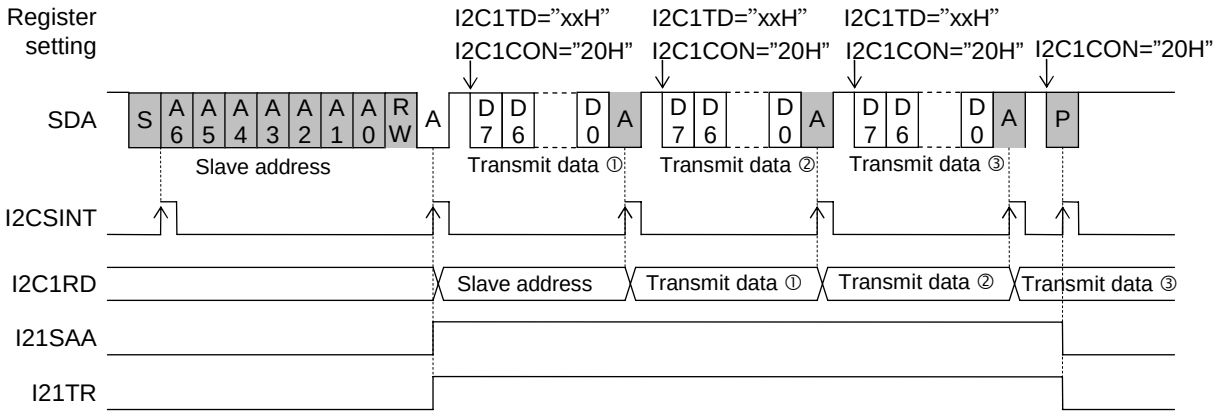


Figure 14-3 Operation Timing in Data Transmit (Write)

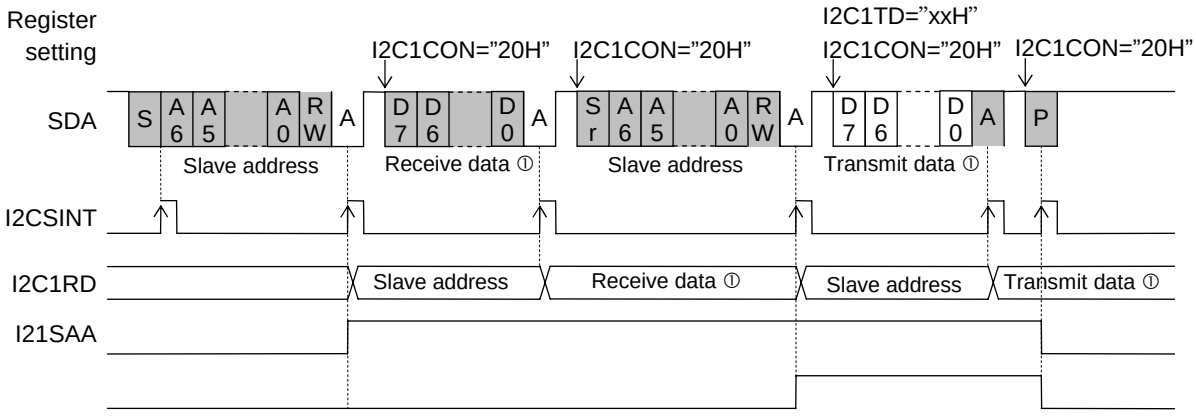


Figure 14-4 Operation Timing at Data Transmit/Receive (Write/Read) Switching

When the values of the transmitted bit and the SDA pin do not coincide, the I21ER bit of the I2C bus 1 status register (I2C0STAT) is set to "1" and SDA pin remains the output until termination of the subsequent byte data communication. I21ER bit is initialized to "0" by writing I²C Bus 1 Control Register (I2C1CON).
Figure 14-5 shows the operation timing and control method when transmission fails.

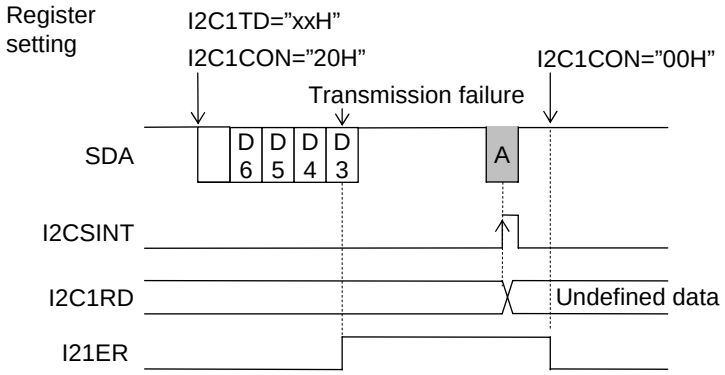


Figure 14-5 Operation Timing When Transmission Fails

14.3.3 Operation Waveforms

Figure 14-6 shows the operation waveforms of the SDA and SCL signals and the I21BB flag.

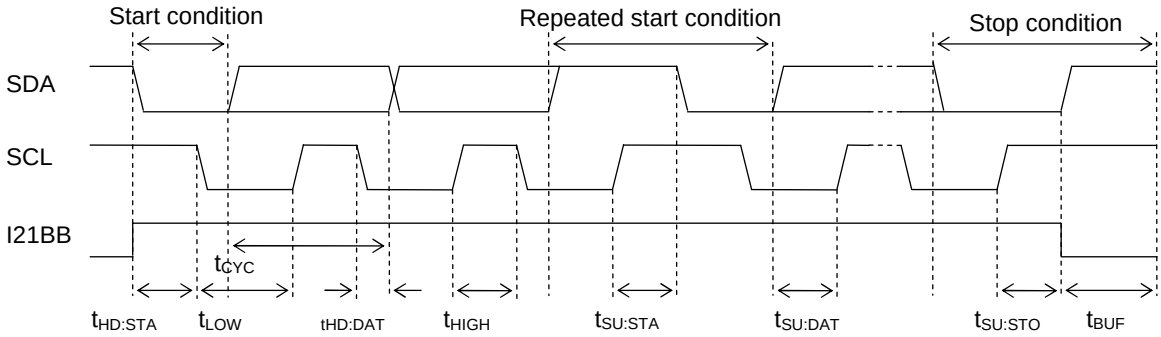


Figure 14-6 Operation Waveforms of SDA and SCL Signals and I21BB Flag

14.4 Specifying port registers

To enable the I²C function, the applicable bit of each related port register needs to be set. See Chapter 16, "Port B" and Chapter 17, "Port C" for detail about the port registers.

14.4.1 Functioning PB5(SCL) and PB6(SDA) as the I2C

Set PB6MD1 to PB5MD1 bit (bit6-5 of PBMOD1 register) to "1", and PB6MD0 to PB5MD0 bit (bit6-5 of PBMOD0 register) to "0", for specifying the I2C as the tertiary function (I²C bus data/clock output) of PB5 and PB6.

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7MD1	**PB6MD1**	**PB5MD1**	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	*	**1**	**1**	*	*	*	*	*

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7MD0	**PB6MD0**	**PB5MD0**	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	*	**0**	**0**	*	*	*	*	*

Set PB6C1-PB5C1 bit(bit6-5 of PBCON1 register) to "1", set PB6C0-PB5C0 bit(bit6-5 of PBCON0 register) to "0", and set PB6DIR-PB5DIR bit(bit6-5 of PBDIR register) to "0", for specifying the PB6 and PB5 as Nch open-drain output. The open-drain/open-collector outputs are required on the I2C bus line to avoid collision between H level and L level.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7C1	**PB6C1**	**PB5C1**	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	*	**1**	**1**	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7C0	**PB6C0**	**PB5C0**	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	*	**0**	**0**	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7DIR	**PB6DIR**	**PB5DIR**	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	*	**0**	**0**	*	*	*	*	*

Data of PB6D-PB5D bits (bit6-5 of PBD register) do not affect to the I2C function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	7	**6**	**5**	4	3	2	1	0
Bit name	PB7D	**PB6D**	**PB5D**	PB4D	PB3D	PB2D	PB1D	PB0D
Data	*	******	******	*	*	*	*	*

* : Bit not related to the I2C bus interface function
** : Don't care the data

Chapter 15

Port A

15 Port A

15.1 Overview

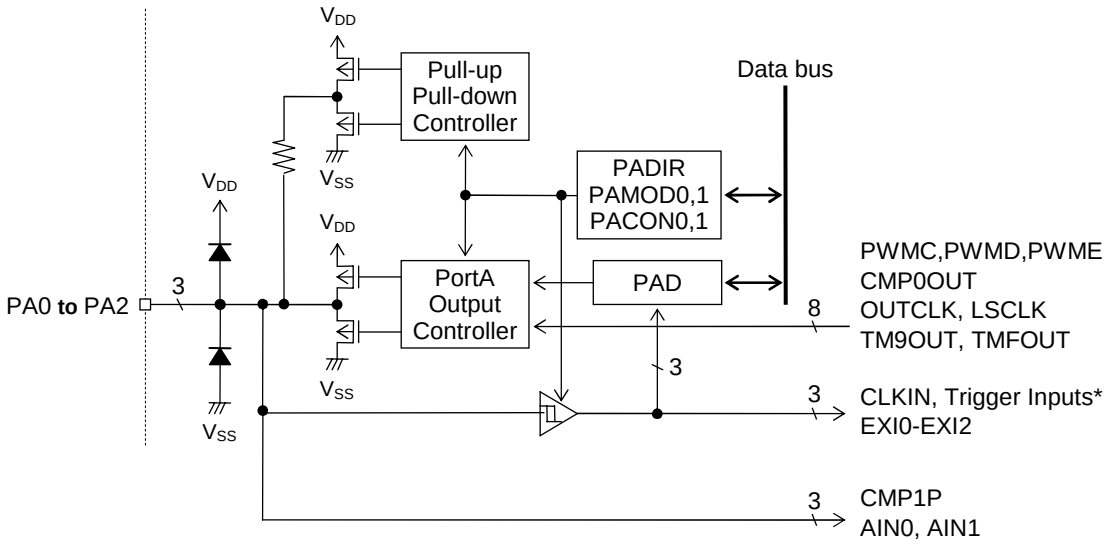
This LSI includes Port A (PA0 to PA2) which is an 3-bit input/output port.
Port A can have external interrupt, input of comparator and input of Successive Approximation Type A/D Converter. And, port A can have PWM, Timers, output of comparator, input of external clock, output of clock functions as secondary, tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM", for the comparator, see Chapter 22, "Analog Comparator ", for the Successive Approximation Type A/D Converter, see Chapter 20, "Successive Approximation Type A/D Converter", for the external clock and output of clock, see Chapter 6, "Clock Generation Circuit", for the Timers, see Chapter 8, "Timers".

15.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The external interrupt pins (EXI0 to EXI2), comparator input pin (CMP1P), and analog input pin of Successive Approximation Type A/D Converter (AIN0, AIN1) can be used. The PWM pins (PWMC, PWMD, PWME), comparator output pin (CMP0OUT), Timers output pins (TM9OUT, TMFOUT), external clock pin (CLKIN), clock output pin (OUTCLK, LSCLK) can be used as secondary, tertiary and fourthly functions.

15.1.2 Configuration

Figure 15-1 shows the configuration of Port A.



* : Trigger Inputs : TETG, TFTG, PCTG, PDTG, PETG, PFTG

PAD	: Port A data register
PADIR	: Port A direction register
PACON0	: Port A control register 0
PACON1	: Port A control register 1
PAMOD0	: Port A mode register 0
PAMOD1	: Port A mode register 1

Figure 15-1 Configuration of Port A

15.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
PA0/ EXI0/ AIN0/ TnTG/ PmTG	I/O	Input/output port, External 0 interrupt, SA-ADC 0 input, Timer n trigger input, PWM m trigger input	PWMC output	High-speed clock output (OUTCLK)	Timer 9 out (TM9OUT)
PA1/ EXI1/ AIN1/ CMP1P/ TnTG/ PmTG	I/O	Input/output port, External 1 interrupt, SA-ADC 1 input, Analog comparator 1 inverted input, Timer n trigger input, PWM m trigger input	PWMD output	Low-speed clock output (LSCLK)	Timer F out (TMFOUT)
PA2/ EXI2/ TnTG/ PmTG	I/O	Input/output port, External 2 interrupt, Timer n trigger input, PWM m trigger input	PWME output	External clock input (CLKIN)	Comparator 0 output (CMP0OUT)

(n: E, F) (m: C, D, E, F)

Note:
PA0 – PA1 are assigned to the input of SA-ADC. When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.
PA1 is assigned to the input of Analog Comparator. When used as an analog input of Analog Comparator, set an applicable port as a high impedance output state.

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H
0F254H	Port A mode register 0	PAMOD0	PAMOD	R/W	8/16	00H
0F255H	Port A mode register 1	PAMOD1		R/W	8	00H

15.2.2 Port A Data Register (PAD)

Address: 0F250H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAD	—	—	—	—	—	PA2D	PA1D	PA0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PAD is a special function register (SFR) to set the value to be output to the Port A pin or to read the input level of the Port A. In output mode, the value of this register is output to the Port A pin. The value written to PAD is readable. In input mode, the input level of the Port A pin is read when PAD is read. Output mode or input mode is selected by using the port direction register (PADIR) described later.

[Description of Bits]

- **PA2D-PA0D** (bits 2 to 0)

  The PA2D to PA0D bits are used to set the output value of the Port A pin in output mode and to read the pin level of the Port A pin in input mode.

PA0D	Description
0	Output or input level of the PA0 pin: "L"
1	Output or input level of the PA0 pin: "H"

PA1D	Description
0	Output or input level of the PA1 pin: "L"
1	Output or input level of the PA1 pin: "H"

PA2D	Description
0	Output or input level of the PA2 pin: "L"
1	Output or input level of the PA2 pin: "H"

15.2.3 Port A Direction Register (PADIR)

Address: 0F251H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PADIR	—	—	—	—	—	PA2DIR	PA1DIR	PA0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PADIR is a special function register (SFR) to select the input/output mode of Port A.

[Description of Bits]

- **PA2DIR-PA0DIR** (bits 2 to 0)

  The PA2DIR to PA0DIR pins are used to set the input/output direction of the Port A pin.

PA0DIR	Description
0	PA0 pin: Output (initial value)
1	PA0 pin: Input

PA1DIR	Description
0	PA1 pin: Output (initial value)
1	PA1 pin: Input

PA2DIR	Description
0	PA2 pin: Output (initial value)
1	PA2 pin: Input

15.2.4 Port A Control Registers 0, 1 (PACON0, PACON1)

Address: 0F252H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON0	—	—	—	—	—	PA2C0	PA1C0	PA0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F253H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON1	—	—	—	—	—	PA2C1	PA1C1	PA0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PACON0 and PACON1 are special function registers (SFRs) to select input/output state of the Port A pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PADIR register.

[Description of Bits]

- **PA2C1-PA0C1, PA2C0-PA0C0** (bits 2 to 0)

  The PA2C1 to PA0C1 pins and the PA2C0 to PA0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PA0 pin		When output mode is selected (PA0DIR bit = "0")	When input mode is selected (PA0DIR bit = "1")
PA0C1	PA0C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA1 pin		When output mode is selected (PA1DIR bit = "0")	When input mode is selected (PA1DIR bit = "1")
PA1C1	PA1C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA2 pin		When output mode is selected (PA2DIR bit = "0")	When input mode is selected (PA2DIR bit = "1")
PA2C1	PA2C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

15.2.5 Port A Mode Registers 0 (PAMOD0, PAMOD1))

Address: 0F254H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAMOD0	—	—	—	—	—	PA2MD0	PA1MD0	PA0MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F255H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAMOD1	—	—	—	—	—	PA2MD1	PA1MD1	PA0MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PAMOD0 and PAMOD1 are special function registers (SFRs) to select the primary, secondary, tertiary and fourthly function of Port A.

[Description of Bits]

- **PA0MD1, PA0MD0** (bit 0)

The PA0MD1 and PA0MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PA0 pin.

PA0MD1	PA0MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMC output
1	0	High-speed clock (OUTCLK) output
1	1	Timer 9 (TM9OUT) out

- **PA1MD1, PA1MD0** (bit 1)

The PA1MD1 and PA1MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PA1 pin.

PA1MD1	PA1MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMD output
1	0	Low-speed clock (LSCLK) output
1	1	Timer F (TMFOUT) out

- **PA2MD1, PA2MD0** (bit 2)

The PA2MD1 and PA2MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PA2 pin.

PA2MD1	PA2MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWME output
1	0	External clock (CLKIN) input
1	1	Comparator 0 (CMP0OUT) output

15.3 Description of Operation

15.3.1 Input/Output Port Functions

For each pin of Port A, either output or input is selected by setting the Port A direction register (PADIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port A depending on the value set by the Port A data register (PAD).
In input mode, the input level of each pin of Port A can be read from the Port A data register (PAD).

15.3.2 Primary Function except for Input/Output Port

Port A is assigned to the SA A/D converter input pins(AIN0, AIN1), Analog comparator input(CMP1P), External interrupts(EXI0-2), Trigger inputs(TETG, TFTG, PCTG, PDTG, PETG, PFTG) as primary function except for input/output port.
When used as the SA A/D converter input pins (AIN0, AIN1) and Analog comparator input pin(CMP1P), set an applicable port as a high impedance output state.
When used as the External interrupts/Trigger inputs(EXI0-2, TETG, TFTG, PCTG, PDTG, PETG, PFTG), set an applicable port as a input state.

15.3.3 Secondary tertiary and fourthly functions

Port A is assigned to the PWM pins (PWMC, PWMD, PWME), comparator output pins (CMP0OUT), Timers output pin (TM9OUT, TMFOUT), external clock pin (CLKIN), clock output pin (OUTCLK, LSCLK) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the PA2MD0 to PA0MD0 bits and the PA2MD1 to PA0MD1 bits of the Port A mode registers (PAMOD0, PAMOD1).

Chapter 16

Port B

16 Port B

16.1 Overview

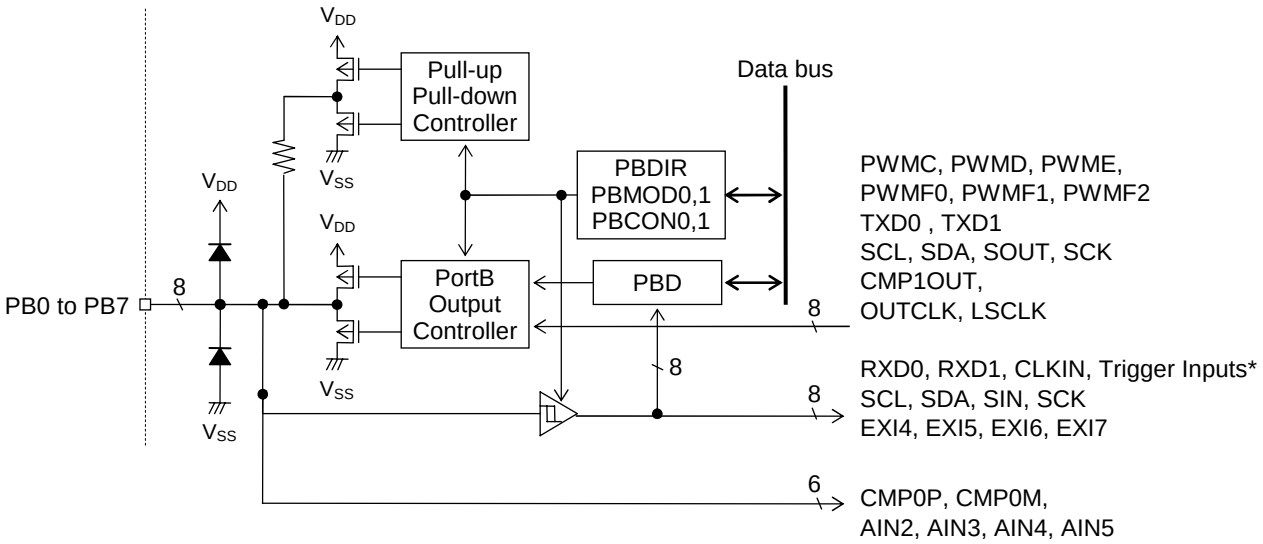
This LSI includes Port B (PB0 to PB7) which is an 8-bit input/output port.
Port B can have external interrupt, input of comparator and input of Successive Approximation Type A/D Converter.
And, port B can have PWM, output of comparator, Synchronous Serial Port (SSIO), UART, I2C Bus Interface, input of external clock, output of clock functions as secondary, tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM", for the comparator, see Chapter 22, "Analog Comparator "; for the Successive Approximation Type A/D Converter, see Chapter 20, "Successive Approximation Type A/D Converter" , for the Synchronous Serial Port (SSIO), see Chapter 11, "Synchronous Serial Port", for the UART, see Chapter 12, "UART", for the I2C Bus Interface, see Chapter 13, "I2C Bus Interface (Master)" and Chapter 14, "I2C Bus Interface (Slave)", for the external clock and output of clock, see Chapter 6, "Clock Generation Circuit".

16.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The external interrupt pins (EXI4, EXI5, EXI6, EXI7), comparator input pins (CMP0P, CMP0M), analog input pins of Successive Approximation Type A/D Converter (AIN2 to 5), and UART input pins (RXD0, RXD1) can be used.
  The PWM pins (PWMC, PWMD, PWME, PWMF0, PWMF1, PWMF2), comparator output pins (CMP1OUT), SSIO pins (SIN, SOUT, SCK), UART output pins (TXD0, TXD1), I2C pins (SCL, SDA), external clock pin (CLKIN), clock output pin (OUTCLK, LSCLK) can be used as the secondary, tertiary and fourthly functions.

16.1.2 Configuration

Figure 16-1 shows the configuration of Port B.



* :Trigger Inputs : TETG, TFTG, PCTG, PDTG, PETG, PFTG

PBD	: Port B data register
PBDIR	: Port B direction register
PBCON0	: Port B control register 0
PBCON1	: Port B control register 1
PBMOD0	: Port B mode register 0
PBMOD1	: Port B mode register 1

Figure 16-1 Configuration of Port B

16.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
PB0/ EXI4/ AIN2/ RXD0/ TnTG/ PmTG	I/O	Input/output port, External 4 interrupt, SA-ADC 2 input, UART0 data input, Timer n trigger input, PWM m trigger input	PWMC output	High-speed clock output (OUTCLK)	Comparator 1 output (CMP1OUT)
PB1/ EXI5/ AIN3/ TnTG/ PmTG	I/O	Input/output port, External 5 interrupt, SA-ADC 3 input, Timer n trigger input, PWM m trigger input	PWMD output	UART0 data output	UART1 data output
PB2/ EXI6/ RXD1/ TnTG/ PmTG	I/O	Input/output port, External 6 interrupt, UART1 data input, Timer n trigger input, PWM m trigger input	PWME output	—	—
PB3/ EXI7/ TnTG/ PmTG	I/O	Input/output port, External 7 interrupt, Timer n trigger input, PWM m trigger input	SSIO data input	UART1 data output	—
PB4/ CMP0P/ TnTG/ PmTG	I/O	Input/output port, Analog comparator 0 non-inverted input, Timer n trigger inpu,t PWM m trigger input	SSIO data output	UART0 data output	UART1 data output
PB5/ RXD0/ CMP0M/ TnTG/ PmTG	I/O	Input/output port, UART0 data input, Analog comparator 0 inverted input pin, Timer n trigger input, PWM m trigger input	SSIO clock input/output	I^2C clock input/output	PWMF2 output
PB6/ AIN4/ TnTG/ PmTG	I/O	Input/output port, SA-ADC 4 input, Timer n trigger input, PWM m trigger input	External clock input (CLKIN)	I^2C data input/output	PWMF1 output
PB7/ RXD1/ AIN5/ TnTG/ PmTG	I/O	Input/output port, UART1 data input, SA-ADC 5 input, Timer n trigger input, PWM m trigger input	Low-speed clock output (LSCLK)	PWMF0 output	PWMC output (PWMC)

(n: E, F) (m: C, D, E, F)

Note:
PB0, PB1, PB6, PB7 are assigned to the input of SA-ADC. When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.
PB4, PB5 are assigned to the input of Analog Comparator. When used as an analog input of Analog Comparator, set an applicable port as a high impedance output state.

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F258H	Port B data register	PBD	—	R/W	8	00H
0F259H	Port B direction register	PBDIR	—	R/W	8	00H
0F25AH	Port B control register 0	PBCON0	PBCON	R/W	8/16	00H
0F25BH	Port B control register 1	PBCON1		R/W	8	00H
0F25CH	Port B mode register 0	PBMOD0	PBMOD	R/W	8/16	00H
0F25DH	Port B mode register 1	PBMOD1		R/W	8	00H

16.2.2 Port B Data Register (PBD)

Address: 0F258H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBD	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBD is a special function register (SFR) to set the value to be output to the Port B pin or to read the input level of the Port B. In output mode, the value of this register is output to the Port B pin. The value written to PBD is readable. In input mode, the input level of the Port B pin is read when PBD is read. Output mode or input mode is selected by using the port direction register (PBDIR) described later.

[Description of Bits]

- **PB7D-PB0D** (bits 7 to 0)

  The PB7D to PB0D bits are used to set the output value of the Port B pin in output mode and to read the pin level of the Port B pin in input mode.

PB0D	Description
0	Output or input level of the PB0 pin: "L"
1	Output or input level of the PB0 pin: "H"

PB1D	Description
0	Output or input level of the PB1 pin: "L"
1	Output or input level of the PB1 pin: "H"

PB2D	Description
0	Output or input level of the PB2 pin: "L"
1	Output or input level of the PB2 pin: "H"

PB3D	Description
0	Output or input level of the PB3 pin: "L"
1	Output or input level of the PB3 pin: "H"

PB4D	Description
0	Output or input level of the PB4 pin: "L"
1	Output or input level of the PB4 pin: "H"

PB5D	Description
0	Output or input level of the PB5 pin: "L"
1	Output or input level of the PB5 pin: "H"

PB6D	Description
0	Output or input level of the PB6 pin: "L"
1	Output or input level of the PB6 pin: "H"

PB7D	Description
0	Output or input level of the PB7 pin: "L"
1	Output or input level of the PB7 pin: "H"

16.2.3 Port B Direction Register (PBDIR)

Address: 0F259H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBDIR	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBDIR is a special function register (SFR) to select the input/output mode of Port B.

[Description of Bits]

- **PB7DIR-PB0DIR** (bits 7 to 0)

The PB7DIR to PB0DIR pins are used to set the input/output direction of the Port B pin.

PB0DIR	Description
0	PB0 pin: Output (initial value)
1	PB0 pin: Input

PB1DIR	Description
0	PB1 pin: Output (initial value)
1	PB1 pin: Input

PB2DIR	Description
0	PB2 pin: Output (initial value)
1	PB2 pin: Input

PB3DIR	Description
0	PB3 pin: Output (initial value)
1	PB3 pin: Input

PB4DIR	Description
0	PB4 pin: Output (initial value)
1	PB4 pin: Input

PB5DIR	Description
0	PB5 pin: Output (initial value)
1	PB5 pin: Input

PB6DIR	Description
0	PB6 pin: Output (initial value)
1	PB6 pin: Input

PB7DIR	Description
0	PB7 pin: Output (initial value)
1	PB7 pin: Input

16.2.4 Port B Control Registers 0, 1 (PBCON0, PBCON1)

Address: 0F25AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBCON0	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F25BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBCON1	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBCON0 and PBCON1 are special function registers (SFRs) to select input/output state of the Port B pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PBDIR register.

[Description of Bits]

- **PB7C1-PB0C1, PB7C0-PB0C0** (bits 7 to 0)

  The PB7C1 to PB0C1 pins and the PB7C0 to PB0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PB0 pin		When output mode is selected (PB0DIR bit = "0")	When input mode is selected (PB0DIR bit = "1")
PB0C1	PB0C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB1 pin		When output mode is selected (PB1DIR bit = "0")	When input mode is selected (PB1DIR bit = "1")
PB1C1	PB1C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB2 pin		When output mode is selected (PB2DIR bit = "0")	When input mode is selected (PB2DIR bit = "1")
PB2C1	PB2C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB3 pin		When output mode is selected (PB3DIR bit = "0")	When input mode is selected (PB3DIR bit = "1")
PB3C1	PB3C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB4 pin		When output mode is selected (PB4DIR bit = "0")	When input mode is selected (PB4DIR bit = "1")
PB4C1	PB4C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB5 pin		When output mode is selected (PB5DIR bit = "0")	When input mode is selected (PB5DIR bit = "1")
PB5C1	PB5C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB6 pin		When output mode is selected (PB6DIR bit = "0")	When input mode is selected (PB6DIR bit = "1")
PB6C1	PB6C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB7 pin		When output mode is selected (PB7DIR bit = "0")	When input mode is selected (PB7DIR bit = "1")
PB7C1	PB7C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

16.2.5 Port B Mode Registers 0 (PBMOD0, PBMOD1)

Address: 0F25CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBMOD0	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F25DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBMOD1	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBMOD0 and PBMOD1 are special function registers (SFRs) to select the primary, secondary, tertiary and fourthly function of Port B.

[Description of Bits]

- **PB0MD1, PB0MD0** (bit 0)

The PB0MD1 and PB0MD0 bits are used to select the primary, secondary, tertiary and fourthly function of the PB0 pin.

PB0MD1	PB0MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMC output
1	0	High-speed clock (OUTCLK) output
1	1	Comparator 1 (CMP1OUT) output

- **PB1MD1, PB1MD0** (bit 1)

The PB1MD1 and PB1MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB1 pin.

PB1MD1	PB1MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMD output
1	0	UART0 data output pin
1	1	UART1 data output pin

- **PB2MD1, PB2MD0** (bit 2)

The PB2MD1 and PB2MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB2 pin.

PB2MD1	PB2MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWME output
1	0	Prohibited
1	1	Prohibited

- **PB3MD1, PB3MD0** (bit 3)
  The PB3MD1 and PB3MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB3 pin.

PB3MD1	PB3MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	SSIO data input
1	0	UART1 data output pin
1	1	Prohibited

- **PB4MD1, PB4MD0** (bit 4)
  The PB4MD1 and PB4MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB4 pin.

PB4MD1	PB4MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	SSIO data output
1	0	UART0 data output pin
1	1	UART1 data output pin

- **PB5MD1, PB5MD0** (bit 5)
  The PB5MD1 and PB5MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB5 pin.

PB5MD1	PB5MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	SSIO clock input/output
1	0	I^2C clock input/output
1	1	PWMF2 output

- **PB6MD0, PB6MD0** (bit 6)
  The PB6MD1 and PB6MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PB6 pin.

PB6MD1	PB6MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	External clock (CLKIN) input
1	0	I^2C data input/output
1	1	PWMF1 output

- **PB7MD1, PB7MD0** (bit 7)
  The PB7MD1 and PB7MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB7 pin.

PB7MD1	PB7MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Low-speed clock (LSCLK) output
1	0	PWMF0 output
1	1	PWMC output

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the Port B is specified to output mode (selected in Port B control register), status of corresponding pin is fixed, regardless the contents of Port B register (PBD)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

16.3 Description of Operation

16.3.1 Input/Output Port Functions

For each pin of Port B, either output or input is selected by setting the Port B direction register (PBDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port B control registers 0 and 1 (PBCON0 and PBCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port B control registers 0 and 1 (PBCON0 and PBCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port B depending on the value set by the Port B data register (PBD).
In input mode, the input level of each pin of Port B can be read from the Port B data register (PBD).

16.3.2 Primary Function except for Input/Output Port

Port B is assigned to the SA A/D converter input pins(AIN2-5), Analog comparator input(CMP0M, CMP0P), External interrupts(EXI4-7), Trigger inputs(TETG, TFTG, PCTG, PDTG, PETG, PFTG), UART input pins (RXD0, RXD1) as primary function except for input/output port.
When used as the SA A/D converter input pins (AIN2-5) and Analog comparator input(CMP0M, CMP0P), set an applicable port as a high impedance output state.
When used as the External interrupts/Trigger inputs /UART input pins (EXI4-7, TETG, TFTG, PCTG, PDTG, PETG, PFTG, RXD0, RXD1), set an applicable port as a input state.

16.3.3 Secondary tertiary and fourthly functions

Port B is assigned to PWM output pins (PWMC, PWMD, PWME, PWMF0, PWMF1, PWMF2), comparator output pin (CMP1OUT), SSIO pins (SIN, SOUT, SCK), UART output pins (TXD0, TXD1), I^2C pins (SCL, SDA), external clock pin (CLKIN), clock output pins (OUTCLK, LSCLK) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the PB7MD0 to PB0MD0 bits and the PB7MD1 to PB0MD1 bits of the Port B mode registers (PBMOD0, PBMOD1).

Chapter 17

Port C

17 Port C

17.1 Overview

This LSI includes Port C (ML610Q111: PC0 to PC3, ML610Q112: PC0 to PC7) which is an 8-bit input/output port.
Port C can have input of Successive Approximation Type A/D Converter.
And, Port C can have PWM, I^2C Bus Interface, Timers as secondary, tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM", for the Successive Approximation Type A/D Converter, see Chapter 20, "Successive Approximation Type A/D Converter" , for the I^2C Bus Interface, see Chapter 13, "I^2C Bus Interface Master" and Chapter 14, "I^2C Bus Interface Slave", for the Timers see Chapter 8, "Timers".

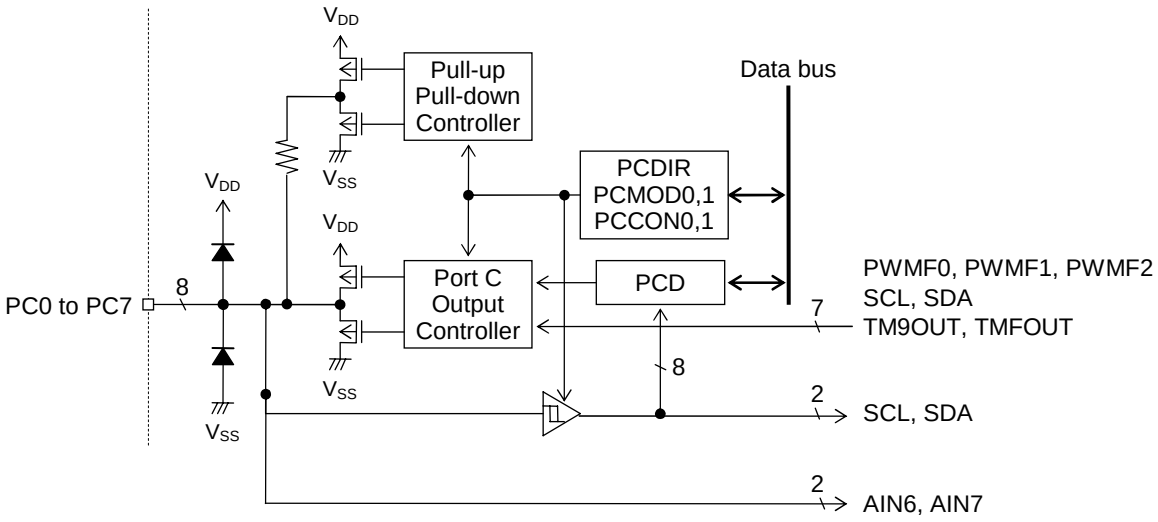
17.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The analog input pins of Successive Approximation Type A/D Converter (AIN6, AIN7) can be used.
  The PWM pins (PWMF0, PWMF1, PWMF2), I^2C pins (SCL, SDA), Timers output pins (TM9OUT, TMFOUT) can be used as the secondary, tertiary and fourthly functions.

Note:
When used as ML610Q111, the PC4 to PC7 ports do not exist, and the PC4 to PC7 special function registers (SFRs) do not perform.

17.1.2 Configuration

Figure 17-1 shows the configuration of Port C.



PCD	: Port C data register
PCDIR	: Port C direction register
PCCON0	: Port C control register 0
PCCON1	: Port C control register 1
PCMOD0	: Port C mode register 0
PCMOD1	: Port C mode register 1

Figure 17-1 Configuration of Port C

17.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
PC0/	I/O	Input/output port	—	PWMF0 output	Timer 9 ouput
PC1/	I/O	Input/output port	—	PWMF1 output	—
PC2/	I/O	Input/output port	—	PWMF2 output	—
PC3/	I/O	Input/output port	—	—	Timer F ouput
PC4/	I/O	Input/output port	I^2C clock input/output	—	—
PC5/	I/O	Input/output port	I^2C data input/output	—	—
PC6/ AIN6	I/O	Input/output port, SA-ADC 6 input	—	—	—
PC7/ AIN7	I/O	Input/output port, SA-ADC 7 input	—	—	—

Note:
PC6, PC7 are assigned to the input of SA-ADC. When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F260H	Port C data register	PCD	—	R/W	8	00H
0F261H	Port C direction register	PCDIR	—	R/W	8	00H
0F262H	Port C control register 0	PCCON0	PCCON	R/W	8/16	00H
0F263H	Port C control register 1	PCCON1		R/W	8	00H
0F264H	Port C mode register 0	PCMOD0	PCMOD	R/W	8/16	00H
0F265H	Port C mode register 1	PCMOD1		R/W	8	00H

17.2.2 Port C Data Register (PCD)

Address: 0F260H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCD	PC7D	PC6D	PC5D	PC4D	PC3D	PC2D	PC1D	PC0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCD is a special function register (SFR) to set the value to be output to the Port C pin or to read the input level of the Port C. In output mode, the value of this register is output to the Port C pin. The value written to PCD is readable. In input mode, the input level of the Port C pin is read when PCD is read. Output mode or input mode is selected by using the port direction register (PCDIR) described later.

[Description of Bits]

- **PC7D-PC0D** (bits 7 to 0)

The PC7D to PC0D bits are used to set the output value of the Port C pin in output mode and to read the pin level of the Port C pin in input mode.
When used as ML610Q111, setting the value of PC7D to PC4D do not affect an applicable ports.

PC0D	Description
0	Output or input level of the PC0 pin: "L"
1	Output or input level of the PC0 pin: "H"

PC1D	Description
0	Output or input level of the PC1 pin: "L"
1	Output or input level of the PC1 pin: "H"

PC2D	Description
0	Output or input level of the PC2 pin: "L"
1	Output or input level of the PC2 pin: "H"

PC3D	Description
0	Output or input level of the PC3 pin: "L"
1	Output or input level of the PC3 pin: "H"

PC4D	Description
0	Output or input level of the PC4 pin: "L"
1	Output or input level of the PC4 pin: "H"

PC5D	Description
0	Output or input level of the PC5 pin: "L"
1	Output or input level of the PC5 pin: "H"

PC6D	Description
0	Output or input level of the PC6 pin: "L"
1	Output or input level of the PC6 pin: "H"

PC7D	Description
0	Output or input level of the PC7 pin: "L"
1	Output or input level of the PC7 pin: "H"

17.2.3 Port C Direction Register (PCDIR)

Address: 0F261H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCDIR	PC7DIR	PC6DIR	PC5DIR	PC4DIR	PC3DIR	PC2DIR	PC1DIR	PC0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCDIR is a special function register (SFR) to select the input/output mode of Port C.

[Description of Bits]

- **PC7DIR-PC0DIR** (bits 7 to 0)

The PC7DIR to PC0DIR pins are used to set the input/output direction of the Port C pin.
When used as ML610Q111, setting the value of PC7DIR to PC4DIR do not affect an applicable ports.

PC0DIR	Description
0	PC0 pin: Output (initial value)
1	PC0 pin: Input

PC1DIR	Description
0	PC1 pin: Output (initial value)
1	PC1 pin: Input

PC2DIR	Description
0	PC2 pin: Output (initial value)
1	PC2 pin: Input

PC3DIR	Description
0	PC3 pin: Output (initial value)
1	PC3 pin: Input

PC4DIR	Description
0	PC4 pin: Output (initial value)
1	PC4 pin: Input

PC5DIR	Description
0	PC5 pin: Output (initial value)
1	PC5 pin: Input

PC6DIR	Description
0	PC6 pin: Output (initial value)
1	PC6 pin: Input

PC7DIR	Description
0	PC7 pin: Output (initial value)
1	PC7 pin: Input

17.2.4 Port C Control Registers 0, 1 (PCCON0, PCCON1)

Address: 0F262H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCCON0	PC7C0	PC6C0	PC5C0	PC4C0	PC3C0	PC2C0	PC1C0	PC0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F263H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCCON1	PC7C1	PC6C1	PC5C1	PC4C1	PC3C1	PC2C1	PC1C1	PC0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCCON0 and PCCON1 are special function registers (SFRs) to select input/output state of the Port C pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PCDIR register.

[Description of Bits]

- **PC7C1-PC0C1, PC7C0-PC0C0** (bits 7 to 0)

The PC7C1 to PC0C1 pins and the PC7C0 to PC0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
When used as ML610Q111, setting the value of PC7C1 to PC4C1, PC7C0 to PC4C0 do not affect an applicable ports.

Setting of PC0 pin		When output mode is selected (PC0DIR bit = "0")	When input mode is selected (PC0DIR bit = "1")
PC0C1	PC0C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC1 pin		When output mode is selected (PC1DIR bit = "0")	When input mode is selected (PC1DIR bit = "1")
PC1C1	PC1C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC2 pin		When output mode is selected (PC2DIR bit = "0")	When input mode is selected (PC2DIR bit = "1")
PC2C1	PC2C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC3 pin		When output mode is selected (PC3DIR bit = "0")	When input mode is selected (PC3DIR bit = "1")
PC3C1	PC3C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC4 pin		When output mode is selected (PC4DIR bit = "0")	When input mode is selected (PC4DIR bit = "1")
PC4C1	PC4C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC5 pin		When output mode is selected (PC5DIR bit = "0")	When input mode is selected (PC5DIR bit = "1")
PC5C1	PC5C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC6 pin		When output mode is selected (PC6DIR bit = "0")	When input mode is selected (PC6DIR bit = "1")
PC6C1	PC6C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PC7 pin		When output mode is selected (PC7DIR bit = "0")	When input mode is selected (PC7DIR bit = "1")
PC7C1	PC7C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

17.2.5 Port C Mode Registers 0 (PCMOD0, PCMOD1)

Address: 0F264H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCMOD0	PC7MD0	PC6MD0	PC5MD0	PC4MD0	PC3MD0	PC2MD0	PC1MD0	PC0MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F265H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PCMOD1	PC7MD1	PC6MD1	PC5MD1	PC4MD1	PC3MD1	PC2MD1	PC1MD1	PC0MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PCMOD0 and PCMOD1 are special function register (SFR) to select the primary, secondary, tertiary and fourthly function of Port C.
When used as ML610Q111, setting the value of PC7MD1 to PC4MD1, PC7MD0 to PC4MD0 do not affect an applicable ports.

[Description of Bits]

- **PC0MD1, PC0MD0** (bit 0)
  The PC0MD1 and PC0MD0 bits are used to select the primary, secondary, tertiary and fourthly function of the PC0 pin.

PC0MD1	PC0MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	PWMF0 output
1	1	Timer 9 (TM9OUT) out

- **PC1MD1, PC1MD0** (bit 1)
  The PC1MD1 and PC1MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC1 pin.

PC1MD1	PC1MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	PWMF1 output
1	1	Prohibited

- **PC2MD1, PC2MD0** (bit 2)
  The PC2MD1 and PC2MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC2 pin.

PC2MD1	PC2MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	PWMF2 output
1	1	Prohibited

- **PC3MD1, PC3MD0** (bit 3)
  The PC3MD1 and PC3MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC3 pin.

PC3MD1	PC3MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Timer F (TMFOUT) out

- **PC4MD1, PC4MD0** (bit 4)
  The PC4MD1 and PC4MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC4 pin.

PC4MD1	PC4MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C clock input/output
1	0	Prohibited
1	1	Prohibited

- **PC5MD1, PC5MD0** (bit 5)
  The PC5MD1 and PC5MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC5 pin.

PC5MD1	PC5MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I^2C data input/output
1	0	Prohibited
1	1	Prohibited

- **PC6MD0, PC6MD0** (bit 6)
  The PC6MD1 and PC6MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PC6 pin.

PC6MD1	PC6MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

- **PC7MD1, PC7MD0** (bit 7)
  The PC7MD1 and PC7MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PC7 pin.

PC7MD1	PC7MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the Port C is specified to output mode (selected in Port C control register), status of corresponding pin is fixed, regardless the contents of Port C register (PCD)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

17.3 Description of Operation

17.3.1 Input/Output Port Functions

For each pin of Port C, either output or input is selected by setting the Port C direction register (PCDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port C control registers 0 and 1 (PCCON0 and PCCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port C control registers 0 and 1 (PCCON0 and PCCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port C depending on the value set by the Port C data register (PCD).
In input mode, the input level of each pin of Port C can be read from the Port C data register (PCD).

Note:
When used as ML610Q111, the PC4 to PC7 ports do not exist, and the PC4 to PC7 special function registers (SFRs) do not perform.

17.3.2 Primary Function except for Input/Output Port

Port C is assigned to the SA A/D converter input pins(AIN6, AIN7) as primary function except for input/output port.
When used as the SA A/D converter input pins (AIN6, AIN7), set an applicable port as a high impedance output state.

Note:
This function is available only ML610Q112.

17.3.3 Secondary tertiary and fourthly functions

Port C is assigned to PWM pins (PWMF0, PWMF1, PWMF2), I^2C pins (SCL, SDA), Timers output pins (TM9OUT, TMFOUT) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the PC7MD0 to PC0MD0 bits and the PC7MD1 to PC0MD1 bits of the Port C mode registers (PCMOD0, PCMOD1).

Note:
I2C pins(SCL, SDA) are available only ML610Q112.

Chapter 18

Port D

18 Port D

18.1 Overview

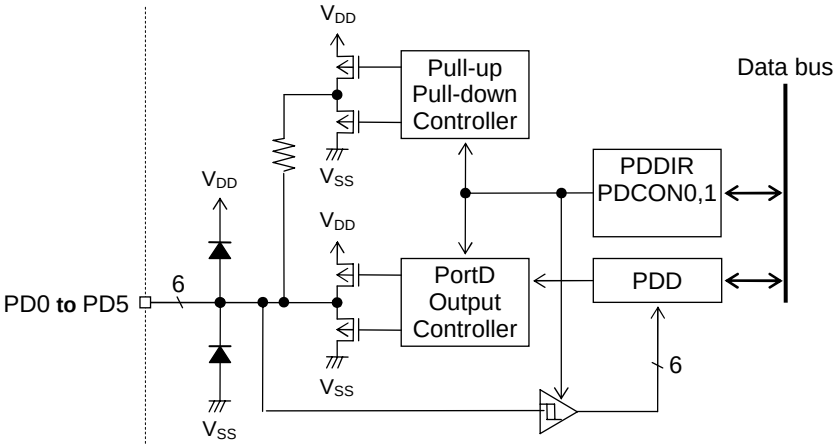
This LSI includes Port D (PD0 to PD5) which is an 6-bit input/output port.(only for ML610Q112)

18.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.

18.1.2 Configuration

Figure 18-1 shows the configuration of Port D.



PDD : Port D data register
PDDIR : Port D direction register
PDCON0 : Port D control register 0
PDCON1 : Port D control register 1

Figure 18-1 Configuration of Port D

18.1.3 List of Pins

Pin name	I/O	Primary function
PD0	I/O	Input/output port
PD1	I/O	Input/output port
PD2	I/O	Input/output port
PD3	I/O	Input/output port
PD4	I/O	Input/output port
PD5	I/O	Input/output port

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F268H	Port D data register	PDD	—	R/W	8	00H
0F269H	Port D direction register	PDDIR	—	R/W	8	00H
0F26AH	Port D control register 0	PDCON0	PDCON	R/W	8/16	00H
0F26BH	Port D control register 1	PDCON1		R/W	8	00H

18.2.2 Port D Data Register (PDD)

Address: 0F268H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDD	—	—	PD5D	PD4D	PD3D	PD2D	PD1D	PD0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDD is a special function register (SFR) to set the value to be output to the Port D pin or to read the input level of the Port D. In output mode, the value of this register is output to the Port D pin. The value written to PDD is readable. In input mode, the input level of the Port D pin is read when PDD is read. Output mode or input mode is selected by using the port direction register (PDDIR) described later.

[Description of Bits]

- **PD5D-PD0D** (bits 5 to 0)

  The PD5D to PD0D bits are used to set the output value of the Port D pin in output mode and to read the pin level of the Port D pin in input mode.

PD0D	Description
0	Output or input level of the PD0 pin: "L"
1	Output or input level of the PD0 pin: "H"

PD1D	Description
0	Output or input level of the PD1 pin: "L"
1	Output or input level of the PD1 pin: "H"

PD2D	Description
0	Output or input level of the PD2 pin: "L"
1	Output or input level of the PD2 pin: "H"

PD3D	Description
0	Output or input level of the PD3 pin: "L"
1	Output or input level of the PD3 pin: "H"

PD4D	Description
0	Output or input level of the PD4 pin: "L"
1	Output or input level of the PD4 pin: "H"

PD5D	Description
0	Output or input level of the PD5 pin: "L"
1	Output or input level of the PD5 pin: "H"

18.2.3 Port D Direction Register (PDDIR)

Address: 0F269H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDDIR	—	—	PD5DIR	PD4DIR	PD3DIR	PD2DIR	PD1DIR	PD0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDDIR is a special function register (SFR) to select the input/output mode of Port D.

[Description of Bits]

- **PD5DIR-PD0DIR** (bits 5 to 0)

The PD5DIR to PD0DIR pins are used to set the input/output direction of the Port D pin.

PD0DIR	Description
0	PD0 pin: Output (initial value)
1	PD0 pin: Input

PD1DIR	Description
0	PD1 pin: Output (initial value)
1	PD1 pin: Input

PD2DIR	Description
0	PD2 pin: Output (initial value)
1	PD2 pin: Input

PD3DIR	Description
0	PD3 pin: Output (initial value)
1	PD3 pin: Input

PD4DIR	Description
0	PD4 pin: Output (initial value)
1	PD4 pin: Input

PD5DIR	Description
0	PD5 pin: Output (initial value)
1	PD5 pin: Input

18.2.4 Port D Control Registers 0, 1 (PDCON0, PDCON1)

Address: 0F26AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDCON0	—	—	PD5C0	PD4C0	PD3C0	PD2C0	PD1C0	PD0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F26BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PDCON1	—	—	PD5C1	PD4C1	PD3C1	PD2C1	PD1C1	PD0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PDCON0 and PDCON1 are special function registers (SFRs) to select input/output state of the Port D pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PDDIR register.

[Description of Bits]

- **PD5C1-PD0C1, PD5C0-PD0C0** (bits 5 to 0)

  The PD5C1 to PD0C1 pins and the PD5C0 to PD0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PD0 pin		When output mode is selected (PD0DIR bit = "0")	When input mode is selected (PD0DIR bit = "1")
PD0C1	PD0C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PD1 pin		When output mode is selected (PD1DIR bit = "0")	When input mode is selected (PD1DIR bit = "1")
PD1C1	PD1C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PD2 pin		When output mode is selected (PD2DIR bit = "0")	When input mode is selected (PD2DIR bit = "1")
PD2C1	PD2C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PD3 pin		When output mode is selected (PD3DIR bit = "0")	When input mode is selected (PD3DIR bit = "1")
PD3C1	PD3C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PD4 pin		When output mode is selected (PD4DIR bit = "0")	When input mode is selected (PD4DIR bit = "1")
PD4C1	PD4C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PD5 pin		When output mode is selected (PD5DIR bit = "0")	When input mode is selected (PD5DIR bit = "1")
PD5C1	PD5C0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

18.3 Description of Operation

18.3.1 Input/Output Port Functions

For each pin of Port D, either output or input is selected by setting the Port D direction register (PDDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port D control registers 0 and 1 (PDCON0 and PDCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port D control registers 0 and 1 (PDCON0 and PDCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port D depending on the value set by the Port D data register (PDD).
In input mode, the input level of each pin of Port D can be read from the Port D data register (PDD).

Chapter 19

Port AB Interrupts

19 Port AB Interrupts

19.1 Overview

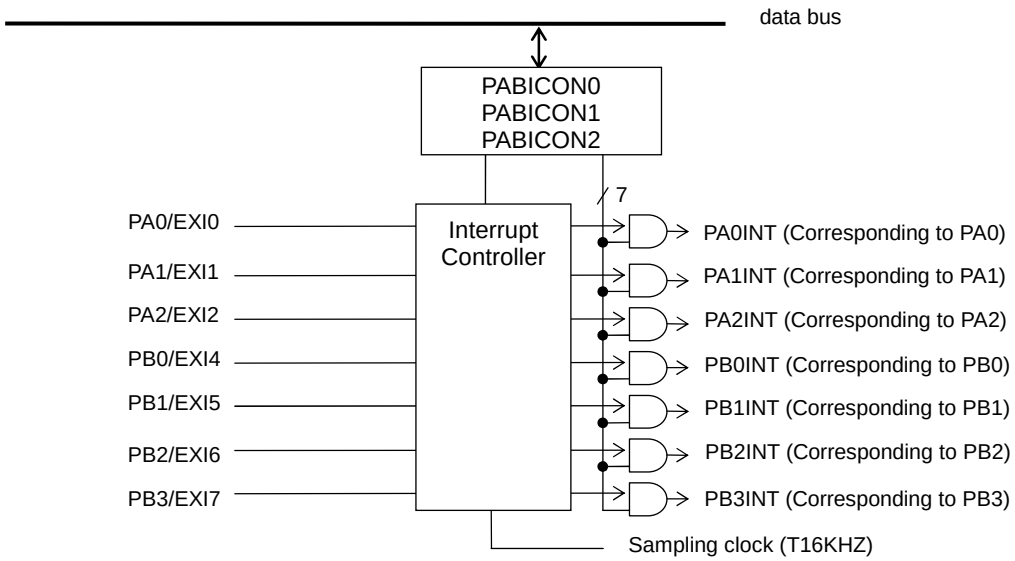
This LSI can have the external interrupts corresponding to seven ports.

19.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ)

19.1.2 Configuration

Figure 19-1 shows the configuration of Port AB interrupts control.



PABICON0 : Port AB interrupt control register 0
PABICON1 : Port AB interrupt control register 1
PABICON2 : Port AB interrupt control register 2

Figure 19-1 Configuration of Port AB Interrupts Control

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F024H	Port AB interrupt control register 0	PABICON0	—	R/W	8	00H
0F025H	Port AB interrupt control register 1	PABICON1	—	R/W	8	00H
0F026H	Port AB interrupt control register 2	PABICON2	—	R/W	8	00H

19.2.2 Port AB Interrupt Control Registers 0, 1 (PABICON0, PABICON1)

Address: 0F024H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON0	PB3E0	PB2E0	PB1E0	PB0E0	—	PA2E0	PA1E0	PA0E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F025H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON1	PB3E1	PB2E1	PB1E1	PB0E1	—	PA2E1	PA1E1	PA0E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PABICON0 and PABICON1 are special function registers (SFRs) to select an interrupt edge of Port A and Port B.

[Description of Bits]

- **PB3E0-PA0E0, PB3E1-PA0E1** (bits 7 to 0)

  The PB3E0 to PA0E0 bits and the PB3E1 to PA0E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The PnE0 bit and the PnE1 bit determine the interrupt mode of Pn (Example: When PA0E0 = "0" and PA0E1 = "1", PA0 is in rising-edge interrupt mode).

PB3E1-PA0E1	PB3E0-PA0E0	Description
0	0	Interrupt disabled mode (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

19.2.3 Port AB Interrupt Control Register 2 (PABICON2)

Address: 0F026H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON2	PB3SM	PB2SM	PB1SM	PB0SM	—	PA2SM	PA1SM	PA0SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PABICON2 is a special function register (SFR) to select detection of signal edge for interrupts with or without sampling.

[Description of Bits]

- **PB3SM-PA0SM** (bits 7 to 0)

The PB3SM to PA0SM bits are used to select detection of signal edge for Port A and Port B interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

PA0SM	Description
0	Detects the input signal edge for a PA0 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA0 interrupt with sampling.

PA1SM	Description
0	Detects the input signal edge for a PA1 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA1 interrupt with sampling.

PA2SM	Description
0	Detects the input signal edge for a PA2 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA2 interrupt with sampling.

PB0SM	Description
0	Detects the input signal edge for a PB0 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB0 interrupt with sampling.

PB1SM	Description
0	Detects the input signal edge for a PB1 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB1 interrupt with sampling.

PB2SM	Description
0	Detects the input signal edge for a PB2 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB2 interrupt with sampling.

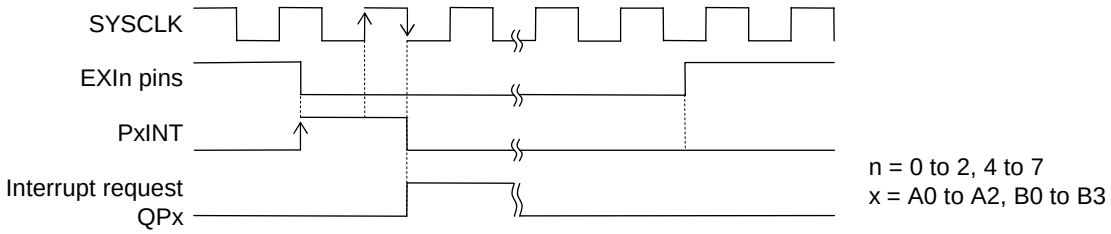
PB3SM	Description
0	Detects the input signal edge for a PB3 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB3 interrupt with sampling.

Note:
In STOP mode, since the sampling clock (T16KHZ) stops, no sampling is performed regardless of the values set in PB3SM to PA0SM.

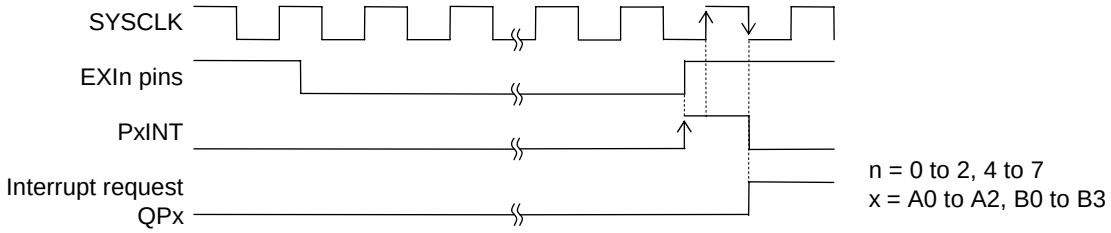
19.3 Description of Operation

19.3.1 Interrupt Request

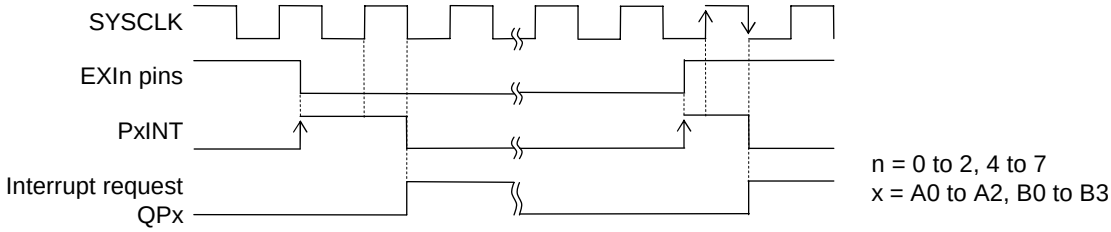
When an interrupt edge selected by the port AB interrupt control registers 0, 1, 2 (PABICON0, PABICON1, PABICON2) occurs at the external interrupt pins EXI0-2, EXI4-7 (PA0-2, PB0-3), the corresponding maskable Pxx interrupt (PA0INT–PA2INT, PB0INT-PB3INT) occurs. For details of Interrupts, see Chapter 5, "Interrupts".
Figure 19-2 shows interrupt generation timing in rising-edge interrupt mode, falling-edge interrupt mode, and both-edges interrupt mode, each without sampling, and interrupt generation timing in rising-edge interrupt mode with sampling.



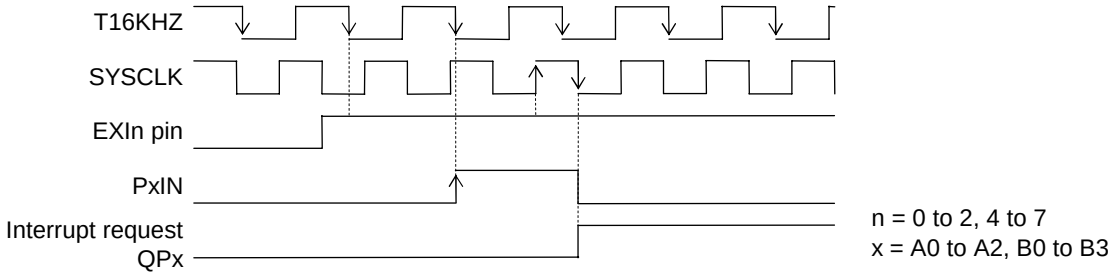
(a) When "falling-edge interrupt; without sampling" is selected



(b) When "rising-edge interrupt; without sampling" is selected



(c) When "both-edges interrupt; without sampling" is selected



(d) When "rising-edge interrupt; with sampling" is selected

Figure 19-2 External Interrupt Generation Timing

Note:
When used as external interrupt, it must be set an applicable port as input.

Chapter 20

Successive Approximation Type A/D Converter

20 Successive Approximation Type A/D Converter

20.1 Overview

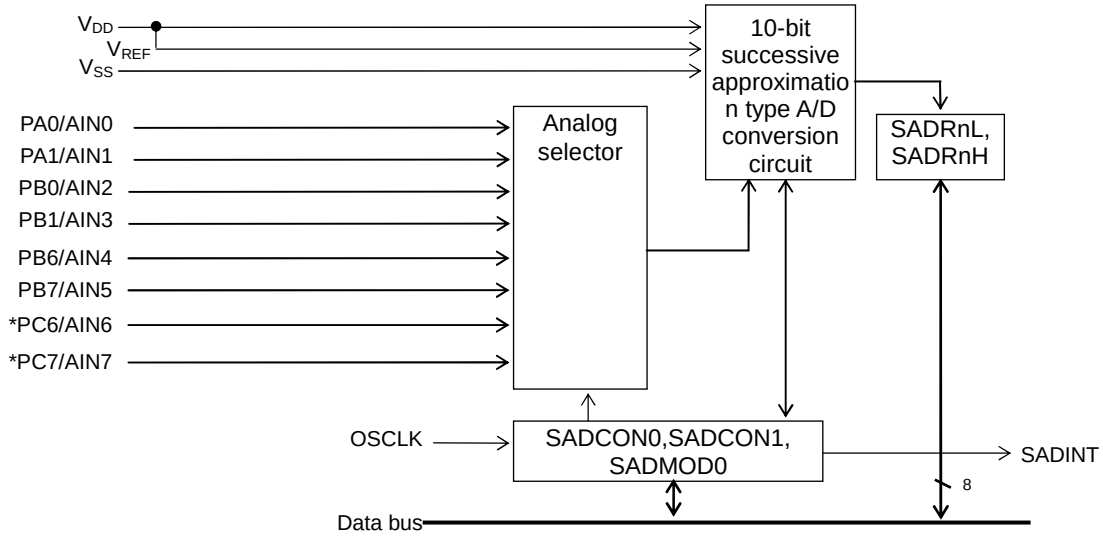
This LSI has a built-in 6-channel or 8-channel successive approximation type A/D converter (SA-ADC).

20.1.1 Features

- Built-in sample/hold 10-bit successive approximation type A-D converter, which enables channel selection from 6 channels or 8 channels
  (ML610Q111: 6-channel, ML610Q112: 8-channel)

20.1.2 Configuration

Figure 20-1 shows the configuration of SA-ADC.



SADRnL : SA-ADC result register nL
SADRnH : SA-ADC result register nH
SADCON0 : SA-ADC control register 0
SADCON1 : SA-ADC control register 1
SADMOD0 : SA-ADC mode register 0

n : 0 to 7

*: AIN6/AIN7(n=6,7) are only used by ML610Q112.

Figure 20-1 Configuration of SA-ADC

20.1.3 List of Pins

Pin name	I/O	Description
PA0/AIN0	I	Successive approximation type A/D converter input pin 0 Used for the primary function of the PA0 pin
PA1/AIN1	I	Successive approximation type A/D converter input pin 1 Used for the primary function of the PA1 pin
PB0/AIN2	I	Successive approximation type A/D converter input pin 2 Used for the primary function of the PB0 pin
PB1/AIN3	I	Successive approximation type A/D converter input pin 3 Used for the primary function of the PB1 pin
PB6/AIN4	I	Successive approximation type A/D converter input pin 4 Used for the primary function of the PB6 pin
PB7/AIN5	I	Successive approximation type A/D converter input pin 5 Used for the primary function of the PB7 pin
PC6/AIN6	I	Successive approximation type A/D converter input pin 6 Used for the primary function of the PC6 pin
PC7/AIN7	I	Successive approximation type A/D converter input pin 7 Used for the primary function of the PC7 pin

Note:
The PC6, PC7 are only used by ML610Q112.

20.2 Description of Registers

20.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F2D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F2D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F2DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F2DBH	SA-ADC result register 5H	SADR5H		R	8	00H
0F2DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F2DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F2DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F2DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H

20.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F2D0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR03	SAR02	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0L is updated after A/D conversion.

[Description of Bits]

- **SAR03-SAR02** (bits 7 to 6)
  The SAR03–SAR02 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F2D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR0B	SAR0A	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0H is updated after A/D conversion.

[Description of Bits]

- **SAR0B-SAR04** (bits 7 to 0)
  The SAR0B–SAR04 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.4 SA-ADC Result Register 1L (SADR1L)

Address: 0F2D2H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1L	SAR13	SAR12	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1L is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1L is updated after A/D conversion.

[Description of Bits]

- **SAR13-SAR12** (bits 7 to 6)
  The SAR13–SAR12 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.5 SA-ADC Result Register 1H (SADR1H)

Address: 0F2D3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1H	SAR1B	SAR1A	SAR19	SAR18	SAR17	SAR16	SAR15	SAR14
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1H is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1H is updated after A/D conversion.

[Description of Bits]

- **SAR1B-SAR14** (bits 7 to 0)
  The SAR1B–SAR14 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.6 SA-ADC Result Register 2L (SADR2L)

Address: 0F2D4H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2L	SAR23	SAR22	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2L is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2L is updated after A/D conversion.

[Description of Bits]

- **SAR23-SAR22** (bits 7 to 6)
  The SAR23–SAR22 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.7 SA-ADC Result Register 2H (SADR2H)

Address: 0F2D5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2H	SAR2B	SAR2A	SAR29	SAR28	SAR27	SAR26	SAR25	SAR24
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2H is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2H is updated after A/D conversion.

[Description of Bits]

- **SAR2B-SAR24** (bits 7 to 0)
  The SAR2B–SAR24 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.8 SA-ADC Result Register 3L (SADR3L)

Address: 0F2D6H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3L	SAR33	SAR32	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3L is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3L is updated after A/D conversion.

[Description of Bits]

- **SAR33-SAR32** (bits 7 to 6)
  The SAR33–SAR32 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.9 SA-ADC Result Register 3H (SADR3H)

Address: 0F2D7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3H	SAR3B	SAR3A	SAR39	SAR38	SAR37	SAR36	SAR35	SAR34
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3H is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3H is updated after A/D conversion.

[Description of Bits]

- **SAR3B-SAR34** (bits 7 to 0)
  The SAR3B–SAR34 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.10 SA-ADC Result Register 4L (SADR4L)

Address: 0F2D8H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4L	SAR43	SAR42	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR4L is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4L is updated after A/D conversion.

[Description of Bits]

- **SAR43-SAR42** (bits 7 to 6)
  The SAR43–SAR42 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.11 SA-ADC Result Register 4H (SADR4H)

Address: 0F2D9H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR4H	SAR4B	SAR4A	SAR49	SAR48	SAR47	SAR46	SAR45	SAR44
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR4H is a special function register (SFR) used to store SA-ADC conversion results on channel 4.
SADR4H is updated after A/D conversion.

[Description of Bits]

- **SAR4B-SAR44** (bits 7 to 0)
  The SAR4B–SAR44 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.12 SA-ADC Result Register 5L (SADR5L)

Address: 0F2DAH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5L	SAR53	SAR52	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR5L is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5L is updated after A/D conversion.

[Description of Bits]

- **SAR53-SAR52** (bits 7 to 6)
  The SAR53–SAR52 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.13 SA-ADC Result Register 5H (SADR5H)

Address: 0F2DBH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR5H	SAR5B	SAR5A	SAR59	SAR58	SAR57	SAR56	SAR55	SAR54
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR5H is a special function register (SFR) used to store SA-ADC conversion results on channel 5.
SADR5H is updated after A/D conversion.

[Description of Bits]

- **SAR5B-SAR54** (bits 7 to 0)
  The SAR5B–SAR54 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.14 SA-ADC Result Register 6L (SADR6L)

Address: 0F2DCH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6L	SAR63	SAR62	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR6L is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6L is updated after A/D conversion.
This register is available only ML610Q112.

[Description of Bits]

- **SAR63-SAR62** (bits 7 to 6)
  The SAR63–SAR62 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.15 SA-ADC Result Register 6H (SADR6H)

Address: 0F2DDH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR6H	SAR6B	SAR6A	SAR69	SAR68	SAR67	SAR66	SAR65	SAR64
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR6H is a special function register (SFR) used to store SA-ADC conversion results on channel 6.
SADR6H is updated after A/D conversion.
This register is available only ML610Q112.

[Description of Bits]

- **SAR6B-SAR64** (bits 7 to 0)
  The SAR6B–SAR64 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.16 SA-ADC Result Register 7L (SADR7L)

Address: 0F2DEH
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7L	SAR73	SAR72	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR7L is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7L is updated after A/D conversion.
This register is available only ML610Q112.

[Description of Bits]

- **SAR73-SAR72** (bits 7 to 6)
  The SAR73–SAR72 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

20.2.17 SA-ADC Result Register 7H (SADR7H)

Address: 0F2DFH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR7H	SAR7B	SAR7A	SAR79	SAR78	SAR77	SAR76	SAR75	SAR74
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR7H is a special function register (SFR) used to store SA-ADC conversion results on channel 7.
SADR7H is updated after A/D conversion.
This register is available only ML610Q112.

[Description of Bits]

- **SAR7B-SAR74** (bits 7 to 0)
  The SAR7B–SAR74 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

20.2.18 SA-ADC Control Register 0 (SADCON0)

Address: 0F2F0H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON0	—	—	—	—	—	—	—	SALP
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SALP** (bit 0)

  This bit is used to select whether A/D conversion is performed once only for each channel or continuously . When this bit is set to "0", A/D conversion is performed once only for each channel and when it is set to "1", A/D conversion is performed continuously according to the setting of SA-ADC Mode Register 0(SADMOD0).

SALP	Description
0	Single A/D conversion only (Initial value)
1	Continuous A/D conversion

20.2.19 SA-ADC Control Register 1 (SADCON1)

Address: 0F2F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	—	—	—	—	—	—	—	SARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SARUN** (bit 0)

  The SARUN bit is used to start or stop SA-ADC conversion. Setting this bit to "1" starts A/D conversion and setting it to "0" stops A/D conversion.

  When SALP of SADCON0 is "0" and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to "0".

SARUN	Description
0	Stops conversion. (Initial value)
1	Starts conversion.

Note:
Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).
The SA-ADC is available only when V_{DD} = 2.7 V to 5.5 V and OSCLK is in the ranges of 3MHz to 8.4MHz.
Do not start A/D conversion with all of bit-7 (SACH7) to bit-0 (SACH0) of the SA-ADC mode register 0 set to "0".

20.2.20 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F2F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	SACH7	SACH6	SACH5	SACH4	SACH3	SACH2	SACH1	SACH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to select A/D conversion channel(s).
The SACH0 to SACH7 bits are used to select channel on which A/D conversion is performed.
If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

[Description of Bits]

• **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

• **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

• **SACH2** (bit 2)

SACH2	Description
0	Stops conversion on channel 2. (Initial value)
1	Performs conversion on channel 2.

• **SACH3** (bit 3)

SACH3	Description
0	Stops conversion on channel 3. (Initial value)
1	Performs conversion on channel 3.

• **SACH4** (bit 4)

SACH4	Description
0	Stops conversion on channel 4. (Initial value)
1	Performs conversion on channel 4.

• **SACH5** (bit 5)

SACH5	Description
0	Stops conversion on channel 5. (Initial value)
1	Performs conversion on channel 5.

- **SACH6** (bit 6)

SACH6	Description
0	Stops conversion on channel 6. (Initial value)
1	Performs conversion on channel 6. Don't set it for ML610Q111.

- **SACH7** (bit 7)

SACH7	Description
0	Stops conversion on channel 7. (Initial value)
1	Performs conversion on channel 7. Don't set it for ML610Q111.

Note:
Do not start A/D conversion when all the SACHn (from SACH0 to SACH7) set to "0".

20.3 Description of Operation

20.3.1 Settings of A/D Conversion Channels

According to the setting of SA-ADC mode register 0 (SADMOD0), A/D conversion is performed as shown below and A/D conversion results are stored in the SA-ADC result register.

SA-ADC mode register 0/1					SA-ADC result register					Remarks
SACH7	…	SACH2	SACH1	SACH0	SADR7	…	SADR2	SADR1	SADR0	
0	0	0	0	0						Prohibition of use
0	0	0	0	1					AIN0	
0	0	0	1	0				AIN1		
0	0	0	1	1				AIN1	AIN0	
0	0	1	0	0			AIN2			
0	0	1	0	1			AIN2		AIN0	
0	0	1	1	0			AIN2	AIN1		
0	0	1	1	1			AIN2	AIN1	AIN0	
1	0	0	0	0	AIN7					
1	0	0	0	1	AIN7				AIN0	
1	0	0	1	0	AIN7			AIN1		
1	0	0	1	1	AIN7			AIN1	AIN0	
1	0	1	0	0	AIN7		AIN2			
1	0	1	0	1	AIN7		AIN2		AIN0	
1	0	1	1	0	AIN7		AIN2	AIN1		
1	0	1	1	1	AIN7		AIN2	AIN1	AIN0	

The values of the result register for the sections with a slash mark remain unchanged.
Do not start A/D conversion in the state that all the bits of the bit 7 (SACH7) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) set to "0".

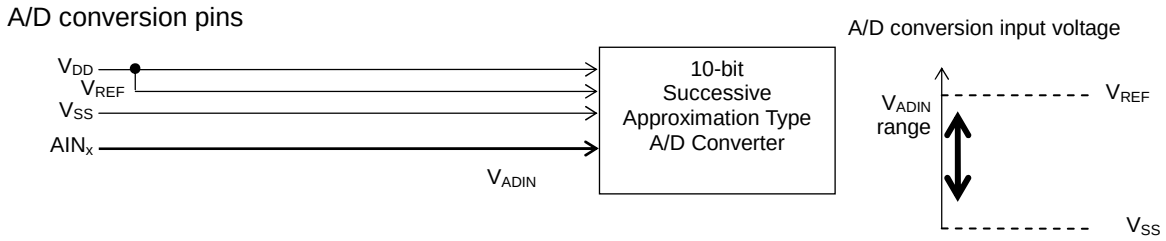


Figure 20-2 The A/D conversion pins and the conversion range

20.3.2 Operation of the Successive Approximation A/D Converter

Use the following procedure to operate the SA-ADC:

1. Before starting the SA-ADC, start oscillation of the high-speed clock (HSCLK) and wait until the oscillation stabilizes.
2. Set the SA-ADC mode register 0 (SADMOD0).
3. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the lower channel number that is selected in the SA-ADC mode register (SADMOD0).
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRnL, SADRnH), and when A/D conversion of the largest channel number that is selected is terminated, an SA-ADC conversion termination interrupt (SADINT) is generated.
5. Finally, by using bit 0 (SALP) of the SADCON0 register, it is possible to specify whether to terminate A/D conversion (SARUN bit is "0") or restart A/D conversion automatically at termination of A/D conversion of the last channel.

Even if a channel is switched during A/D conversion, the channel that was selected at the start of A/D conversion is used until an A/D conversion termination interrupt occurs.
Figure 20-3 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

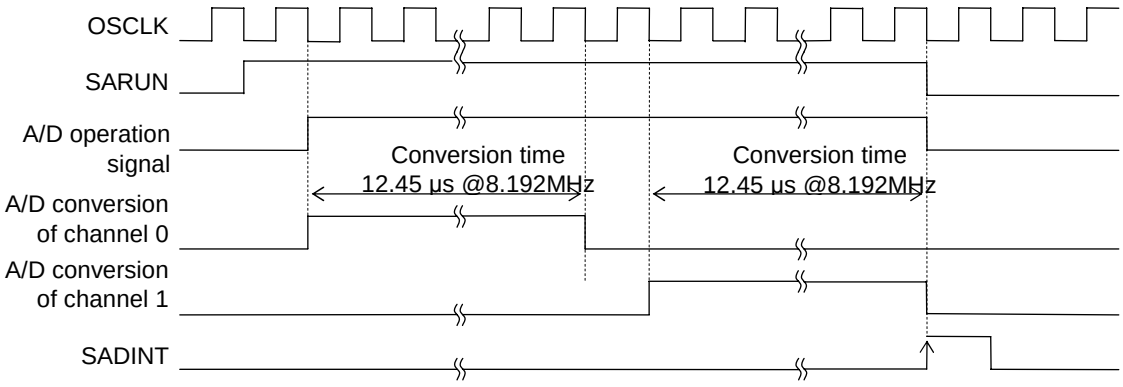


Figure 20-3 SA-ADC Operation Timing

Chapter 21

Voltage Level Supervisor

21 Voltage Level Supervisor

21.1 Overview

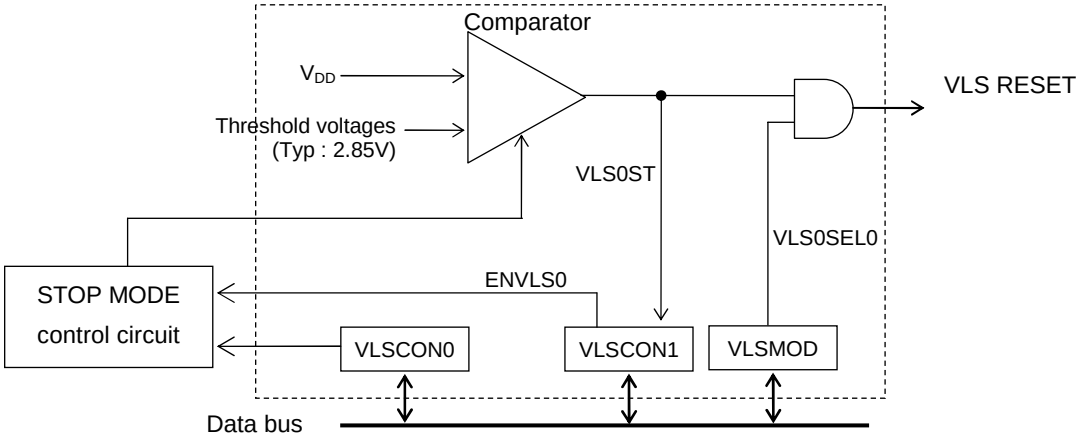
This LSI includes two channels of the voltage level supervisor (VLS).

21.1.1 Features

- Accuracy: ±3% (Typ.)
- The threshold voltages of VLS0 (V_{DD} fall) : 2.85V (Typ.)
  (V_{DD} rise) : 2.92V (Typ.)
- The threshold voltages of VLS1 (V_{DD} fall) : 4 types selectable 3.3V/ 3.6V/ 3.9V/ 4.2V (Typ.)
- The VLS0 can be used as the low voltage level detector reset.

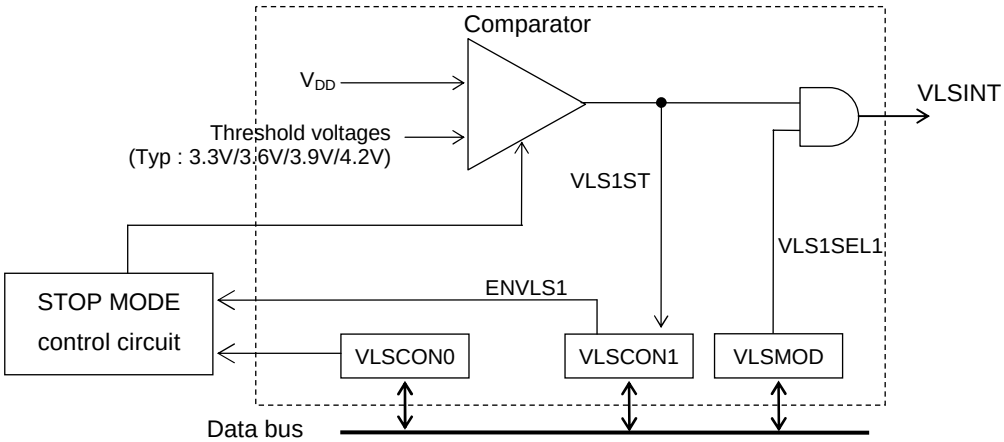
21.1.2 Configuration

VLS consists of the comparator and threshold voltage select circuits.
Figure 21-1 shows the configuration of the VLS 0.
Figure 21-2 shows the configuration of the VLS 1.



VLSCON0 : Voltage level supervisor control register 0
VLSCON1 : Voltage level supervisor control register 1
VLSMOD : Voltage level supervisor mode register

Figure 21-1 Configuration of VLS0



VLSCON0 : Voltage level supervisor control register 0
VLSCON1 : Voltage level supervisor control register 1
VLSMOD : Voltage level supervisor mode register

Figure 21-2 Configuration of VLS1

21.2 Description of Registers

21.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0D8H	Voltage level supervisor control register 0	VLSCON0	VLSCON	R/W	8/16	00H
0F0D9H	Voltage level supervisor control register 1	VLSCON1		R/W	8	11H
0F0DAH	Voltage level supervisor mode register	VLSMOD	—	R/W	8	00H

21.2.2 Voltage Level Supervisor Control Register 0 (VLSCON0)

Address: 0F0D8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VLSCON0	—	—	DVLSSP	—	—	—	VLS1LV1	VLS1LV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

VLSCON0 is a special function register (SFR) to control the voltage level supervisor (VLS).

[Description of Bits]

- **VLS1LV1-VLS1LV0** (bit 1-0)

  The VLS1LV1-VLS1LV0 bits are used to select a threshold voltage of the VLS1.

VLS1LV1	VLS1LV0	Description
0	0	3.3V (initial value)
0	1	3.6V
1	0	3.9V
1	1	4.2V

- **DVLSSP** (bit 5)

  The DVLSSP bit is used to control the VLS operation during the STOP mode. If the VLS is operating with DVLSSP set to "1", it automatically stops when the mode transits to the STOP mode. If the VLS is operating with DVLSSP set to "0", it continues operating even when the mode transits to the STOP mode.

DVLSSP	Description
0	Does not control the VLS operation during the STOP mode (initial value)
1	Stops the VLS automatically during the STOP mode

21.2.3 Voltage Level Supervisor Control Register 1 (VLSCON1)

Address: 0F0D9H
Access: R/W
Access size: 8 bits
Initial value: 11H

	7	6	5	4	3	2	1	0
VLSCON1	—	—	VLS1ST	ENVLS1	—	—	VLS0ST	ENVLS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	1

VLSCON1 is a special function register (SFR) to control the voltage level supervisor (VLS).

[Description of Bits]

- **ENVLS0** (bit 0)

  ENVLS0 bit is used to control activation (ON) or deactivation (OFF) of the VLS0.
  The VLS0 is activated (ON) and deactivated (OFF) by setting the ENVLS0 bit to "1" and "0", respectively.

ENVLS0	Description
0	VLS0 OFF
1	VLS0 ON (initial value)

- **VLS0ST** (bit 1)

  VLS0ST is the voltage level detection flag 0.
  It becomes "0" if the power supply voltage (V_{DD}) is higher than the threshold voltage and "1" if the power supply voltage is lower than the threshold voltage. When ENVLS0 is "0", VLS0ST is fixed to"0".

VLS0ST	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

- **ENVLS1** (bit 4)

  ENVLS1 bit is used to control activation (ON) or deactivation (OFF) of the VLS1.
  The VLS1 is activated (ON) and deactivated (OFF) by setting the ENVLS1 bit to "1" and "0", respectively.

ENVLS1	Description
0	VLS1 OFF
1	VLS1 ON (initial value)

- **VLS1ST** (bit 5)

  VLS1ST is the voltage level detection flag 1.
  It becomes "0" if the power supply voltage (V_{DD}) is higher than the threshold voltage and "1" if the power supply voltage is lower than the threshold voltage. When ENVLS1 is "0", VLS1ST is fixed to"0".

VLS1ST	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

21.2.4 Voltage Level Supervisor Mode Register (VLSMOD)

Address: 0F0DAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VLSMOD	—	—	VLS1SEL	—	—	—	—	VLS0SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

VLSMOD is a special function register (SFR) to select the mode of operation when detecting the voltage level.

[Description of Bits]

- **VLS0SEL0** (bit 0)

  The VLS0SEL0 bits is used to control enable/disable of the voltage level detector reset function of VLS0.
  If VLS0SEL0 is set to "1", a VLS reset function will be enabled, and if VLS0SEL0 is set to "0", it will be disabled.

VLS0SEL0	Description
0	VLS reset function of VLS0: Disabled (initial value)
1	VLS reset function of VLS0: Enabled

- **VLS1SEL1** (bit 5)

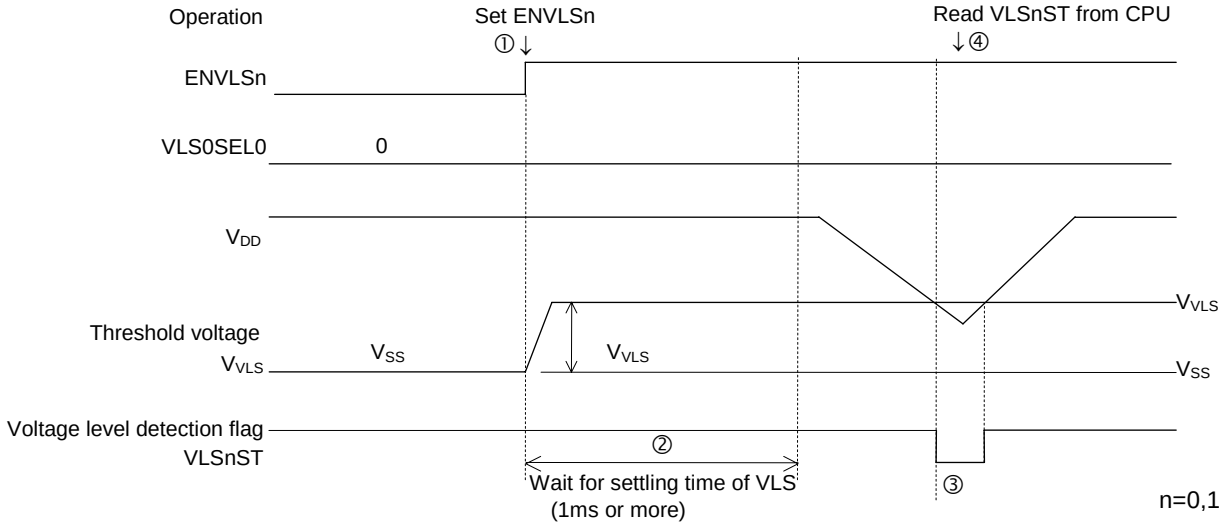
  The VLS1SEL1 bits is used to control enable/disable of the interrupt request function of VLS1.
  If VLS1SEL1 is set to "1", a VLS interrupt function will be enabled, and if VLS1SEL1 is set to "0", it will be disabled.

VLS1SEL1	Description
0	VLS Interrupt request function of VLS1: Disabled (initial value)
1	VLS Interrupt request function of VLS1: Enabled

21.3 Description of Operation

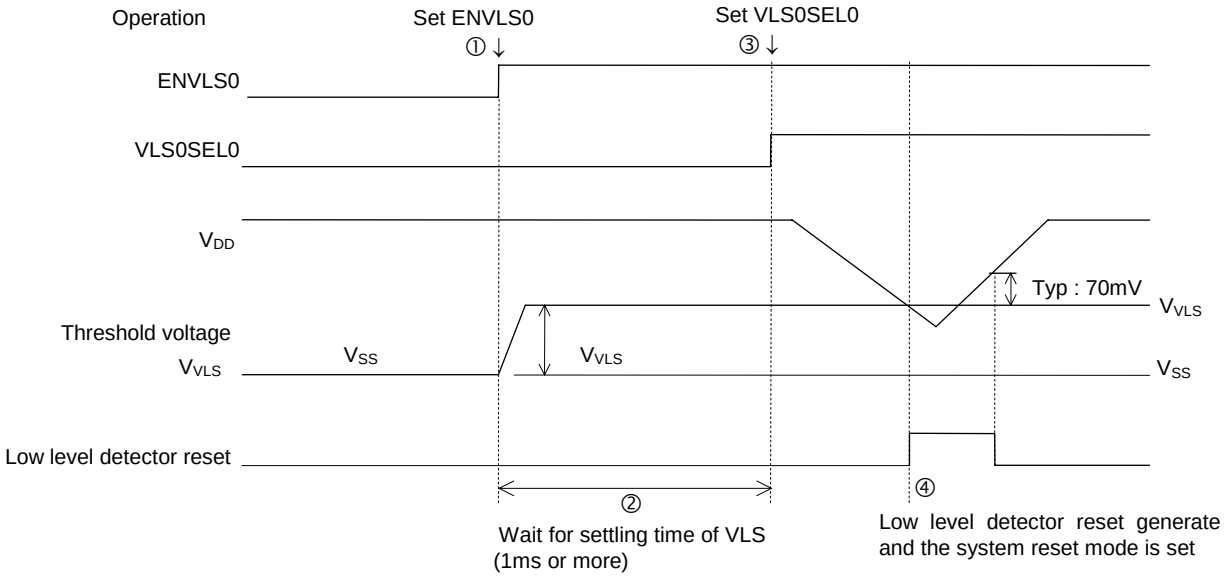
21.3.1 Operation of Voltage Level Supervisor

For the VLS, the ENVLSn bit of the VLS control register 1 (VLSCON1) controls ON/OFF, the VLP0SEL0 bit of VLSMOD controls enable/disable of the low level detector reset function of VLS0, and VLP1SEL1 bit of VLSMOD controls enable/disable of the interrupt request function of VLS1..
When ENVLSn, the enable control bit of the VLS, is set to "1", the supervisor is activated (ON). When ENVLSn is set to "0", the VLS is deactivated (OFF) and has no supply current.
The VLS requires a settling time. Set the VLS0SEL0, VLS1SEL1 bit to "1" 1ms or more after the ENVLSn bit is set to "1".
Figure 21-3 shows an example of the operation timing diagram with the voltage level detection flag (VLSnST). Figure 21-4 shows an example of the operation timing diagram with the low level detector reset function enabled.



① Set ENVLSn to "1" to turned on the voltage level supervisor.
② Wait the settling time (min. 1 ms) of the voltage level supervisor.
③ When V_{DD} drops, the voltage level detection flag (VLSnST) becomes "0".
④ Read VLSnST from CPU.

Figure 21-3 Example of Operation Timing Diagram with voltage level detection flag (VLSnST)



① Set ENVLS0 to "1" to turned on the voltage level supervisor.
② Wait the settling time (min. 1 ms) of the voltage level supervisor.
③ Set VLS0SEL0 to "1" to enabled level detector reset function.
④ VDD drops and low voltage level detector reset generate, and then the system reset mode is set.

Figure 21-4 Example of Operation Timing Diagram with low level detector reset function enabled(VLS0)

Chapter 22

Analog Comparator

22 Analog Comparator

22.1 Overview

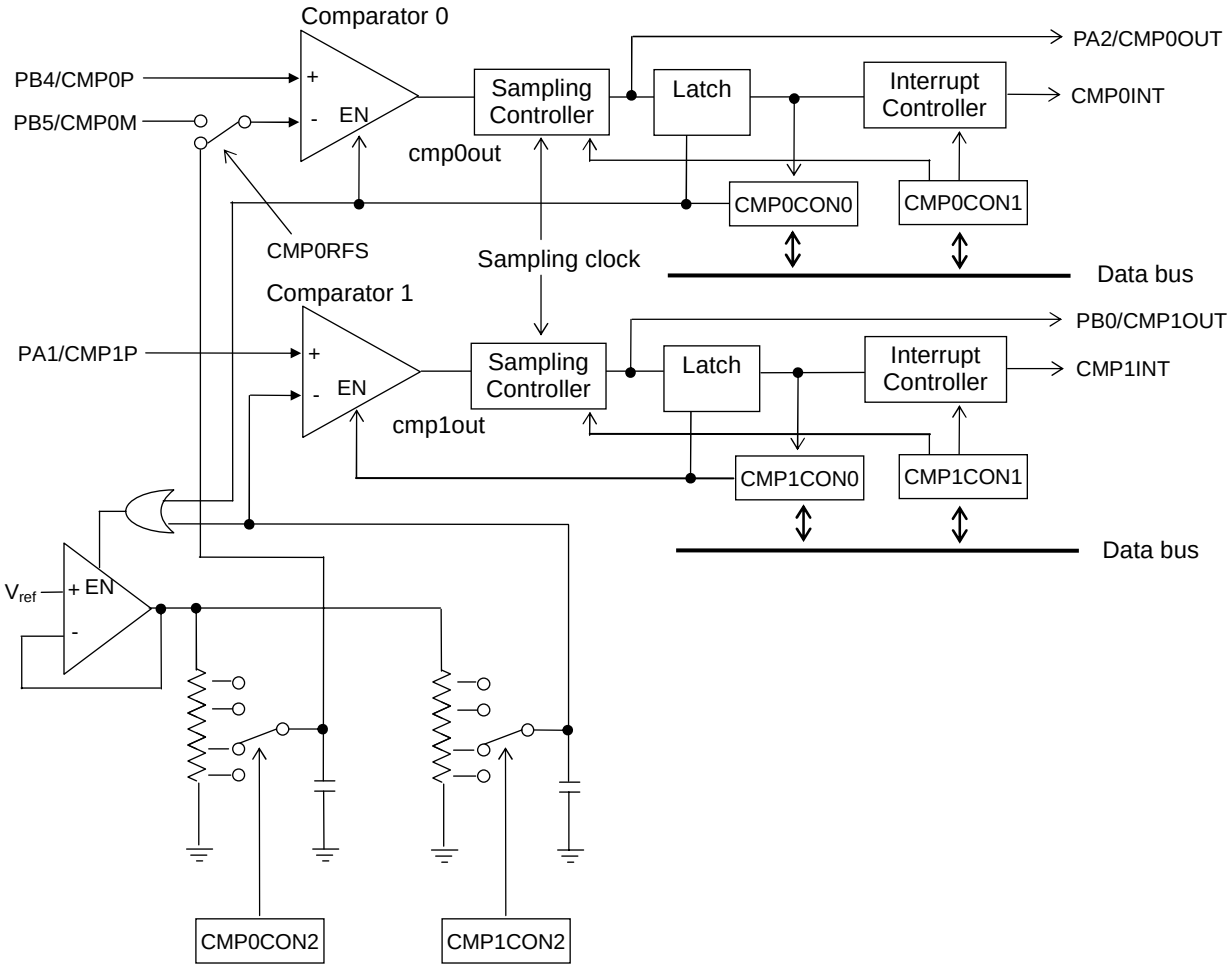
This LSI includes 2 channels of analogue comparator.
Voltage comparison (differential input) between two pins (CMP0P, CMP0M) that are input to the comparator is available.

22.1.1 Features

- The comparator output can generate an interrupt.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.
- Allows selection of with/without interrupt sampling for each bit. Sampling frequency is prepared the 3-types of value. (T16KHZ, OSCLK/64(128kHz at OSCLK=8.192MHz), OSCLK/32(256kHz at OSCLK=8.192MHz))
- The last status of comparator output (CMPnD) remains after the comparator is deactivated.
- The comparator 0 includes 20mV hysteresis at typ.

22.1.2 Configuration

Figure 22-1 shows the configuration of the Comparator.



CMP0/1CON0: Comparator 0/1 control register 0
CMP0/1CON1: Comparator 0/1 control register 1
CMP0/1CON2: Comparator 0/1 control register 2

Figure 22-1 Configuration of Analog Comparator

22.1.3 List of Pins

Pin name	I/O	Description
PB4/CMP0P	I	Analog comparator 0 non-inverted input pin
PB5/CMP0M	I	Analog comparator 0 inverted input pin
PA2/CMP0OUT	O	Analog comparator 0 output pin
PA1/CMP1P	I	Analog comparator 1 non-inverted input pin
PB0/CMP1OUT	O	Analog comparator 1 output pin

22.2 Description of Registers

22.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F950H	Comparator 0 control register 0	CMP0CON0	—	R/W	8	00H
0F951H	Comparator 0 control register 1	CMP0CON1	—	R/W	8	00H
0F952H	Comparator 0 control register 2	CMP0CON2	—	R/W	8	08H
0F954H	Comparator 1 control register 0	CMP1CON0	—	R/W	8	00H
0F955H	Comparator 1 control register 1	CMP1CON1	—	R/W	8	00H
0F956H	Comparator 1 control register 2	CMP1CON2	—	R/W	8	08H

22.2.2 Comparator 0 control register 0 (CMP0CON0)

Address: 0F950H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON0	—	—	—	—	—	—	CMP0D	CMP0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON0 is a special function register (SFR) to control the comparator.

[Description of Bits]

- **CMP0EN** (bit 0)

The CMP0EN bit is used to control ON/OFF of the comparator 0.When CMP0EN is set to "1", the comparator 0 is turned on. When it is set to "0", the comparator 0 is turned off.

CMP0EN	Description
0	Comparator 0 OFF (initial value)
1	Comparator 0 ON

- **CMP0D** (bit 1)

CMP0D indicates the status of the comparator 0 output (CMP0OUT in Figure 22-1).It is set to "1" when the PB4 pin voltage is higher than the PB5 pin voltage (PB4>PB5). It is set to "0" when the PB4 pin voltage is lower than the PB5 pin voltage (PB4<PB5).It holds the last status even after the comparator 0 is turned off (CMP0EN is set to "0").

CMP0D	Description
0	PB4 < PB5 (initial value)
1	PB4 > PB5

22.2.3 Comparator 0 control register 1 (CMP0CON1)

Address: 0F951H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON1	—	—	—	CMP0RFS	CMP0SM1	CMP0SM0	CMP0E1	CMP0E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON1 is a special function register (SFR) to control the comparator 0 interrupt.

[Description of Bits]

- **CMP0E1, CMP0E0** (bit 1, bit 0)
  The CMP0E1 and CMP0E0 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.

CMP0E1	CMP0E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

- **CMP0SM1, CMP0SM0** (bit 3, bit 2)
  The CMP0SM1 and CMP0SM0 bits are used to select with/without sampling for the comparator 0 comparison.

CMP0SM1	CMP0SM0	Description
0	0	Detects without sampling (initial value)
0	1	Detects with sampling Sampling clock = T16KHZ (16.384kHz Typ.)
1	0	Detects with sampling Sampling clock = OSCLK/64 (128kHz at OSCLK=8.192MHz)
1	1	Detects with sampling Sampling clock = OSCLK/32 (256kHz at OSCLK=8.192MHz)

- **CMP0RFS** (bit 4)
  The CMP0RFS bit is used to select the reference voltage (Vref) of the comparator 0.

CMP0RFS	Description
0	Vref= (initial value): Internal reference input
1	Vref=PB5: Differential external input

Note:
– In STOP mode, since the sampling clock stops, no sampling is performed regardless of the values set in CMP0SM1/0.
– When the sampling (OSCLK/64, OSCLK/32) is selected, HSCLK must be operated.

22.2.4 Comparator 0 control register 2 (CMP0CON2)

Address: 0F952H
Access: R/W
Access size: 8 bits
Initial value: 08H

	7	6	5	4	3	2	1	0
CMP0CON2	—	—	—	—	CMP0RF3	CMP0RF2	CMP0RF1	CMP0RF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

CMP0CON2 is a special function register (SFR) to select the reference voltage of the comparator 0.

[Description of Bits]

- **CMP0RF3-CMP0RF0** (bit 3 to 0)
  The CMP0RF0, CMP0RF1, CMP0RF2, and CMP0RF3 bits are used to select the reference voltage of the comparator 0. This setting is valid when the reference voltage (Vref) of the comparator 0 is set to the internal reference input (CMP0RFS=0). A setting of 0h (0.05V) is possible without a guaranteed accuracy.

CMP0RF3	CMP0RF2	CMP0RF1	CMP0RF0	Comparator 0 Reference voltage
0	0	0	0	0.05V (no guaranteed accuracy)
0	0	0	1	0.10V
0	0	1	0	0.15V
0	0	1	1	0.20V
0	1	0	0	0.25V
0	1	0	1	0.30V
0	1	1	0	0.35V
0	1	1	1	0.40V
1	0	0	0	0.45V (initial value)
1	0	0	1	0.50V
1	0	1	0	0.55V
1	0	1	1	0.60V
1	1	0	0	0.65V
1	1	0	1	0.70V
1	1	1	0	0.75V
1	1	1	1	0.80V

22.2.5 Comparator 1 control register 0 (CMP1CON0)

Address: 0F954H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP1CON0	—	—	—	—	—	—	CMP1D	CMP1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMP1CON0 is a special function register (SFR) to control the comparator.

[Description of Bits]

- **CMP1EN** (bit 0)

  The CMP1EN bit is used to control ON/OFF of the Comparator 1.
  When CMP1EN is set to "1", the Comparator 1 is turned on. When it is set to "0", the Comparator 1 is turned off.

CMP1EN	Description
0	Comparator 1 OFF (initial value)
1	Comparator 1 ON

- **CMP1D** (bit 1)

  CMP1D indicates the status of the Comparator 1 output (CMP1OUT in Figure 22-1).
  It is set to "1" when the PA1 pin voltage is higher than the internal reference voltage (PA1>Internal reference voltage). It is set to "0" when the PA1 pin voltage is lower than the internal reference voltage (PA1<Internal reference voltage).
  It holds the last status even after the Comparator 1 is turned off (CMP1EN is set to "0").

CMP1D	Description
0	PA1 < Internal reference voltage (initial value)
1	PA1 > Internal reference voltage

22.2.6 Comparator 1 control register 1 (CMP1CON1)

Address: 0F955H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP1CON1	—	—	—	—	CMP1 SM1	CMP1 SM0	CMP1E1	CMP1E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMP1CON1 is a special function register (SFR) to control the Comparator 1 interrupt.

[Description of Bits]

- **CMP1E1, CMP1E0** (bit 1, bit 0)
  The CMP1E1 and CMP1E0 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.

CMP1E1	CMP1E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

- **CMP1SM1, CMP1SM0** (bit 1, bit 0)
  The CMP1SM1 and CMP1SM0 bits are used to select with/without sampling for the Comparator 1 comparison.

CMP1SM1	CMP1SM0	Description
0	0	Detects without sampling (initial value)
0	1	Detects with sampling Sampling clock = T16KHZ (16.384kHz Typ.)
1	0	Detects with sampling Sampling clock = OSCLK/64 (128kHz at OSCLK=8.192MHz)
1	1	Detects with sampling Sampling clock = OSCLK/32 (256kHz at OSCLK=8.192MHz)

Note:
– In STOP mode, since the sampling clock stops, no sampling is performed regardless of the values set in CMP1SM1/0.
– When the sampling (OSCLK/64, OSCLK/32) is selected, HSCLK must be operated.

22.2.7 Comparator 1 control register 2 (CMP1CON2)

Address: 0F956H
Access: R/W
Access size: 8 bits
Initial value: 08H

	7	6	5	4	3	2	1	0
CMP1CON2	—	—	—	—	CMP1RF3	CMP1RF2	CMP1RF1	CMP1RF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

CMP1CON2 is a special function register (SFR) to select the reference voltage of the Comparator 1.

[Description of Bits]

- **CMP1RF3-0** (bit 3 to 0)
  The CMP1RF0, CMP1RF1, CMP1RF2, and CMP1RF3 bits are used to select the reference voltage of the Comparator 1. This setting is valid when the reference voltage (Vref) of the Comparator 1 is set to the internal reference input (CMP1RFS=0). A setting of 0h (0.05V) is possible without a guaranteed accuracy.

CMP1RF3	CMP1RF2	CMP1RF1	CMP1RF0	Comparator 1 Reference voltage
0	0	0	0	0.05V (no guaranteed accuracy)
0	0	0	1	0.10V
0	0	1	0	0.15V
0	0	1	1	0.20V
0	1	0	0	0.25V
0	1	0	1	0.30V
0	1	1	0	0.35V
0	1	1	1	0.40V
1	0	0	0	0.45V (initial value)
1	0	0	1	0.50V
1	0	1	0	0.55V
1	0	1	1	0.60V
1	1	0	0	0.65V
1	1	0	1	0.70V
1	1	1	0	0.75V
1	1	1	1	0.80V

22.3 Description of Operation

22.3.1 Comparator Functions

The comparator compares the input voltages of the CMPnP and CMPnM pins to output the result to the CMPnD bit of the comparator control register 0 (CMPnCON0).
CMPnEN of CMPnCON0 is controlled by the comparator enable. When CMPnEN is set to "1", the comparator is activated (ON). When CMPnEN is set to "0", the comparator is deactivated (OFF) and has no supply current.
The comparison result is read from the CMPnD bit. When CMPnD is "1", it indicates that the input voltage of the CMPnP pin is higher than that of the CMPnM pin. When CMPnD is "0", it indicates that the input voltage of the CMPnP pin is lower than that of the CMPnM pin.
The comparator requires a settling time. Read CMPnD bit 100us or more after CMPnEN bit is set to "1".
Figure 22-2 shows an example of the operation timing diagram.

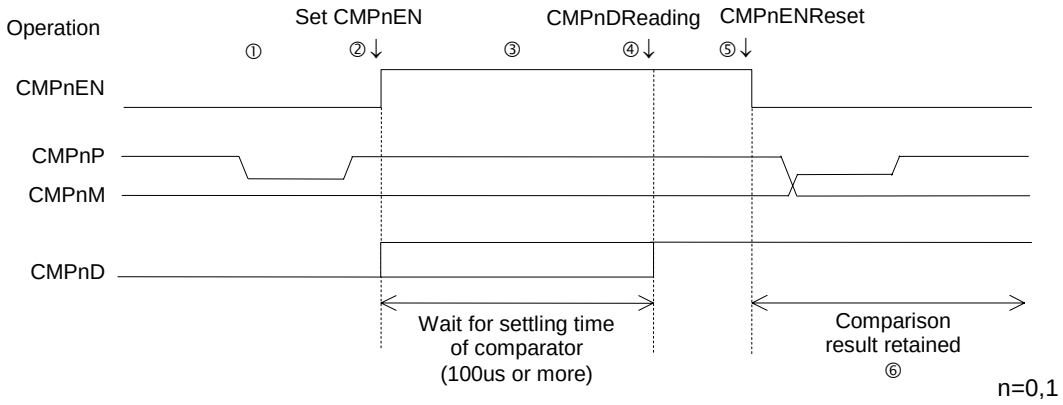


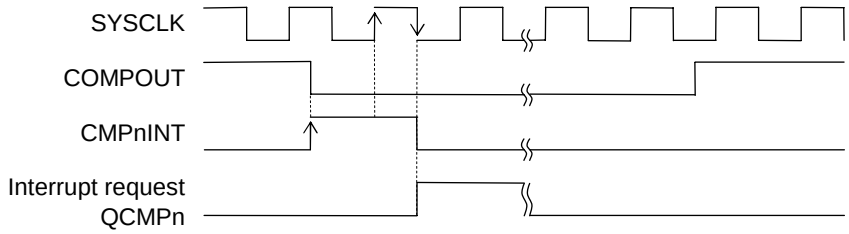
Figure 22-2 Example of Operation Timing Diagram (n=0,1)

The operations in Figure 22-2 are described below.

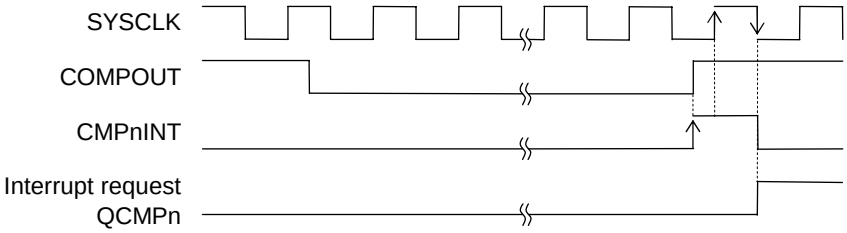
① Select the interrupt mode by CMPnCON1.
② Set CMPnEN to "1" to turn on the comparator.
③ Wait the settling time (min. 100 us) of the comparator.
④ Read the comparison result (CMPnD).
⑤ Set CMPnEN to "0" to turn off the comparator. At the same time, the result is retained.
⑥ CMPnD can be read after CMPnEN is set to "0" because CMPnD holds the comparison result at the time when CMPnEN is set to "0".

22.3.2 Interrupt Request

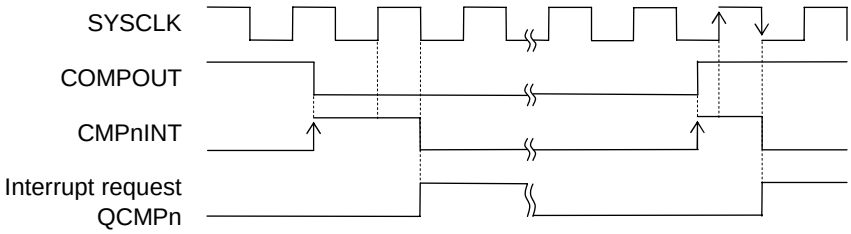
When an interrupt edge selected by the comparator control register 1 (CMPnCON1) occurs on the comparison result of the comparator, a comparator interrupt (CMPnINT) is generated. For the comparator interrupt, the edge can be selected. Figure 22-3 shows the interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



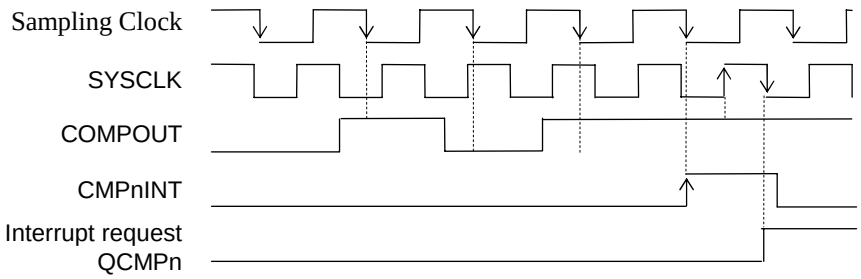
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 22-3 Comparator Interrupt Generation Timing

Chapter 23

Data Flash Memory

23 Data Flash Memory

23.1 Overview

This LSI includes the data flash memory (data memory space (4 Kbytes: 1 Kbytes x 4 sectors)) that is rewritable by using a special function register (SFR) programmatically.

23.1.1 Features

- Rewrite counts[*1] : 6000 times, V_{DD}=2.7 to 5.5 V@-20 to 85°C.
- Sector Erase : Erase of 512 words (1 Kbytes).
- Block erase : Erase of 2 Kwords (4 Kbytes).
- Writing : 1-word write.

[*1]: Rewrite counts is counted as one even if you erase suspend.

23.2 Description of Registers

23.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	—	W	8	00H
0F0E5H	Flash acceptor	FLASHACP	—	W	8	00H
0F0E6H	Flash segment register	FLASHSEG	—	R/W	8	00H
0F0E7H	Flash self register	FLASHSLF	—	R/W	8	00H
0F0E8H	Flash protection register	FLASHPRT	—	R/W	8	00H
0F0EEH	Flash erase abort source select register	FLASHEAS	—	R/W	8	00H
0F0EFH	Flash erase status register	FLASHEST	—	R/W	8	00H

23.2.2 Flash Address Register (FLASHAL,H)

Address: 0F0E0H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAL	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAH	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHAL and FLASHAH are special function registers (SFRs) that set the flash memory rewrite addresses.

[Description of Bits]

- **FA7-FA0** (bits 7-0)
  The FA7 to FA0 bits are used to set the lower address for 1-word write.
  Note that the bit 0 is fixed to 0 and cannot be written.

- **FA15-FA8** (bits 7-0)
  The FA15 to FA8 bits are used to set the upper address for sector erase, block erase, or 1-word write.
  The upper address is specified by the flash segment registers FSEG0, FSEG1, and FA15 to FA8.
  Table 23-1 shows the address setting values for sector erase, and table 23-2 shows the address values for block erase.

Table 23-1 Address Setting Values for Sector Erase

Area for sector erase				FLASHSEG		FLASHAH							
Segment	Address			FSEG1	FSEG0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 2	0000H	to	03FFH	1	0	0	0	0	0	0	0	0	0
	0400H	to	07FFH	1	0	0	0	0	0	0	1	0	0
	0800H	to	0BFFH	1	0	0	0	0	0	1	0	0	0
	0C00H	to	0FFFH	1	0	0	0	0	0	1	1	0	0

Table 23-2 Address Setting Values for Block Erase

Area for block erase				FLASHSEG		FLASHAH							
Segment	Address			FSEG1	FSEG0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 2	0000H	to	0FFFH	1	0	0	0	0	0	0	0	0	0

23.2.3 Flash Data Register (FLASHDL,H)

Address: 0F0E2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDL	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDH	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHDL and FLASHDH are special function registers (SFRs) that sets the flash memory rewrite data.

[Description of Bits]

- **FD7-FD0** (bits 7-0)
  The FD7 to FD0 bits are used to set the lower write data for 1-word write.

- **FD15-FD8** (bits 7-0)
  The FD15 to FD8 bits are used to set the upper write data for 1-word write.
  Writing to FD15-FD8 starts the 1-word write.

Note:
Clear the contents of the target addresses in advance. The content of an overwritten address is not guaranteed.
Wiriting to FLASHDH start the 1-word write. Write data to FLASHDL and FLASHDH in this order. Or, perform the word writes.

23.2.4 Flash Control Register (FLASHCON)

Address: 0F0E4H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHCON	—	—	—	—	—	—	FSERS	FERS
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHCON is a write-only special function register (SFR) to control the block erase or the sector erase for the flash memory rewrite.

[Description of Bits]

- **FERS** (bit 0)
  The FERS bit is used to start the block erase.
  Setting the FERS bit to "1" erases the block specified by the FSEG1 to FSEG0 bit of FLASHSEG register, and the FA15 to FA8 bit of FLASHAH register. This bit is automatically set to "0" after completing the erase.

- **FSERS** (bit 1)
  FSERS is a bit to specify the start of the sector erase.
  Setting the FSERS bit to "1" erases the sector specified by the FSEG1 to FSEG0 bit of FLASHSEG register, and the FA15 to FA8 bit of FLASHAH register. This bit is automatically set to "0" after completing the erase.

FSERS	FERS	Description
0	0	Stop erase (initial value)
0	1	Start block erase
1	0	Start sector erase
1	1	Start block erase

23.2.5 Flash Accepter (FLASHACP)

Address: 0F0E5H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHACP	fac7	fac6	fac5	fac4	fac3	fac2	fac1	fac0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHACP is a write-only special function register (SFR) to control the sector erase, the block erase for the flash memory rewrite or enable/disable the 1-word write operation.

[Description of Bits]

- **fac7 to fac0** (bit 7 to 0)

  The fac7 to fac0 bits are used to restrict the sector erase, block erase, or 1-word write operation in order to prevent an unintended operation.

  Writing "0FAH" and "0F5H" to FLASHACP in this order enables a one-time sector erase, block erase, or 1-word write. For subsequent sector erases, block erases, or 1-word writes, you must write "0FAH" and "0F5H" to FLASHACP each time.

  Even if another instruction is inserted between "0FAH" and "0F5H" written to FLASHACP, the sector erase, block erase, or 1-word write is enabled. Note that, if data other than "0F5H" is written to FLASHACP after "0FAH" is written, the "0FAH" write processing becomes invalid. So, you must rewrite "0FAH" at first.

23.2.6 Flash Segment Register (FLASHSEG)

Address: 0F0E6H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSEG	—	—	—	—	—	—	FSEG1	FSEG0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSEG is a special function register (SFR) that sets the flash memory rewrite segment address.

[Description of Bits]

• **FSEG1, FSEG0** (bits 1 to 0)
The FSEG1and FSEG0 bits are used to set the flash memory segment address.

FSEG1	**FSEG0**	Description
0	0	Disabled (initial value)
0	1	Disabled
1	0	Segment 2 is selected
1	1	Disabled

23.2.7 Flash Self Register (FLASHSLF)

Address: 0F0E7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSLF	—	—	—	—	—	—	—	FSELF
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSLF is a special function register (SFR) that control the data flash memory rewrite function.

[Description of Bits]

• **FSELF** (bit 0)
The FSELF is a bit that controls the flash memory rewrite function. Writing "1" to FSELF enables the flash rewrite function.
FSELF is set to "0" at system reset.

FSEG0	Description
0	Data-Flash Memory Rewrite Function: Disabled (initial value)
1	Data-Flash Memory Rewrite Function: Enabled

23.2.8 Flash Protection Register (FLASHPRT)

Address: 0F0E8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHPRT	—	—	—	—	FPRT3	FPRT2	FPRT1	FPRT0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHPRT is a special function register (SFR) to control the sector erase, block erase, and 1-word write in the segment 2 0000H to 03FFH, 0400H to 07FFH, 0800H to 0BFFH, or 0C00H to 0FFFH.

[Description of Bits]

- **FPRT0** (bit 0)

The FPRT0 is a bit to control the sector erase, block erase, and 1-word write in the segment 2 0000H to 03FFH. Writing "1" to FPRT0 sets FPRT0 to "1", and disables the subsequent sector erases, block erases, and 1-word writes in the segment 2 0000H to 03FFH. Even if "0" is written to FPRT0 after "1" is written to FPRT0, it is not set to "0". FPRT0 is set to "0" at system reset.

FPRT0	Description
0	The sector erase, block erase, and 1-word write in the segment 2 0000H to 03FFH: Enabled (initial value)
1	The sector erase, block erase, and 1-word write in the segment 2 0000H to 03FFH: Disabled

- **FPRT1** (bit 1))

The FPRT1 is a bit to control the sector erase, block erase, and 1-word write in the segment 2 0400H to 07FFH. Writing "1" to FPRT1 sets FPRT1 to "1", and disables the subsequent sector erases, block erases, and 1-word writes in the segment 2 0400H to 07FFH. Even if "0" is written to FPRT1 after "1" is written to FPRT1, it is not set to "0". FPRT1 is set to "0" at system reset.

FPRT1	Description
0	The sector erase, block erase, and 1-word write in the segment 2 0400H to 07FFH: Enabled (initial value)
1	The sector erase, block erase, and 1-word write in the segment 2 0400H to 07FFH: Disabled

- **FPRT2** (bit 2)

The FPRT2 is a bit to control the sector erase, block erase, and 1-word write in the segment 2 0800H to 0BFFH. Writing "1" to FPRT2 sets FPRT2 to "1", and disables the subsequent sector erases, block erases, and 1-word writes in the segment 2 0800H to 0BFFH. Even if "0" is written to FPRT2 after "1" is written to FPRT2, it is not set to "0". FPRT2 is set to "0" at system reset.

FPRT2	Description
0	The sector erase, block erase, and 1-word write in the segment 2 0800H to 0BFFH: Enabled (initial value)
1	The sector erase, block erase, and 1-word write in the segment 2 0800H to 0BFFH: Disabled

- **FPRT3** (bit 3)

  The FPRT3 is a bit to control the sector erase, block erase, and 1-word write in the segment 2 0C00H to 0FFFH. Writing "1" to FPRT3 sets FPRT3 to "1", and disables the subsequent sector erases, block erases, and 1-word writes in the segment 2 0C00H to 0FFFH. Even if "0" is written to FPRT3 after "1" is written to FPRT3, it is not set to "0"..
  FPRT3 is set to "0" at system reset.

FPRT3	Description
0	The sector erase, block erase, and 1-word write in the segment 2 0C00H to 0FFFH: Enabled (initial value)
1	The sector erase, block erase, and 1-word write in the segment 2 0C00H to 0FFFH: Disabled

Note:
Writing "1" to one of FPRT0 to FPRT3 disables the subsequent block erases in the segment 2 0000H to 0FFFH.

23.2.9 Flash Erase Abort Source Select Register (FLASHEAS)

Address: 0F0EEH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHEAS	FEPB3S	FEPB2S	FEPB1S	FEPB0S	—	FEPA2S	FEPA1S	FEPA0S
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHEAS is a special function register (SFR) to select the external interrupt to abort the flash erase operation.

[Description of Bits]

- **FEPA0S** (bit 0)
  When this bit is set to "1", PA0INT is selected as the erase abort source.

- **FEPA1S** (bit 1)
  When this bit is set to "1", PA1INT is selected as the erase abort source.

- **FEPA2S** (bit 2)
  When this bit is set to "1", PA2INT is selected as the erase abort source.

- **FEPB0S** (bit 4)
  When this bit is set to "1", PB0INT is selected as the erase abort source.

- **FEPB1S** (bit 5)
  When this bit is set to "1", PB1INT is selected as the erase abort source.

- **FEPB2S** (bit 6)
  When this bit is set to "1", PB2INT is selected as the erase abort source.

- **FEPB3S** (bit 7)
  When this bit is set to "1", PB3INT is selected as the erase abort source.

Note:
When multiple selection has been made, the erase is aborted for any one of the interrupts.
This function requires the target interrupt function to be enabled on the interrupt controller side.
For setting each interrupt, see Chapter 5, "Interrupt" and Chapter 19, "Port AB interrupt control circuit".

23.2.10 Flash Erase Status Register (FLASHEST)

Address: 0F0EFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHEST	ESTAT	—	—	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHEST is a special function register (SFR) to indicate the flash erase status.

[Description of Bits]

- **ESTAT** (bit 7)

  The ESTAT bit is used to indicate the erase status.
  If erase is completed successfully, it is set to "0"..
  If erase is aborted, it is set to "1".It is returned to "0" by writing "0"

ESTAT	Description
0	Not erasing, or erase has been completed successfully
1	Erase has been aborted by the source selected to FLASHEAS

Note:
ESTAT shows "0" if erase operation is aborted by the power-off or reset.

23.3 Description of Operation

The rewrite function includes the sector erase function that erases by 1K bytes, the block erase function that erases by 4K bytes, and the 1-word write function that writes by 1 word (2 bytes).
It also includes the flash rewrite acceptor function which restricts the rewrite operation, to prevent an improper rewriting of the flash memory. Writing "0FAH" and "0F5H" to flash acceptor (FLASHACP) in this order enables a one-time sector erase, block erase, or 1-word write.
For the specification of the flash memory, see the section for flash memory specification in Appendix C, "Electrical Characteristics"

Note:
Use it with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON1), and with HSCLK selected as system clock.

23.3.1 Sector Erase Function

This function erases the flash memory data by sector (1K bytes).
When writing "01H" to the flash self register (FLASHSLF), writing "0FAH" and "0F5H" to the flash acceptor (FLASHACP), setting block addresses for the flash segment register (FLASHSEG) and the flash address register H (FLASHAH), and then writing "1" to the flash control register (FLASHCON) FSERS bit, data in the sector (1Kbytes) specified by FLASHSEG and FLASHAH is erased.
During the sector erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that set the FLASHCON FSERS bit to "1".
Figure 23-1 shows the sector erase flow

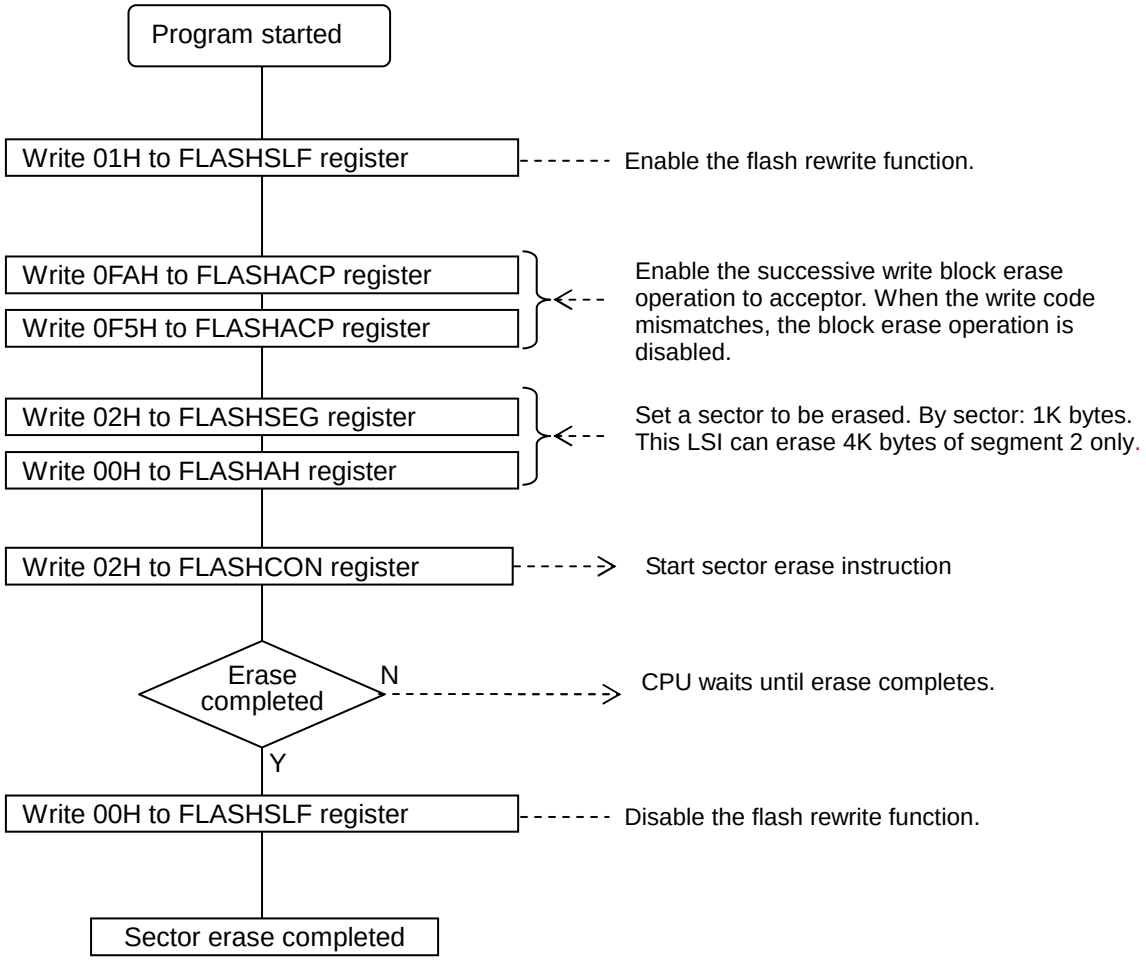


Figure 23-1 Sector Erase Flow

Note:
– Clear the WDT counter of WDT as required.
– Since the WDT counter cannot be cleared while erasing, set the WDT overflow period to be equal to or more than 125ms.

– The sector erase is disabled in the segment 2 0000H to 03FFH area after writing "1" to the flash protection register (FLASHPRT) FPRT0 bit.
– The sector erase is disabled in the segment 2 0400H to 07FFH area after writing "1" to the flash protection register (FLASHPRT) FPRT1 bit.
– The sector erase is disabled in the segment 2 0800H to 0BFFH area after writing "1" to the flash protection register (FLASHPRT) FPRT2 bit.
– The sector erase is disabled in the segment 2 0C00H to 0FFFH area after writing "1" to the flash protection register (FLASHPRT) FPRT3 bit.

– Be sure to set the NOP instruction twice or more, following the sector erase start instruction.

Figure 23-2 shows a sample program of sector erase (assuming that the FLASHSEG register is already set).

```
        LEA     offset FLASHAH          ; EA <- FLASHAH address
        MOV     R0,     #0FAH           ; Flash acceptor enable data
        MOV     R1,     #0F5H           ; Flash acceptor enable data
        MOV     R2,     #01H
        MOV     R3,     #00H
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8       ; ER4 <- FLASHACP address
        MOV     R6,     #(offset FLASHCON)&0FFH
        MOV     R7,     #(offset FLASHCON)>>8       ; ER6 <- FLASHCON address
        MOV     R8,     #02H
          :
        (Set the erase start block address in R9)
MARK:
        ST      R2,     FLASHSLF        ; Enables the flash rewrite function
        ST      R0,     [ER4]           ; Enable flash acceptor
        ST      R1,     [ER4]           ; Enable flash acceptor
        ST      R9 ,    [EA]            ; Set block address
        ST      R8,     [ER6]           ; Start sector erase
        NOP                             ; * Always set
        NOP                             ; * Always set
        ST      R3,     FLASHSLF        ; Disables the flash rewrite function
        ;
```

Figure 23-2 Sample Program of Sector Erase

Note:
- Be sure to set the NOP instruction twice or more, following the sector erase start instruction.
- Use it with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON1), and with HSCLK selected as system clock.

23.3.2 Block Erase Function

This function erases the flash memory data by block (4K bytes).
When writing "01H" to the flash self register (FLASHSLF), writing "0FAH" and "0F5H" to the flash acceptor (FLASHACP), setting block addresses for the flash segment register (FLASHSEG) and the flash address register H (FLASHAH), and then writing "1" to the flash control register (FLASHCON) FERS bit, data in the block (4Kbytes) specified by FLASHSEG and FLASHAH is erased.
During the block erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that set the FLASHCON FERS bit to "1".
Figure 23-3 shows the block erase flow

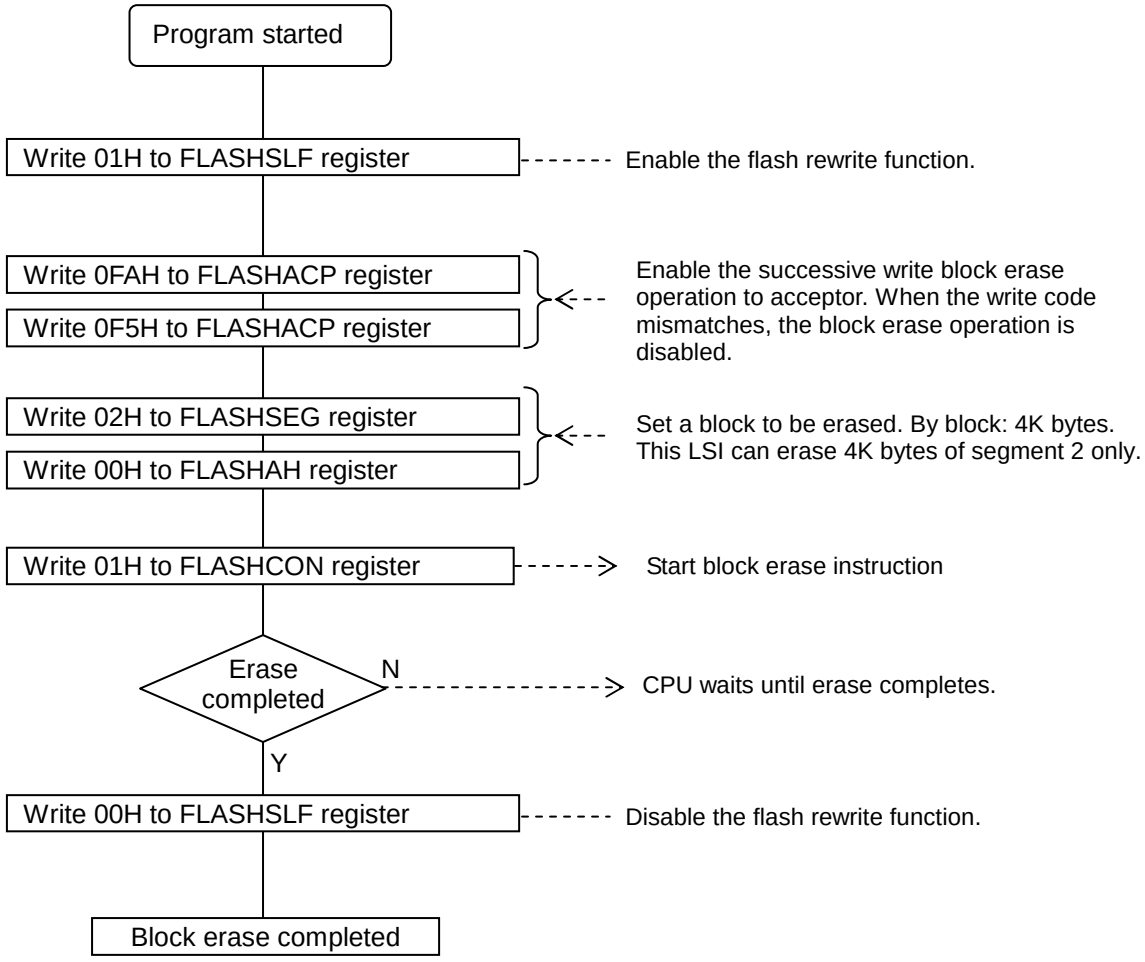


Figure 23-3 Block Erase Flow

Note:
– Clear the WDT counter of WDT as required.
– Since the WDT counter cannot be cleared while erasing, set the WDT overflow period to be equal to or more than 125ms.

– Writing "1" to one of FPRT0 to FPRT3 disables the subsequent block erases in the segment 2 0000H to 0FFFH.

– Be sure to set the NOP instruction twice or more, following the block erase start instruction.

Figure 23-4 shows a sample program of block erase (assuming that the FLASHSEG register is already set).

```
        LEA     offset FLASHAH          ; EA <- FLASHAH address
        MOV     R0,     #0FAH           ; Flash acceptor enable data
        MOV     R1,     #0F5H           ; Flash acceptor enable data
        MOV     R2,     #01H
        MOV     R3,     #00H
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8       ; ER4 <- FLASHACP address
        MOV     R6,     #(offset FLASHCON)&0FFH
        MOV     R7,     #(offset FLASHCON)>>8       ; ER6 <- FLASHCON address
          :
        (Set the erase start block address in R9)
MARK:
        ST      R2,     FLASHSLF        ; Enables the flash rewrite function
        ST      R0,     [ER4]           ; Enable flash acceptor
        ST      R1,     [ER4]           ; Enable flash acceptor
        ST      R9 ,    [EA]            ; Set block address
        ST      R2,     [ER6]           ; Start block erase
        NOP                             ; * Always set
        NOP                             ; * Always set
        ST      R3,     FLASHSLF        ; Disables the flash rewrite function
        ;
```

Figure 23-4 Sample Program of Block Erase

Note:
- Be sure to set the NOP instruction twice or more, following the block erase start instruction.
- Use it with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON1), and with HSCLK selected as system clock.

23.3.3 1-Word Write Function

This function writes data to the flash memory by 1 word (2 bytes).
Write "01H" to the flash self register (FLASHSLF) and write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the address in the flash segment register (FLASHSEG) and the flash address register L, H (FLASHAL,H). Then, write data to the flash data register L, H (FLASHDL,H) to write the data in the address specified by FLASHSEG and FLASHAL, H.
During the 1-word write, the CPU is stopped. When the write is completed, the program is restarted from the instruction following the write to FLASHDH instruction.
Figure 23-5 shows the 1-word write flow.

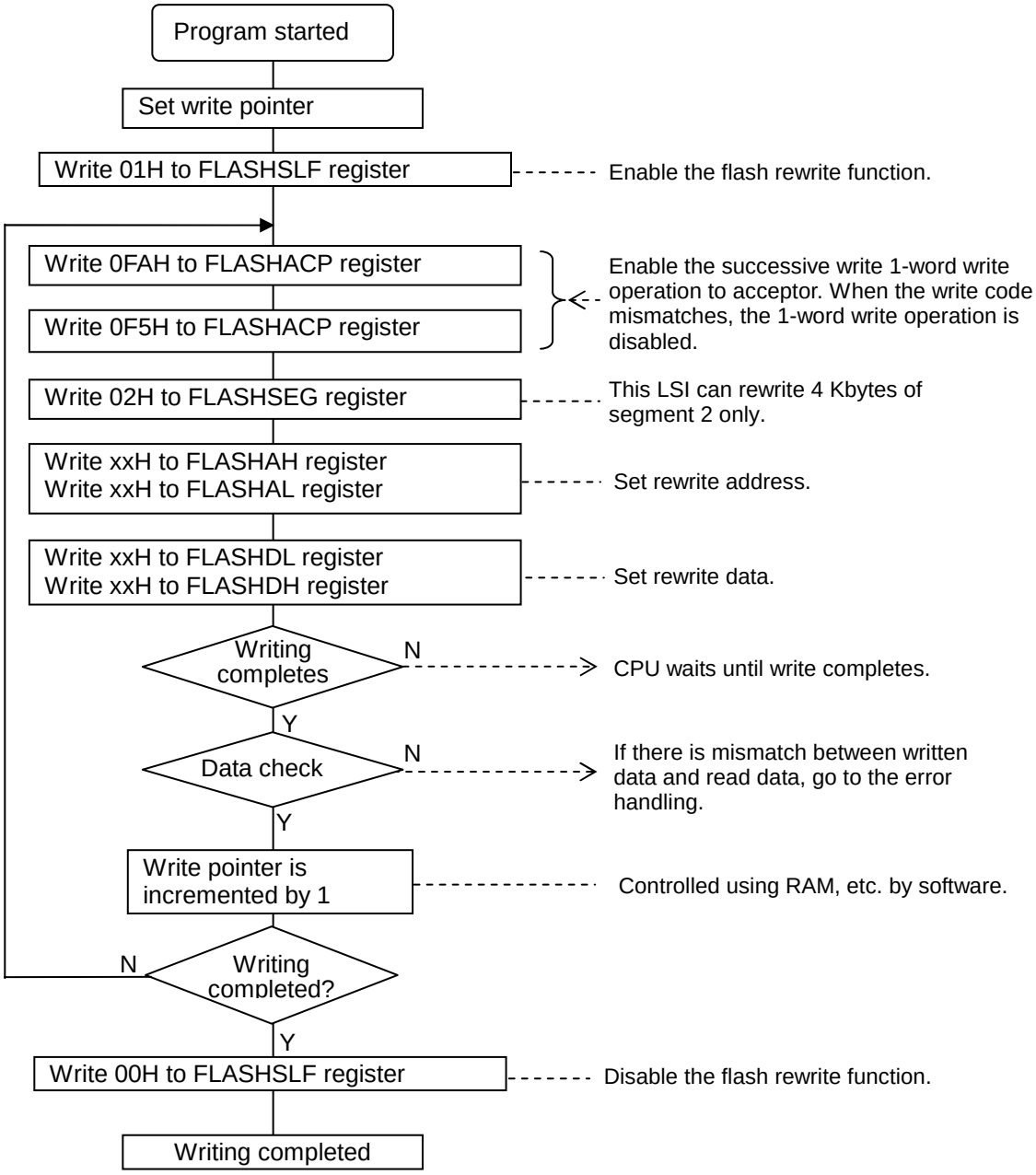


Figure 23-5 1-word Write Flow

Note:
– Clear the WDT counter of WDT as required.

– The block erase is disabled in the segment 2 0000H to 03FFH area after writing "1" to the flash protection register (FLASHPRT) FPRT0 bit.

– The block erase is disabled in the segment 2 0400H to 07FFH area after writing "1" to the flash protection register (FLASHPRT) FPRT1 bit.
– The sector erase is disabled in the segment 2 0800H to 0BFFH area after writing "1" to the flash protection register (FLASHPRT) FPRT2 bit.
– The sector erase is disabled in the segment 2 0C00H to 0FFFH area after writing "1" to the flash protection register (FLASHPRT) FPRT3 bit.

– Be sure to set the NOP instruction twice or more, following the write to FLASHDH instruction.

Figure 23-6 shows a sample program of 1-word write (assuming that the FLASHSEG register is already set).

```
            LEA     offset FLASHAL          ; EA <- FLASHAL address
            MOV     R0,     #0FAH           ; Flash acceptor enable data
            MOV     R1,     #0F5H           ; Flash acceptor enable data
            MOV     R2,     #02H            ; Address increment data
            MOV     R3,     #01H
            MOV     R4,     #(offset FLASHACP)&0FFH
            MOV     R5,     #(offset FLASHACP)>>8       ; ER4 <- FLASHACP address
;
            :
            (Set the write start address in ER8)
            (Set the write end address in ER12)
            :
            ST      R3      FLASHSLF        ; Enables the flash rewrite function
            MOV     R3,     #00H
            :
MARK:
            :
            (Set the write data in ER10)
            :
            ST      R0,     [ER4]           ; Enable flash acceptor
            ST      R1,     [ER4]           ; Enable flash acceptor
            ST      XR8,    [EA]            ; Set address and data, start 1-word write
            NOP                             ; * Always set
            NOP                             ; * Always set

;
            L       ER14,   [ER8]           ; Load data
            CMP     ER14,   ER10            ; Check data
            BNE     ERROR                   ; Go to error routine on error
;
            ADD     ER8,    ER2             ; Address increment
            CMP     ER8,    ER12
            BLE     MARK                    ; Compare addresses
;
            ST      R3,     FLASHSLF        ; Disables the flash rewrite function
;
```

Figure 23-6 Sample Program of 1-word Write

Note:
– Be sure to set the NOP instruction twice or more, following the write to FLASHDH instruction.
– Use it with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON1), and with HSCLK selected as system clock.

23.3.4 Notes in Use

When the power is down or the operation is terminated forcibly during sector erase, block erase, or 1-word write, retry the sector erase or block erase and rewrite the sector block area.

Chapter 24

On-chip Debug

24 On-Chip Debug Function

24.1 Overview

This LSI has an on-chip debug function allowing Flash memory rewriting.
The on-chip debug emulator (uEASE) is connected to this LSI to perform the on-chip debug function.

24.2 Method of Connecting to On-Chip Debug Emulator

Figure 24-1 shows the connection to the on-chip debug emulator (uEASE).
For the on-chip debug emulator, refer to the "uEASE User's Manual."

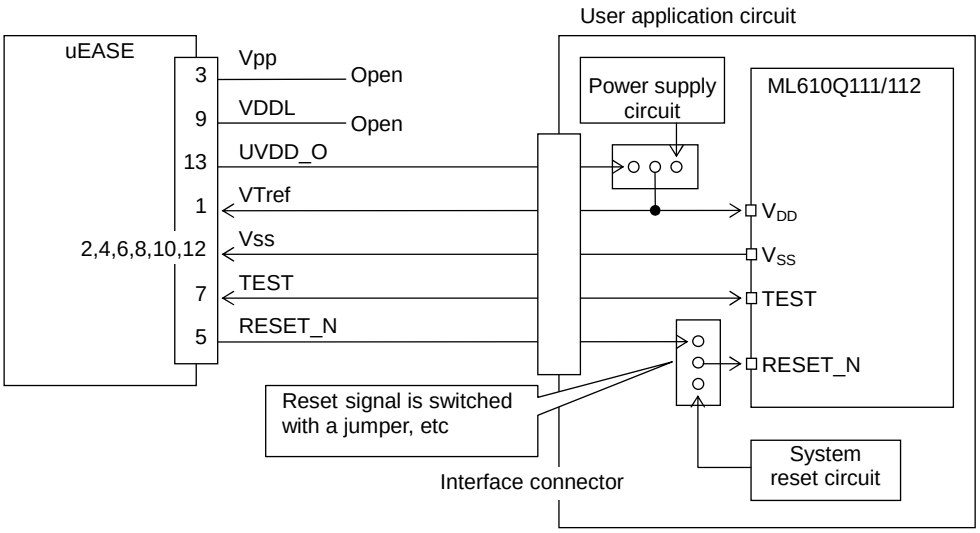


Figure 24-1 Connection to On-chip Debug Emulator (uEASE)

Note:

- Please do not apply LSIs being used for debugging to mass production.
- When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 4 pins (V_{DD}, V_{SS}, RESET_N, TEST) required for connection to the on-chip debug emulator can be connected.
- "2.7V to 5.5V" has to be supplied to V_{DD} while debugging and writing flash.
- When the system reset circuit is included in the user application circuit, enable switching of the connection in the user application circuit, as shown above. When the system reset circuit is not included in the user application circuit, the RESET_N pin can be connected directly to the RESET_N pin of this LSI.
- Please start a debugger after canceling stop mode.

For details, see "uEASE User's Manual" and "uEASE Target Connection Manual".

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	00H
0F008H	Stop code acceptor	STPACP	—	W	8	Undefined
0F009H	Standby control register	SBYCON	—	W	8	00H
0F00AH	Low-speed time base counter divide register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter divide register	HTBDR	—	R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H
0F024H	Port AB interrupt control register 0	PABICON0	—	R/W	8	00H
0F025H	Port AB interrupt control register 1	PABICON1	—	R/W	8	00H
0F026H	Port AB interrupt control register 2	PABICON2	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	—	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	—	R/W	8	00H
0F0D8H	Voltage Level Supervisor control register 0	VLSCON0	VLSCON	R/W	8/16	00H
0F0D9H	Voltage Level Supervisor control register 1	VLSCON1		R/W	8	11H
0F0DAH	Voltage Level Supervisor mode register	VLSMOD	—	R/W	8	00H
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	—	W	8	00H
0F0E5H	Flash acceptor register	FLASHACP	—	W	8	00H
0F0E6H	Flash segment register	FLASHSEG	—	R/W	8	00H
0F0E7H	Flash self register	FLASHSLF	—	R/W	8	00H
0F0E8H	Flash protect register	FLASHPRT	—	R/W	8	00H
0F0EEH	Flash erase abort source select register	FLASHEAS	—	R/W	8	00H
0F0EFH	Flash erase status register	FLASHEST	—	R/W	8	00H
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H
0F254H	Port A mode register 0	PAMOD0	PAMOD	R/W	8/16	00H
0F255H	Port A mode register 1	PAMOD1		R/W	8	00H
0F258H	Port B data register	PBD	—	R/W	8	00H
0F259H	Port B direction register	PBDIR	—	R/W	8	00H
0F25AH	Port B control register 0	PBCON0	PBCON	R/W	8/16	00H
0F25BH	Port B control register 1	PBCON1		R/W	8	00H
0F25CH	Port B mode register 0	PBMOD0	PBMOD	R/W	8/16	00H
0F25DH	Port B mode register 1	PBMOD1		R/W	8	00H
0F260H	Port C data register	PCD	—	R/W	8	00H
0F261H	Port C direction register	PCDIR	—	R/W	8	00H
0F262H	Port C control register 0	PCCON0	PCCON	R/W	8/16	00H
0F263H	Port C control register 1	PCCON1		R/W	8	00H
0F264H	Port C mode register 0	PCMOD0	PCMOD	R/W	8/16	00H
0F265H	Port C mode register 1	PCMOD1		R/W	8	00H
0F268H	Port D data register	PDD	—	R/W	8	00H
0F269H	Port D direction register	PDDIR	—	R/W	8	00H
0F26AH	Port D control register 0	PDCON0	PDCON	R/W	8/16	00H
0F26BH	Port D control register 1	PDCON1		R/W	8	00H
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	—	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F298H	UART1 transmit/receive buffer	UA1BUF	—	R/W	8	00H
0F299H	UART1 control register	UA1CON	—	R/W	8	00H
0F29AH	UART1 mode register 0	UA1MOD0	UA1MOD	R/W	8/16	00H
0F29BH	UART1 mode register 1	UA1MOD1		R/W	8	00H
0F29CH	UART1 baud rate register L	UA1BRTL	UA1BRT	R/W	8/16	0FFH
0F29DH	UART1 baud rate register H	UA1BRTH		R/W	8	0FH
0F29EH	UART1 status register	UA1STAT	—	R/W	8	00H
0F2A0H	I^2C bus 0 receive register	I2C0RD	—	R	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H
0F2A8H	I^2C bus 1 receive register	I2C1RD	—	R	8	00H
0F2A9H	I^2C bus 1 slave address register	I2C1SA	—	R/W	8	00H
0F2AAH	I^2C bus 1 transmit data register	I2C1TD	—	R/W	8	00H
0F2ABH	I^2C bus 1 control register	I2C1CON	—	R/W	8	00H
0F2ACH	I^2C bus 1 mode register	I2C1MOD	—	R/W	8	00H
0F2ADH	I^2C bus 1 status register	I2C1STAT	—	R	8	00H
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H	SADR3H		R	8	00H
0F2D8H	SA-ADC result register 4L	SADR4L	SADR4	R	8/16	00H
0F2D9H	SA-ADC result register 4H	SADR4H		R	8	00H
0F2DAH	SA-ADC result register 5L	SADR5L	SADR5	R	8/16	00H
0F2DBH	SA-ADC result register 5H	SADR5H		R	8	00H
0F2DCH	SA-ADC result register 6L	SADR6L	SADR6	R	8/16	00H
0F2DDH	SA-ADC result register 6H	SADR6H		R	8	00H
0F2DEH	SA-ADC result register 7L	SADR7L	SADR7	R	8/16	00H
0F2DFH	SA-ADC result register 7H	SADR7H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H
0F360H	Timer E data register	TMED	TMEDC	R/W	8/16	0FFH
0F361H	Timer E counter register	TMEC		R/W	8	00H
0F362H	Timer E control register 0	TMECON0	TMECON	R/W	8/16	00H
0F363H	Timer E control register 1	TMECON1		R/W	8	00H
0F364H	Timer E control register 2	TMECON2	TMECON23	R/W	8/16	00H
0F365H	Timer E control register 3	TMECON3		R/W	8	00H
0F368H	Timer F data register	TMFD	TMFDC	R/W	8/16	0FFH
0F369H	Timer F counter register	TMFC		R/W	8	00H
0F36AH	Timer F control register 0	TMFCON0	TMFCON	R/W	8/16	00H
0F36BH	Timer F control register 1	TMFCON1		R/W	8	00H
0F36CH	Timer F control register 2	TMFCON2	TMFCON23	R/W	8/16	00H
0F36DH	Timer F control register 3	TMFCON3		R/W	8	00H
0F8E0H	Timer 8 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 8 counter register	TM8C		R/W	8	00H
0F8E2H	Timer 8 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 8 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 9 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 9 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 9 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 9 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer A data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer A counter register	TMAC		R/W	8	00H
0F8EAH	Timer A control register 0	TMACON0	TMACON	R/W	8/16	00H
0F8EBH	Timer A control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer B data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer B counter register	TMBC		R/W	8	00H
0F8EEH	Timer B control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer B control register 1	TMBCON1		R/W	8	00H
0F910H	PWMC period register L	PWCPL	PWCP	R/W	8/16	0FFH
0F911H	PWMC period register H	PWCPH		R/W	8	0FFH
0F912H	PWMC duty register L	PWCDL	PWCD	R/W	8/16	00H
0F913H	PWMC duty register H	PWCDH		R/W	8	00H
0F914H	PWMC counter register L	PWCCL	PWCC	R/W	8/16	00H
0F915H	PWMC counter register H	PWCCH		R/W	8	00H
0F916H	PWMC control register 0	PWCCON0	PWCCON	R/W	8/16	00H
0F917H	PWMC control register 1	PWCCON1		R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F918H	PWMC control register 2	PWCCON2	PWCCON23	R/W	8/16	00H
0F919H	PWMC control register 3	PWCCON3		R/W	8	00H
0F920H	PWMD period register L	PWDPL	PWDP	R/W	8/16	0FFH
0F921H	PWMD period register H	PWDPH		R/W	8	0FFH
0F922H	PWMD duty register L	PWDDL	PWDD	R/W	8/16	00H
0F923H	PWMD duty register H	PWDDH		R/W	8	00H
0F924H	PWMD counter register L	PWDCL	PWDC	R/W	8/16	00H
0F925H	PWMD counter register H	PWDCH		R/W	8	00H
0F926H	PWMD control register 0	PWDCON0	PWDCON	R/W	8/16	00H
0F927H	PWMD control register 1	PWDCON1		R/W	8	00H
0F928H	PWMD control register 2	PWDCON2	PWDCON23	R/W	8/16	00H
0F929H	PWMD control register 3	PWDCON3		R/W	8	00H
0F930H	PWME period register L	PWEPL	PWEP	R/W	8/16	0FFH
0F931H	PWME period register H	PWEPH		R/W	8	0FFH
0F932H	PWME duty register L	PWEDL	PWED	R/W	8/16	00H
0F933H	PWME duty register H	PWEDH		R/W	8	00H
0F934H	PWME counter register L	PWECL	PWEC	R/W	8/16	00H
0F935H	PWME counter register H	PWECH		R/W	8	00H
0F936H	PWME control register 0	PWECON0	PWECON	R/W	8/16	00H
0F937H	PWME control register 1	PWECON1		R/W	8	00H
0F938H	PWME control register 2	PWECON2	PWECON23	R/W	8/16	00H
0F939H	PWME control register 3	PWECON3		R/W	8	00H
0F950H	Comparator 0 control register 0	CMP0CON0	—	R/W	8	00H
0F951H	Comparator 0 control register 1	CMP0CON1	—	R/W	8	00H
0F952H	Comparator 0 control register 2	CMP0CON2	—	R/W	8	08H
0F954H	Comparator 1 control register 0	CMP1CON0	—	R/W	8	00H
0F955H	Comparator 1 control register 1	CMP1CON1	—	R/W	8	00H
0F956H	Comparator 1 control register 2	CMP1CON2	—	R/W	8	08H
0F960H	PWMF period register L	PWFPL	PWFP	R/W	8/16	0FFH
0F961H	PWMF period register H	PWFPH		R/W	8	0FFH
0F962H	PWMF0 duty register L	PWF0DL	PWF0D	R/W	8/16	00H
0F963H	PWMF0 duty register H	PWF0DH		R/W	8	00H
0F964H	PWMF1 duty register L	PWF1DL	PWF1D	R/W	8/16	00H
0F965H	PWMF1 duty register H	PWF1DH		R/W	8	00H
0F966H	PWMF2 duty register L	PWF2DL	PWF2D	R/W	8/16	00H
0F967H	PWMF2 duty register H	PWF2DH		R/W	8	00H
0F970H	PWMF counter register L	PWFCL	PWFC	R/W	8/16	00H
0F971H	PWMF counter register H	PWFCH		R/W	8	00H
0F972H	PWMF control register 0	PWFCON0	PWFCON	R/W	8/16	00H
0F973H	PWMF control register 1	PWFCON1		R/W	8	00H
0F974H	PWMF control register 2	PWFCON2	PWFCON23	R/W	8/16	00H
0F975H	PWMF control register 3	PWFCON3		R/W	8	00H
0F976H	PWMF control register 4	PWFCON4	PWFCON45	R/W	8/16	10H
0F977H	PWMF control register 5	PWFCON5		R/W	8	00H

Appendix B Package Dimensions

● ML610Q111

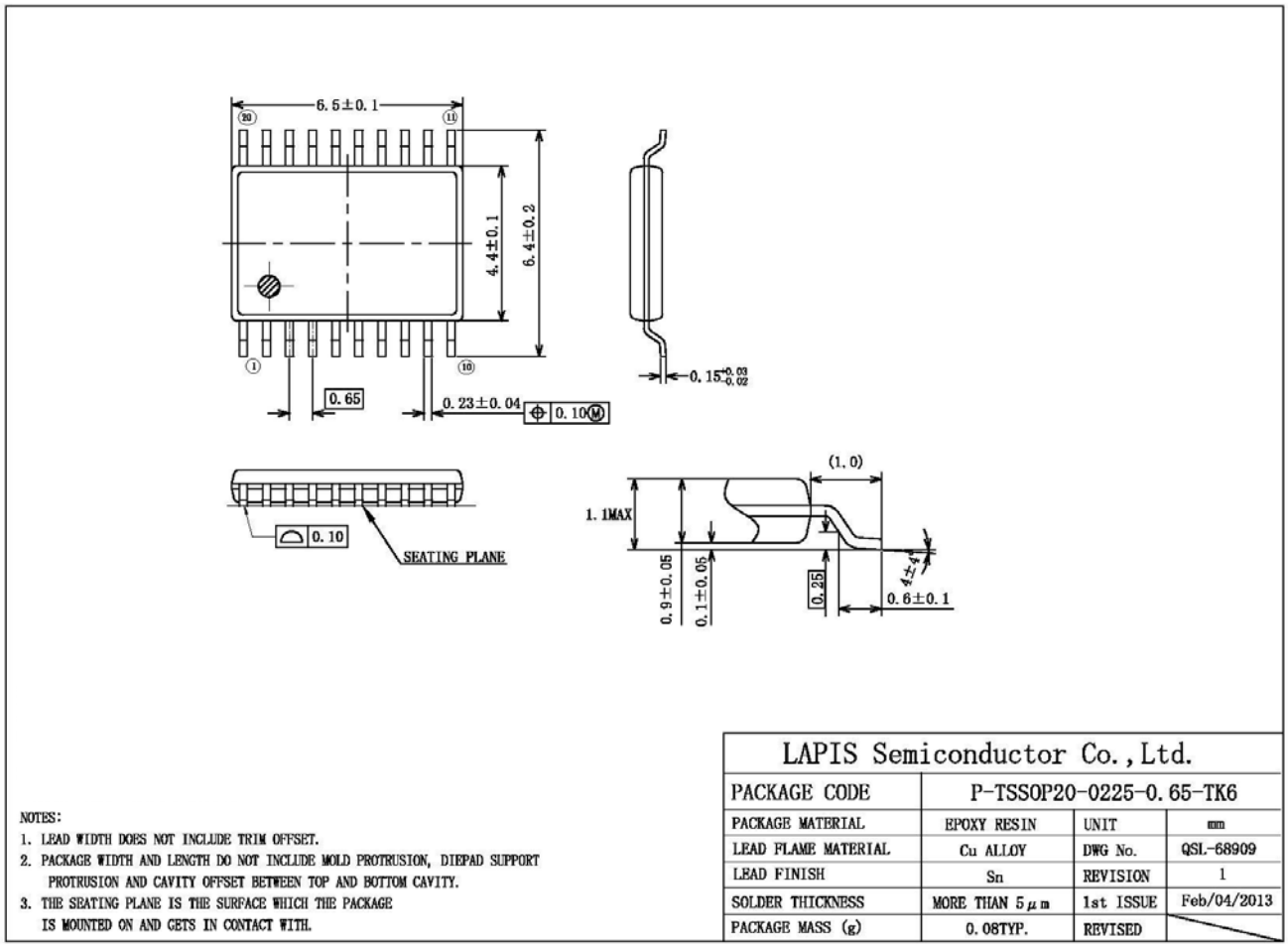
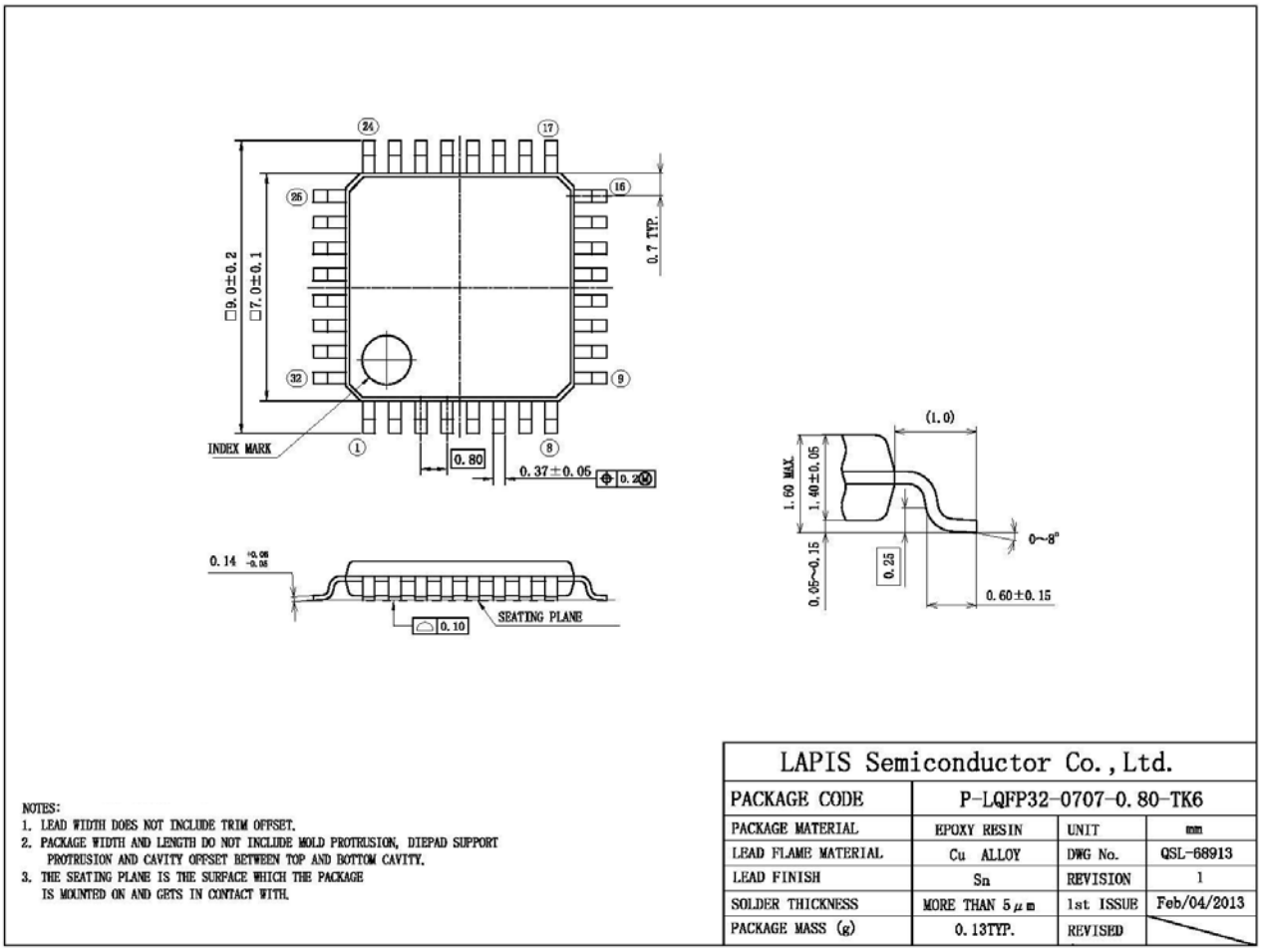


Figure B-1 TSSOP20

● ML610Q112



FigureB-2 LQFP32

● Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C Electrical Characteristics

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current	I_{OUT}	Ta = 25°C	–12 to +11	mA
Power dissipation	PD	Ta = 25°C	0.84	W
Storage temperature	T_{STG}	—	-55 to 150	°C

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Operating temperature (ambience)	T_{OP}	—	–40 to +105	°C
Operating voltage	V_{DD}	—	2.7 to 5.5	V

● Flash Memory Specification

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature (ambience)	T_{OPF}	At read		-40 to +105	°C
		At write/erase		-20 to +85	°C
Rewrite counts *1	C_{EPD}	Data area(4KB)		6000	cycles
	C_{EPP}	Program area		80	
Erase unit	—	Chip erase		All of the program and data area	—
	—	Block erase	Program area	8	KB
			Data area	4	KB
	—	Sector erase (effective only data area)		1	KB
Erase time (Maximum)	—	Chip erase/ Block erase/ Sector erase		100	ms
Write unit	—	—		1 word (2 byte)	—
Write time (Maximum)	—	1 word (2 byte)		40	us
Data retention*2	Y_{DR}	—		15	year

*1 : Rewrite counts is counted as one even if you erase suspend.

*2 : However, keep active of the flash memory from exceeding 10 years.

● DC Characteristics (1/4)

(VDD=2.7 to 5.5V, VSS=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Supply current 1	IDD1	CPU : In STOP state (All clock stop) V_{DD}=5.0V	—	1	50	μA	1
Supply current 2	IDD2	CPU : In HALT state*1 (Only CR oscillation operates) V_{DD}=5.0V	—	240	—	μA	
Supply current 3	IDD3	CPU : CR 32.768kHz operating state*2 (Only CR oscillation operates) V_{DD}=5.0V	—	250	—	μA	
Supply current 4	IDD4	CPU : PLL 8.192MHz operating state*3 (CR and PLL oscillation operate) V_{DD}=5.0V	—	4	6	mA	

*1 : LTBC and WDT are operating ,and significant bits of BLKCON0 to BLKCON7 registers are all "1".

*2 : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 30.52 μs (at 32.768kHz system clock)

*3 : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 122 ns (at 8.192MHz system clock)

● DC Characteristics (2/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=−40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
VLS0 threshold voltage (V_{DD}=fall)	V_{VLS0F}	Ta=25°C		Typ. −3.0%	2.85	Typ. +3.0%	V	1
		—		Typ. −5.0%		Typ. +5.0%		
VLS0 threshold voltage (V_{DD}=rise)	V_{VLS0R}	Ta=25°C		Typ. −3.0%	2.92	Typ. +3.0%		
		—		Typ. −5.0%		Typ. +5.0%		
VLS1 threshold voltage (V_{DD}=fall)	V_{VLS1}	Ta=25°C	VLS1=0	Typ. −3.0%	3.3	Typ. +3.0%		
			VLS1=1		3.6			
			VLS1=2		3.9			
			VLS1=3		4.2			
		—	VLS1=0	Typ. -5.0%	3.3	Typ. +5.0%		
			VLS1=1		3.6			
			VLS1=2		3.9			
			VLS1=3		4.2			
Comparator 0 In-phase input voltage range	V_{CMR}	—		0.1	—	V_{DD} -1.5	V	
Comparator 0 hysteresis	V_{HYSP}	Ta=25°C , V_{DD} = 5.0V		10	20	30	mV	
		V_{DD} = 5.0V		5	20	35		
Comparator 0 Input offset voltage	V_{CMOF}	Ta=25°C , V_{DD} = 5.0V		—	—	7		
Comparator Reference-voltage error*1	V_{CMREF}	Ta=25°C		-25	—	25		
		—		-50	—	50		

*1 :Comparator input offset voltage is included.

● DC Characteristics (3/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (TEST, PA0-2, PB0-7, PC0-7, PD0-5)	VOH1	IOH = –3.0mA, V_{DD} = 4.5V *1 Ta=-40 to 85°C	V_{DD} –0.7	—	—	V	2
		IOH = –3.0mA, V_{DD} = 4.5V *1	V_{DD} –0.8	—	—		
	VOL1	IOL = +8.5mA, V_{DD} = 4.5V *1 Ta=-40 to 85°C	—	—	0.6		
		IOL = +8.5mA, V_{DD} = 4.5V *1	—	—	0.7		
Output voltage 2 (PB5,PB6, PC4,PC5)	VOL2	IOL = +3.0mA	—	—	0.4		
Output leakage (PA0-2, PB0-7, PC0-7, PD0-5)	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	—	—	1	µA	4
	IIL1	VIL1 = V_{SS}, V_{DD} = 5.0V	–650	–500	–350		
Input current 2 (TEST)	IIH2	VIH2= V_{DD} = 5.0V	20	115	200		
	IIL2	VIL2 = V_{SS}	–1	—	—		
Input current 3 (PA0-2, PB0-7, PC0-7, PD0-5)	IIH3	VIH3 = V_{DD} = 5.0V (when pulled-down)	20	115	200		
	IIL3	VIL3 = V_{SS}, V_{DD} = 5.0V (when pulled-up)	–200	–100	–20		
	IIH3Z	VIH3 = V_{DD} (in high-impedance stat)	—	—	1		
	IIL3Z	VIH3 = V_{SS} (in high-impedance stat)	-1	—	—		

*1 : When the one terminal output state.

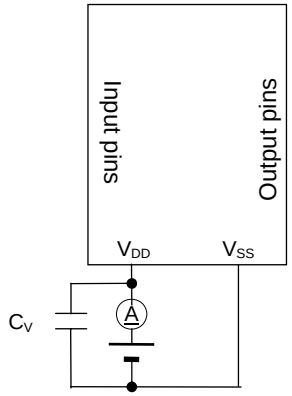
● DC Characteristics (4/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, TEST, PA0-2, PB0-7, PC0-7, PD0-5)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	2
	VIL1	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (PA0-2, PB0-7, PC0-7, PD0-5)	CIN	f = 10kHz Ta = 25°C	—	—	20	pF	—

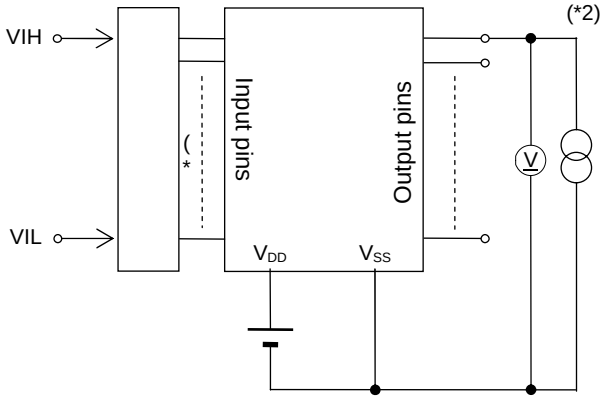
● Measuring circuit

Measuring circuit 1

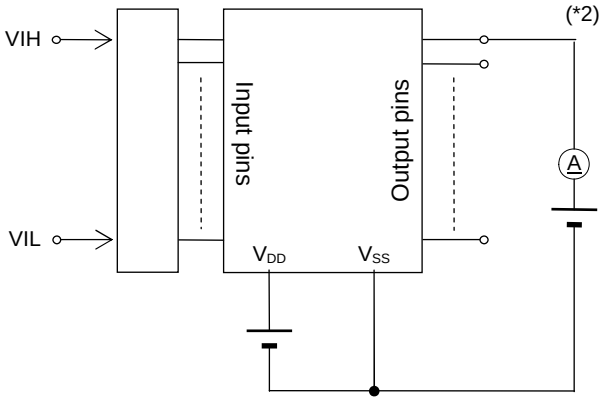


C_V : 1µF

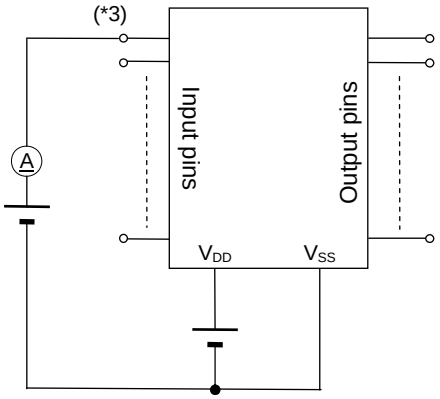
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.
*3: Measured at the specified input pins.

● AC Characteristics (Clock)

(VDD=2.7 to 5.5V, VSS=0V, Ta=–40 to +105°C, unless otherwise specified)

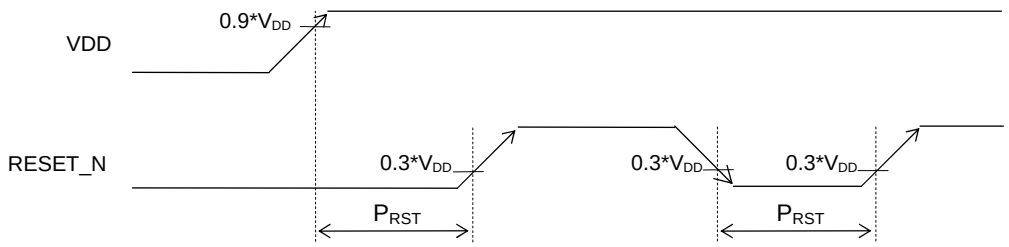
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
32kHz RC oscillation frequency	f_{RCL}	Ta = -20°C to 85°C	Typ. -3%	32.768	Typ. +3%	kHz
		—	Typ. -4%		Typ. +4%	
PLL oscillation frequency*1	f_{PLL}	Ta = -20°C to 85°C	Typ. -3%	16.384	Typ. +3%	MHz
		—	Typ. -4%		Typ. +4%	

*1 : Average value of 1024 clocks. The CPU clock is set to the maximum f_{PLL} / 2.

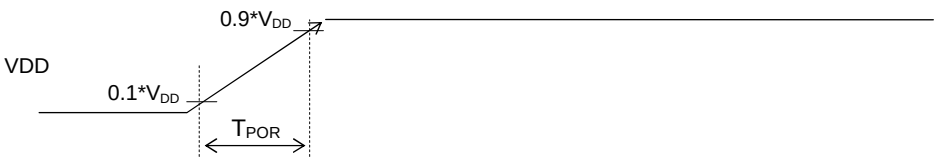
● AC Characteristics (Power on / Reset sequence)

(VDD=2.7 to 5.5V, VSS=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Reset pulse width	P_{RST}	—	100	—	—	µs
Reset noise elimination pulse width	P_{NRST}	—	—	—	0.4	
Power-on reset activation power rise time	T_{POR}	—	—	—	10	ms



External Reset sequence

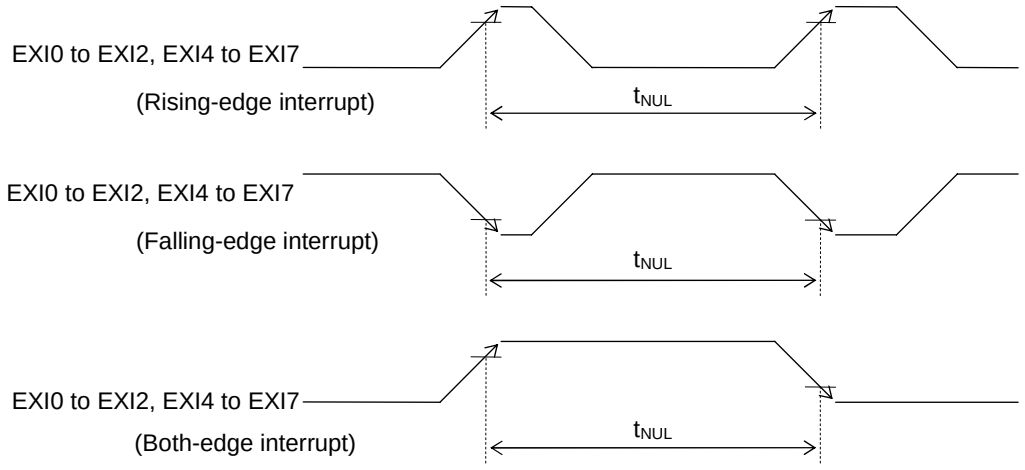


Power-on Reset sequence

● AC Characteristics (External Interrupt)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	t_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5 X sysclk	—	3.5 X sysclk	ϕ

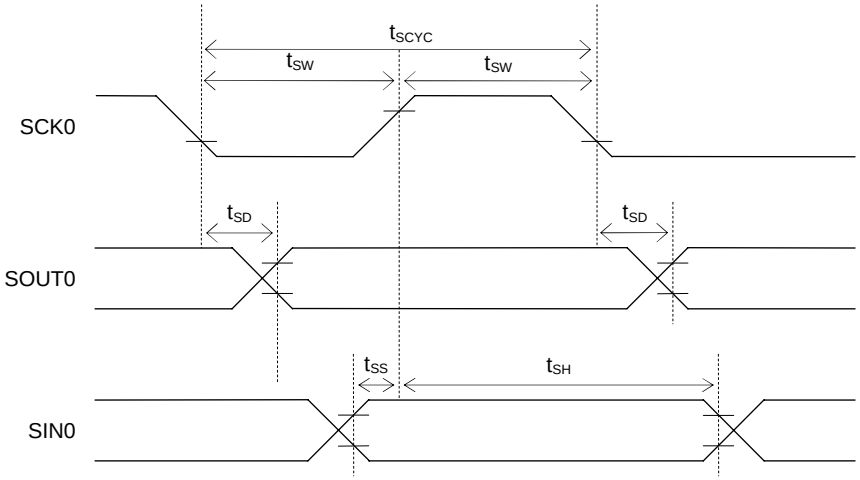


● AC Characteristics (Synchronous Serial Port)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
		When high-speed oscillation is active	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK*1	—	ns
SCK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
		When high-speed oscillation is active	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected with S0CK3-0 of the serial port 0 mode register (SIO0MOD1)



● AC Characteristics (I2C Bus Interface: Standard Mode 100kHz)

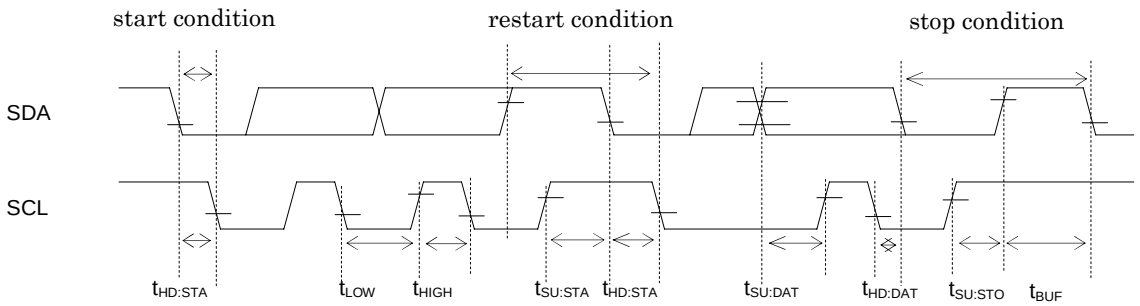
(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

● AC Characteristics (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

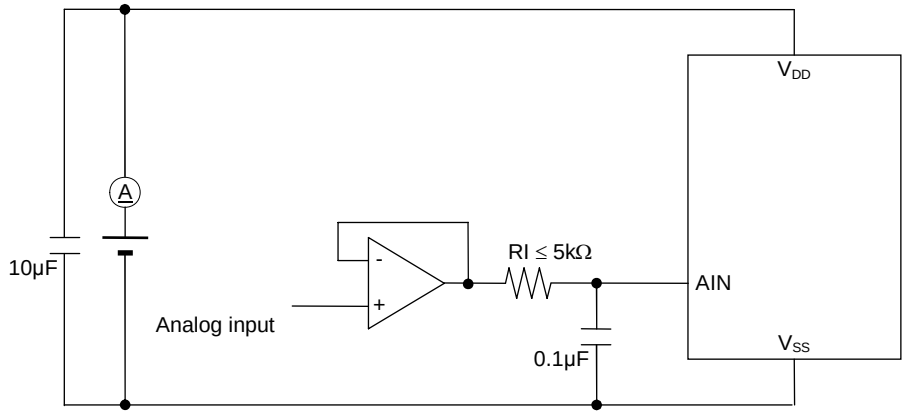


● Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	10	bit
Integral non-linearity error	INL	—	–4	—	+4	LSB
Differential non-linearity error	DNL	—	–3	—	+3	
Zero-scale error	V_{OFF}	—	–4	—	+4	
Full-scale error	FSE	—	–4	—	+4	
Conversion time	t_{CONV}	—	—	102	—	ϕ/CH

ϕ: Period of OSCLK (more than 3MHz)



Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL610Q111-01	Oct. 01, 2013	–	–	Final edition 1
FEUL610Q111-02	Feb. 07, 2014	9-4	9-4	Add note to WDTMOD register.
		10-26	10-26	Corrected a description of PWMF Period register.
		10-42	10-42	Corrected a description of Figure 10-7. Identifying PWM Interrupt.
		C-2,3	C-2,3	Corrected temperature range of DC-Characteristics.