DATASHEET

General Description

The XUN is an Ultra Precision HCSL Crystal Oscillator with 300fs typical phase jitter over 12kHz to 20 MHz bandwidth. Available in a wide frequency range from 16kHz to 670MHz, the IDT XUN Series Crystal Oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 4th order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XUN is an excellent choice over the conventional technologies. The XUN has stabilities as tight as ±20ppm with extremely quick delivery for both standard and custom frequencies

Features

- Frequency range: 0.016MHz to 670MHz
- Output Type: HCSL
- Frequency Stability: ± 20ppm, ± 25ppm, ± 50ppm, or ± 100 ppm
- Supply Voltage: 1.8V, 2.5V, or 3.3V
- Phase Jitter (1.875MHz to 20MHz): 100fs typical
- Phase Jitter (12kHz to 20MHz): 300fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6) 7.0mm x 5.0mm x 1.3mm (JU6)
- Operating Temperatures: -20°C to +70°C or -40°C to +85°C

Pin Assignment



6-pin CLCC

Pin Descriptions

Pin Number	Pin Name	Description		
1	E/D	Enable/Disable ¹ (0=Output Disabled)		
2	NC	No connect		
3	GND	Connect to ground		
4	OUT	Output		
5	OUT2	Complementary output		
6	VDD	Supply Voltage		

1. Pulled high internally.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XUN. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0 V
E/D	-0.5 V to VDD + 0.5 V
OUT	-0.5 V to VDD + 0.5 V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

ESD Compliance

Human Body Model (HBM	1000V
Machine Model (MM)	150V

Mechanical Testing

Parameter	Test Method
Mechanical Shock	Half-Sine wave with 0.3ms 3000G X, Y, Z each direction 1 time
Mechanical Vibration	Frequency: 10 to 55 MHz Amplitude: 1.5mm Frequency: 55~2000Hz Peak value: 20G Duration time: 4H for each X,Y,Z axis Total 12 hours
High Temp Operating Life (HTOL)	2000 Hours, 125°C (under power)
Hermetic Seal	Gross leak (Air leak test) Fine leak (Helium leak test) He-pressure: 6kgf/cm² 2 hours

Solder Reflow Profile



DC Characteristics

(V_{DD} = 3.3 V ± 5%, T_A = - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Power Supply Current	I _{DD}	Standard frequencies			145	mA
Output HIGH Voltage	V _{OH}	Std HCSL load	0.6		1.1	V
Output LOW Voltage	V _{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V _{IH}		70%V _{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V _{IL}				30%V _{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

(V_{DD} = 3.3 V ± 5%, T_A = - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Output Frequency Range	F _{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Aging (1 st year)		Ta = 25°C			±3	
Aging (10 years)		Ta = 25°C			±10	
Output Load		To GND		50		Ohms
Start-up Time	T _{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V _{PP} (Standard frequencies			330	ps
Output Fall Time		80% to 20% V _{PP} (Standard frequencies)			330	ps
Output Clock Duty Cycle	T _{DTCY}	@ 50% V _{PP}	45		55	%
Output Enable/ Disable Time	T _{OE}				100	ns
Period Jitter, RMS	J _{PER}	Frequency = 156.25MHz		7	10	psec
Random Jitter	RJ	Frequency = 156.25MHz		0.6	0.7	psec
Deterministic Jitter	DJ	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		10	22	psec
Total Jitter	TJ			19	31	psec
Phase Jitter (12kHz – 20MHz)	ф _{JITTER}	Standard frequencies		300	400	fsec
Phase Noise Performance	φ _{NOISE}	100Hz of Carrier		-90		dBc/Hz
Frequency = 156.25MHz		1kHz of Carrier		-113		dBc/Hz
		10kHz of Carrier		-121		dBc/Hz
		100kHz of Carrier		-129		dBc/Hz
		1MHz of Carrier		-147		dBc/Hz
		10MHz of Carrier		-156		dBc/Hz
Output Frequency (Standards)	F _{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 15 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)	55.52MHz, 7	156.25MHz,	200MHz, 2	212,5MHz,

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

DC Characteristics

(V_{DD} = 2.5 V ± 5%, T_A = - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Power Supply Current	I _{DD}	Standard frequencies			102	mA
Output HIGH Voltage	V _{OH}	Std HCSL load	0.55		0.95	V
Output LOW Voltage	V _{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V _{IH}		70%V _{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V _{IL}				30%V _{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

(V_{DD}= 2.5 V ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Мах	Units
Output Frequency Range	F _{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Output Load		To GND		50		Ohms
Start-up Time	T _{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V _{PP} (Standard frequencies)			315	ps
Output Fall Time		80% to 20% V _{PP} (Standard frequencies)			315	ps
Output Clock Duty Cycle	T _{DTCY}	@ 50% V _{PP}	45		55	%
Output Enable/ Disable Time	T _{OE}				100	ns
Period Jitter, RMS	J _{PER}	Frequency = 156.25MHz		7	10	psec
Random Jitter	RJ	Frequency = 156.25MHz		0.7	1	psec
Deterministic Jitter	DJ	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		10	20	psec
Total Jitter	TJ			20	31	psec
Phase Jitter (12kHz – 20MHz)	φ _{JITTER}	Standard frequencies		350	500	fsec
Phase Noise Performance	φ _{NOISE}	100Hz of Carrier		-95		dBc/Hz
Frequency = 156.25MHz		1kHz of Carrier		-1113		dBc/Hz
		10kHz of Carrier		-123		dBc/Hz
		100kHz of Carrier		-129		dBc/Hz
		1MHz of Carrier		-147		dBc/Hz
		10MHz of Carrier		-153		dBc/Hz
Output Frequency (Standards)	F _{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212,5 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)				2,5MHz,

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

DC Characteristics

(V_{DD} = 1.8 V ± 5%, T_A = - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Power Supply Current	I _{DD}	Standard frequencies			68	mA
Output HIGH Voltage V _{OH}		Std HCSL load	0.45		0.7	V
Output LOW Voltage	V _{OL}	Std HCSL load	0		0.2	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V _{IH}		70%V _{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V _{IL}				30%V _{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

(V_{DD}= 1.8 V ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Output Frequency Range	F _{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Output Load		To GND		50		Ohms
Start-up Time	T _{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V _{PP} (Standard frequencies)			320	ps
Output Fall Time		80% to 20% V _{PP} (Standard frequencies)			320	ps
Output Clock Duty Cycle	T _{DTCY}	@ 50% V _{PP}	40		60	%
Output Enable/ Disable Time	T _{OE}				100	ns
Period Jitter, RMS	J _{PER}	Frequency = 156.25MHz		7	10	psec
Random Jitter	RJ	Frequency = 156.25MHz		0.85	1.2	psec
Deterministic Jitter	DJ	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		10	22	psec
Total Jitter	TJ			20	35	psec
Phase Jitter (12kHz – 20MHz)	ф _{JITTER}	Standard frequencies		1	1.2	psec
Phase Noise Performance	φ _{NOISE}	100Hz of Carrier		-84		dBc/Hz
Frequency = 156.25MHz		1kHz of Carrier		-105		dBc/Hz
		10kHz of Carrier		-111		dBc/Hz
		100kHz of Carrier		-121		dBc/Hz
		1MHz of Carrier		-144		dBc/Hz
		10MHz of Carrier		-148		dBc/Hz
Output Frequency (Standards)	F _{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 15 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)	5.52MHz, 1	56.25MHz,	200MHz, 2	12,5MHz,

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices



Period

Typical Phase Noise (3.3V)

1/2 Period



JS6 Package Outline and Dimensions



JS6 Package Outline and Dimensions (cont.)



JU6 Package Outline and Dimensions



() IDT

JU6 Package Outline and Dimensions (cont.)





IDT Ordering Information Scheme #1 (for reference only)

The *IDT Ordering Information Scheme #1* table above is to be used for reference only. IDT is updating the orderable part number for this device family to support frequency accuracy and ordering down to the 1Hz level. Please see the *IDT Ordering Information Scheme #2* table on the following page for the latest ordering information.

IDT Ordering Information Scheme #2



Revision History

Rev.	Date	Originator	Description of Change
A	10/01/14	B. Chandhoke	1. Corrected typo in spec for Enable/Disable Low Voltage; from \geq 30%VDD to \leq 30%VDD. 2. Moved from Advance to Preliminary.
В	12/15/14	B. Chandhoke	 Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings. Updates to all DC char tables. Updates to all AC char tables. Updated ordering information table/graphic to show JU6 package option
С	10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.



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