STB7N52K3, STD7N52K3
STF7N52K3, STP7N52K3

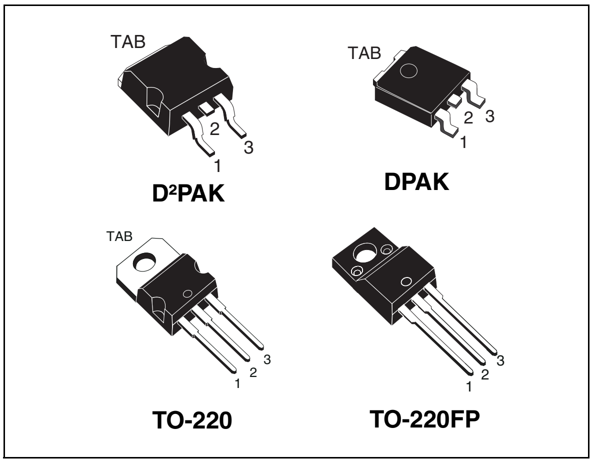
N-channel 525 V, 0.72 Ω, 6 A SuperMESH3™ Power MOSFET in D²PAK, DPAK, TO-220FP and TO-220 packages

Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D	Pw
STB7N52K3	525 V	< 0.85 Ω	6 A	90 W
STD7N52K3				90 W
STF7N52K3				25 W
STP7N52K3				90 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected



Application

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Figure 1. Internal schematic diagram

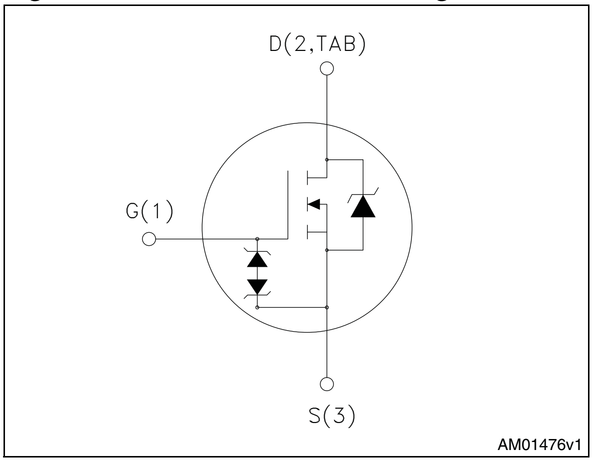


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB7N52K3	7N52K3	D²PAK	Tape and reel
STD7N52K3		DPAK	
STF7N52K3		TO-220FP	Tube
STP7N52K3		TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	DPAK	D²PAK	TO-220FP	
V_{GS}	Gate- source voltage	± 30				V
I_D	Drain current (continuous) at T_C = 25 °C	6			6 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.8			3.8 (1)	A
I_{DM} (2)	Drain current (pulsed)	24			24 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90			25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3				A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	100				mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 kΩ)	2500				V
dv/dt (3)	Peak diode recovery voltage slope	12				V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)				2500	V
T_{stg}	Storage temperature	- 55 to 150				°C
T_j	Max. operating junction temperature	150				°C

1. Limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 6 A, di/dt = 400 V, peak $V_{DS} < V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	DPAK	D²PAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.39			5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max		50	30		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5			62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300			300	°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3 A		0.72	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	870 70 13	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	53	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 420 V, I_D = 6 A, V_{GS} = 10 V (see *Figure 20*)	-	33 6 21	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 260 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19*)	-	13 11 36 19	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		6 24	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 24*)	-	220 1800 16		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 24*)	-	250 2200 18		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-		V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

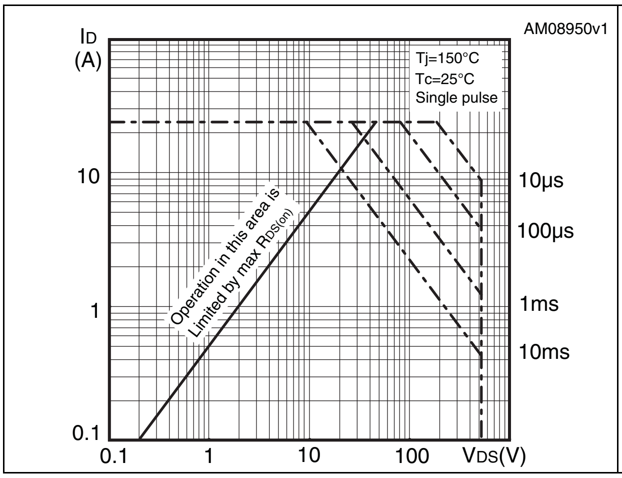


Figure 3. Thermal impedance for TO-220, D²PAK

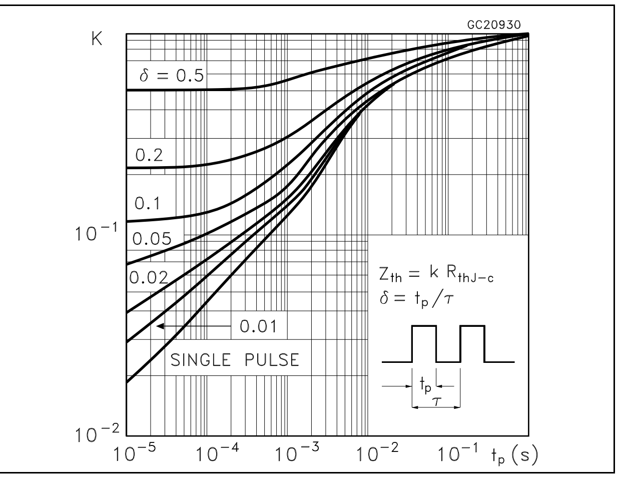


Figure 4. Safe operating area for DPAK

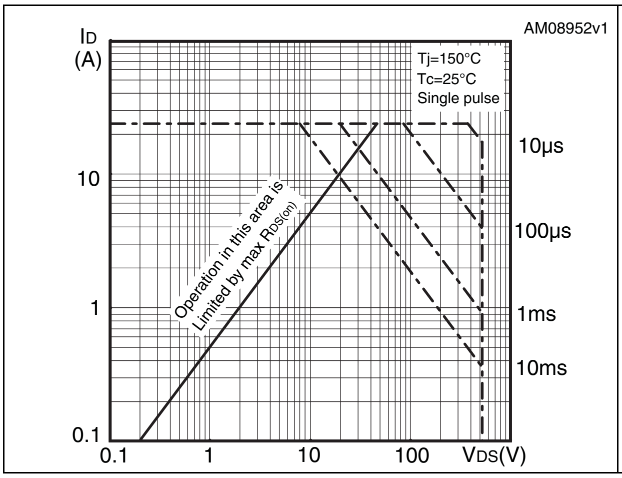


Figure 5. Thermal impedance for DPAK

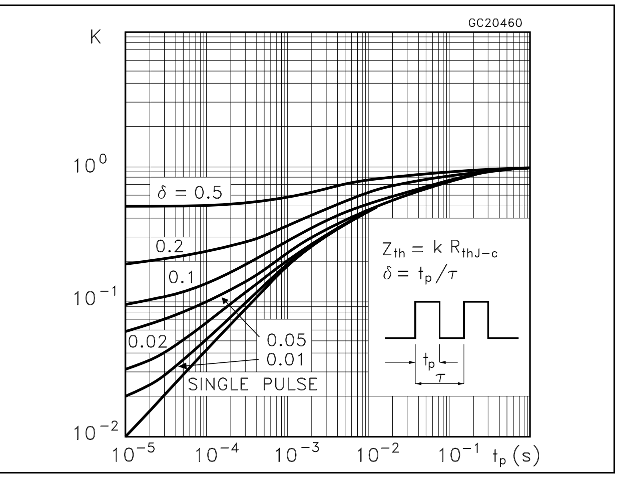


Figure 6. Safe operating area for TO-220FP

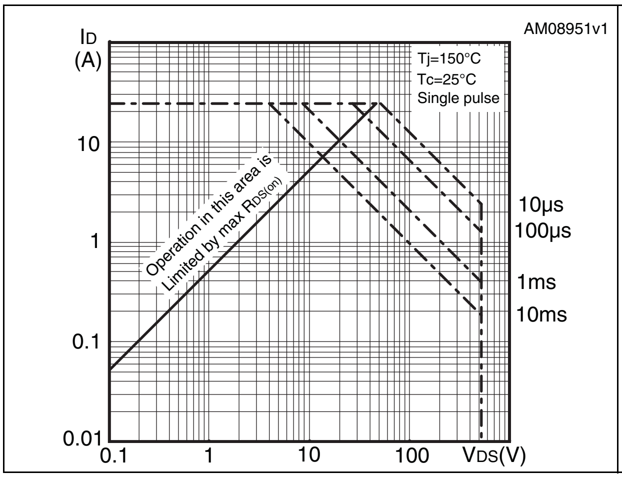


Figure 7. Thermal impedance for TO-220FP

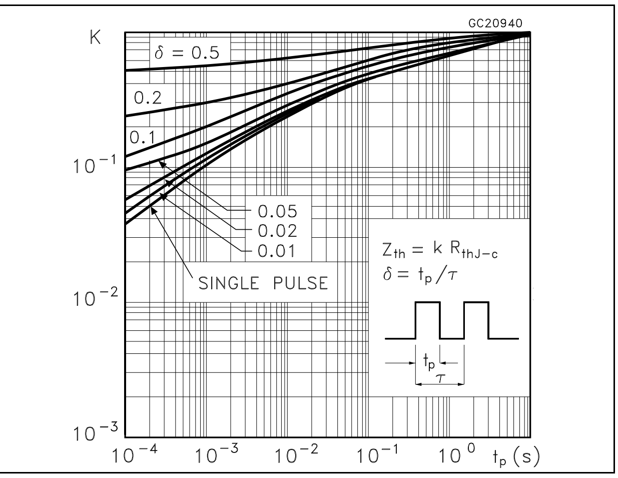


Figure 8. Output characteristics

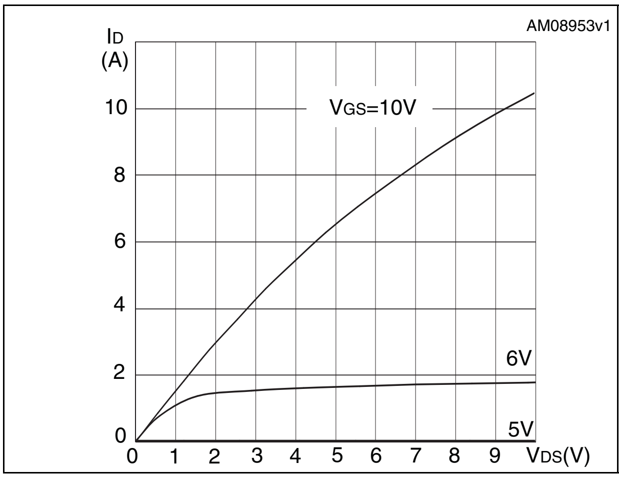


Figure 9. Transfer characteristics

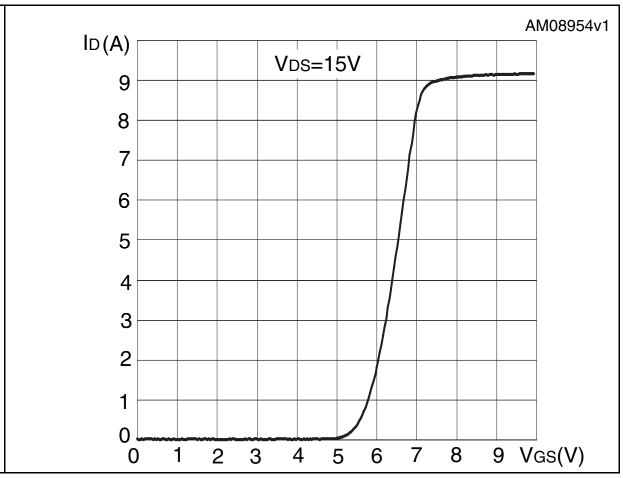


Figure 10. Normalized BV_{DSS} vs temperature

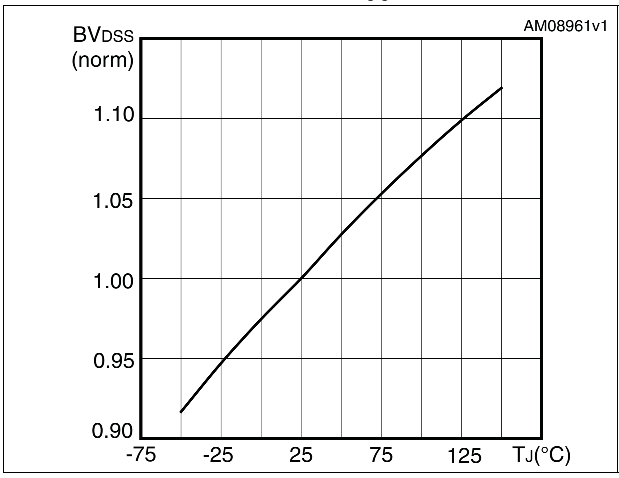


Figure 11. Static drain-source on resistance

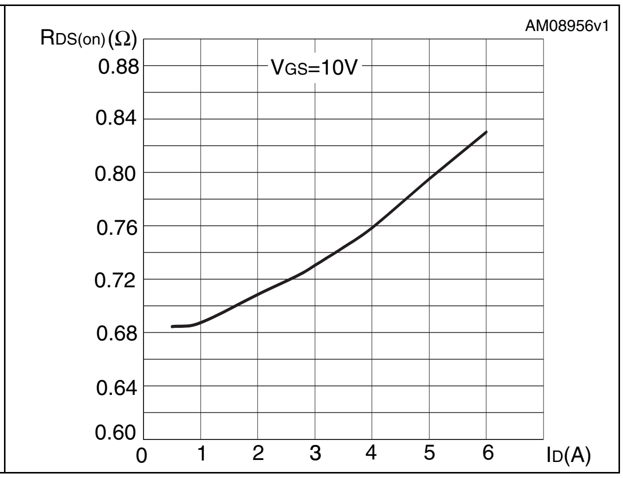


Figure 12. Output capacitance stored energy

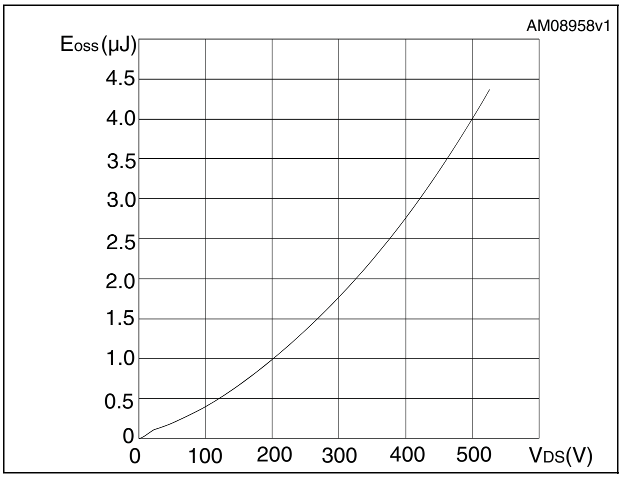


Figure 13. Capacitance variations

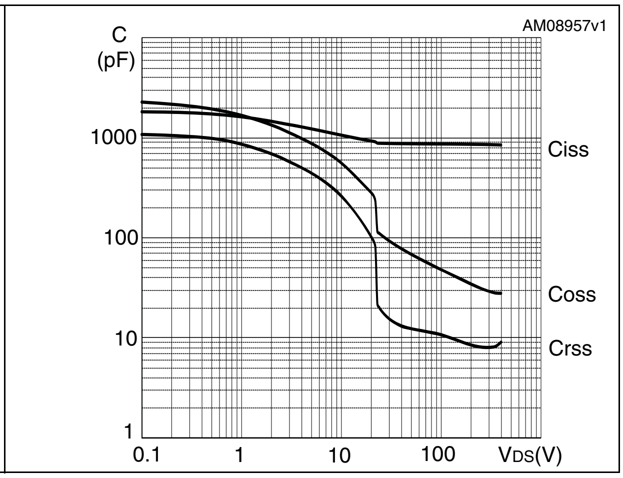


Figure 14. Gate charge vs gate-source voltage

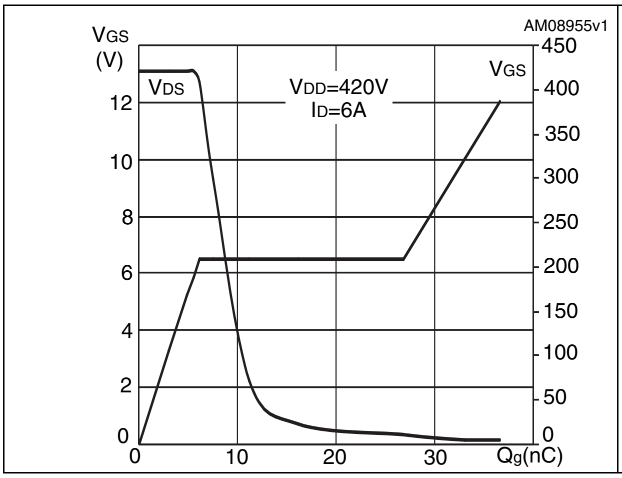


Figure 15. Normalized on resistance vs temperature

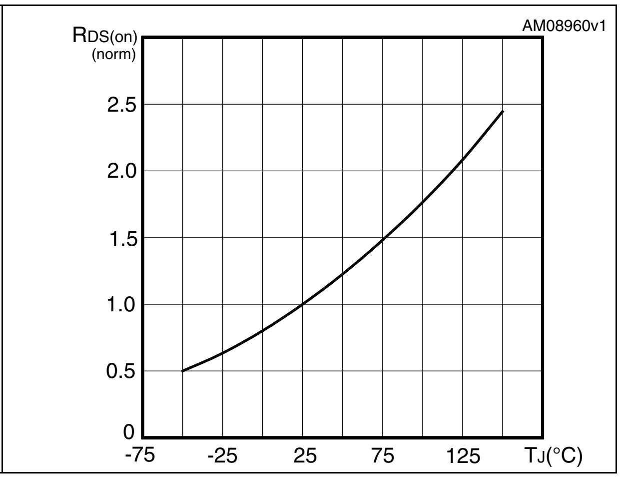


Figure 16. Normalized gate threshold voltage vs temperature

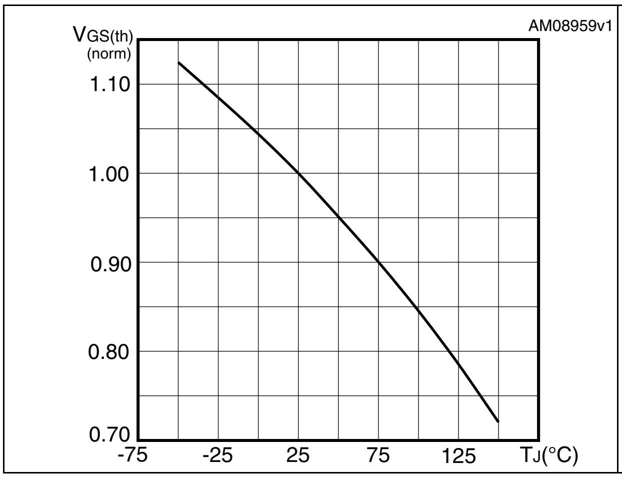


Figure 17. Maximum avalanche energy vs temperature

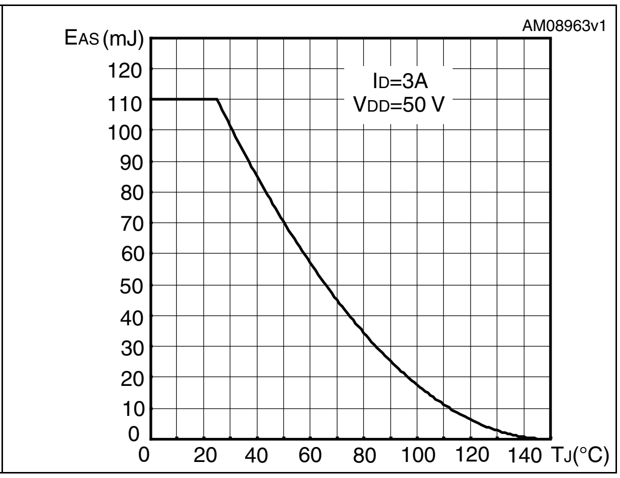
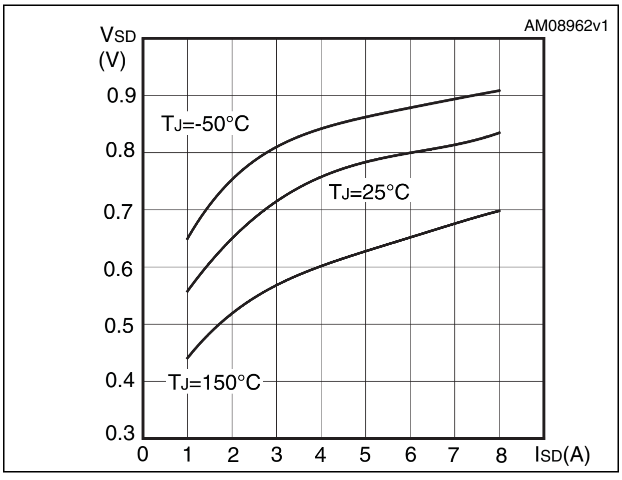


Figure 18. Source-drain diode forward characteristics



3 Test circuits

Figure 19. Switching times test circuit for resistive load

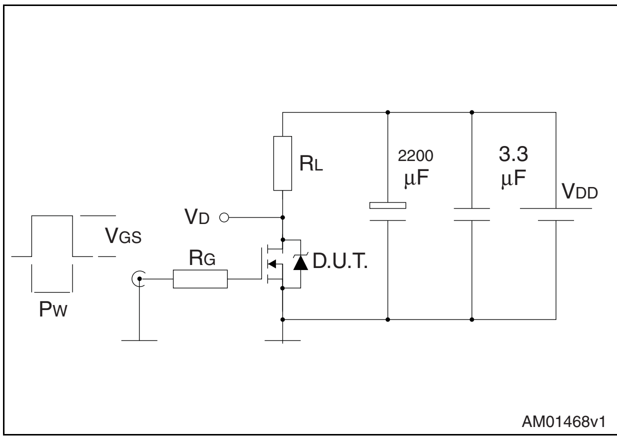


Figure 20. Gate charge test circuit

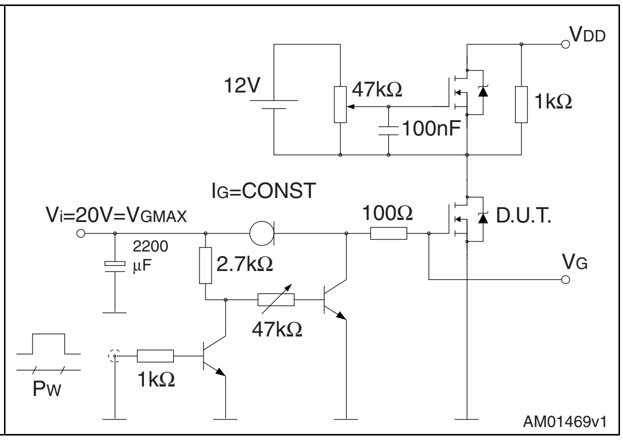


Figure 21. Test circuit for inductive load switching and diode recovery times

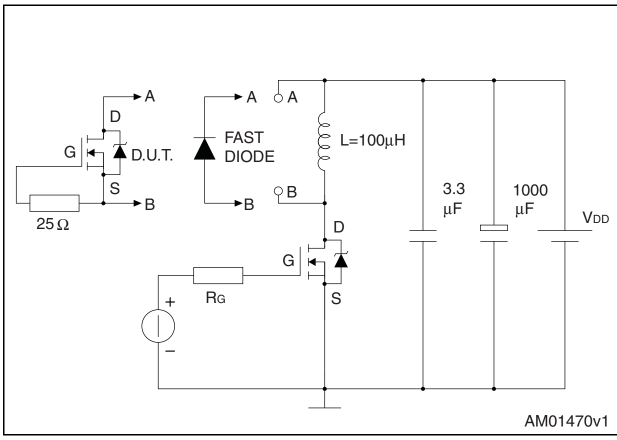


Figure 22. Unclamped Inductive load test circuit

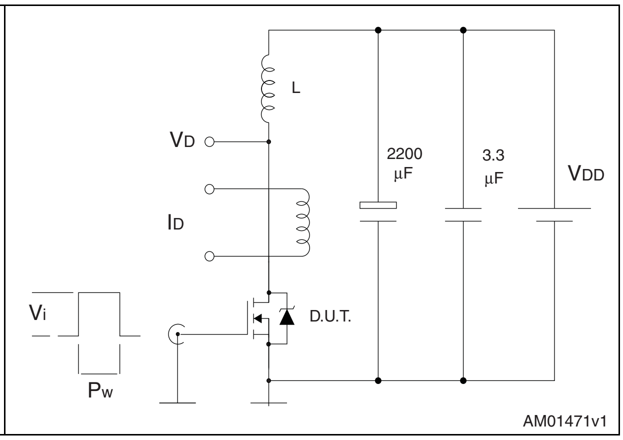


Figure 23. Unclamped inductive waveform

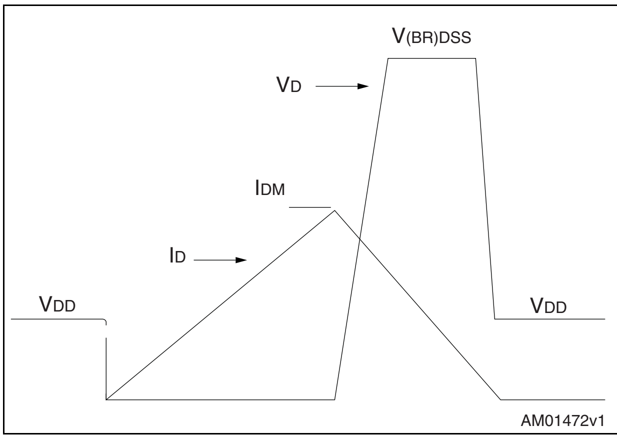
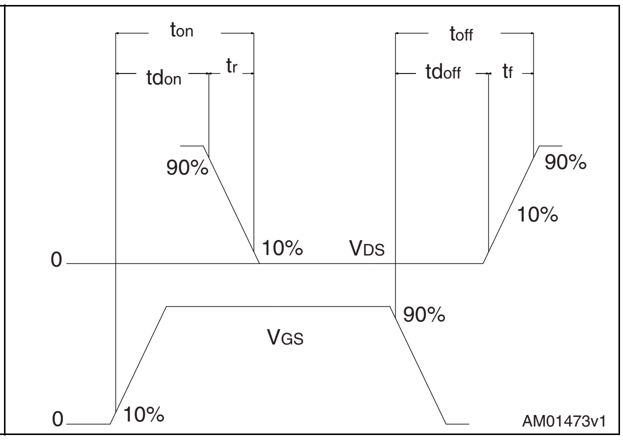


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 25. D²PAK (TO-263) drawing

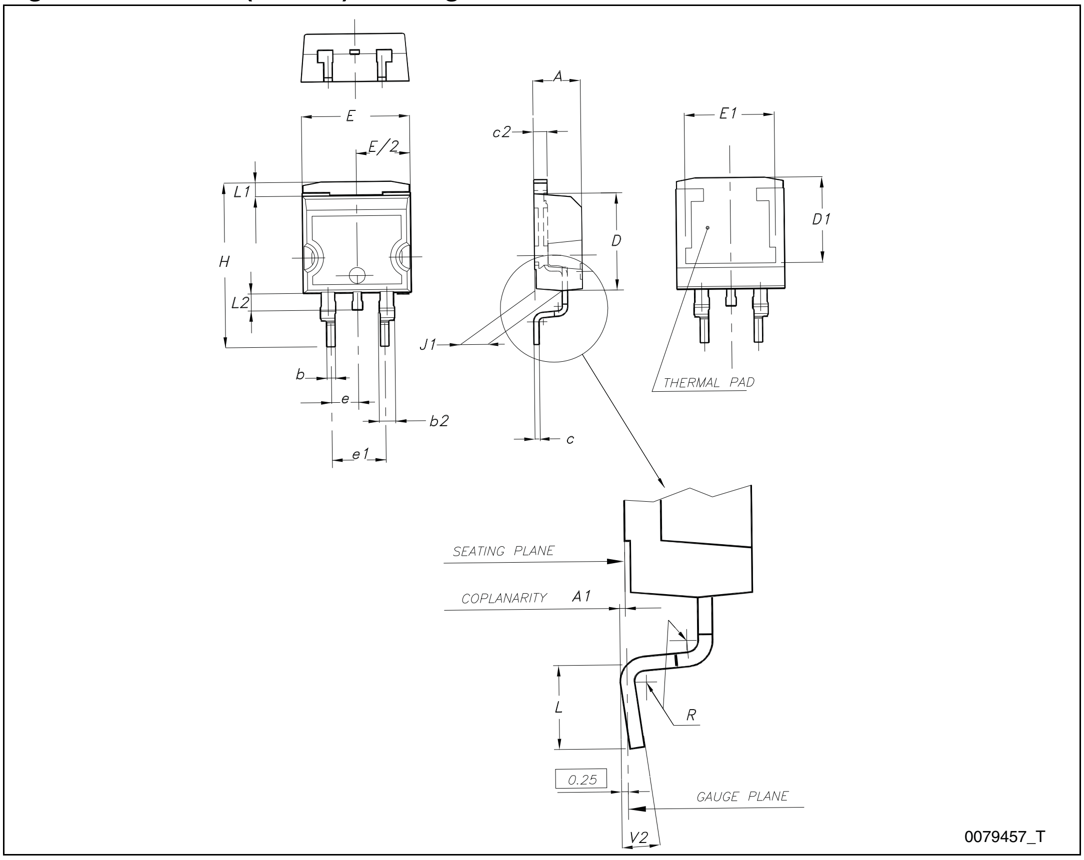
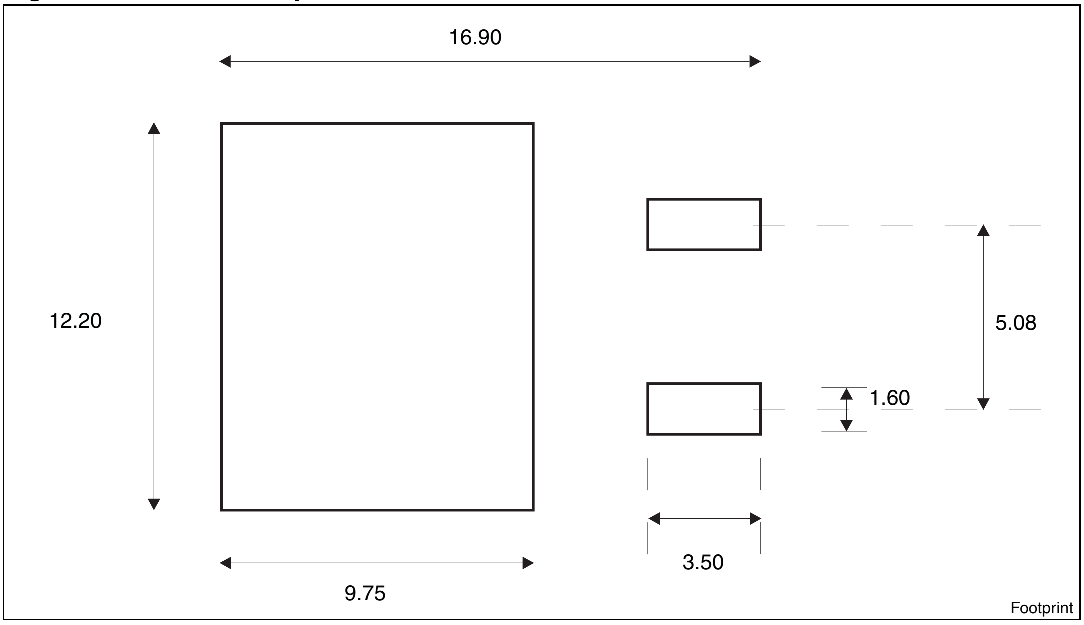


Figure 26. D²PAK footprint[(a)]



a. All dimension are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 27. DPAK (TO-252) drawing

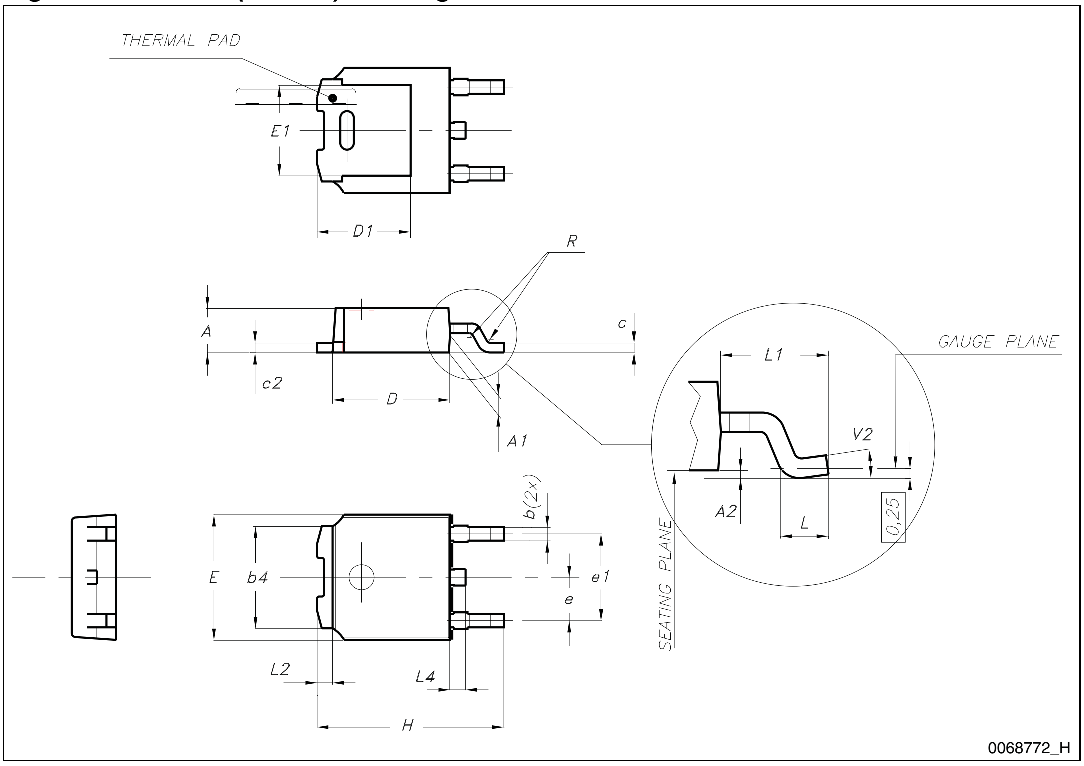
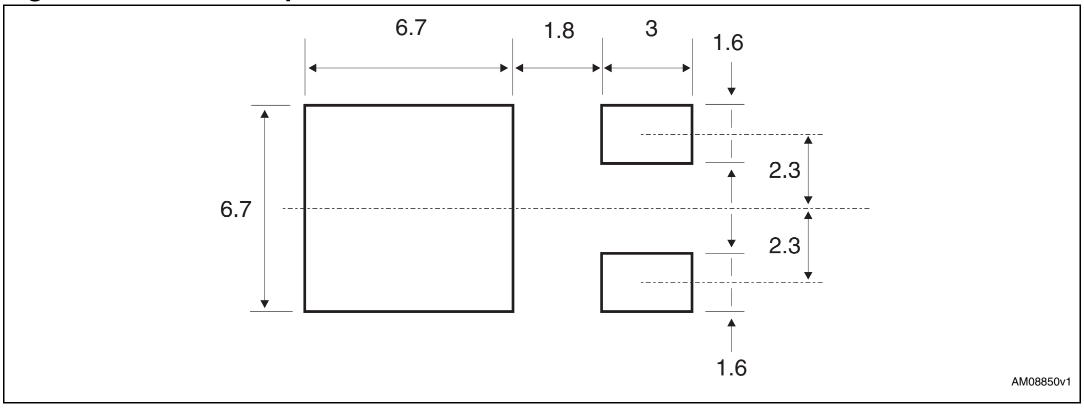


Figure 28. DPAK footprint[b]



b. All dimension are in millimeters

Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 29. TO-220FP drawing

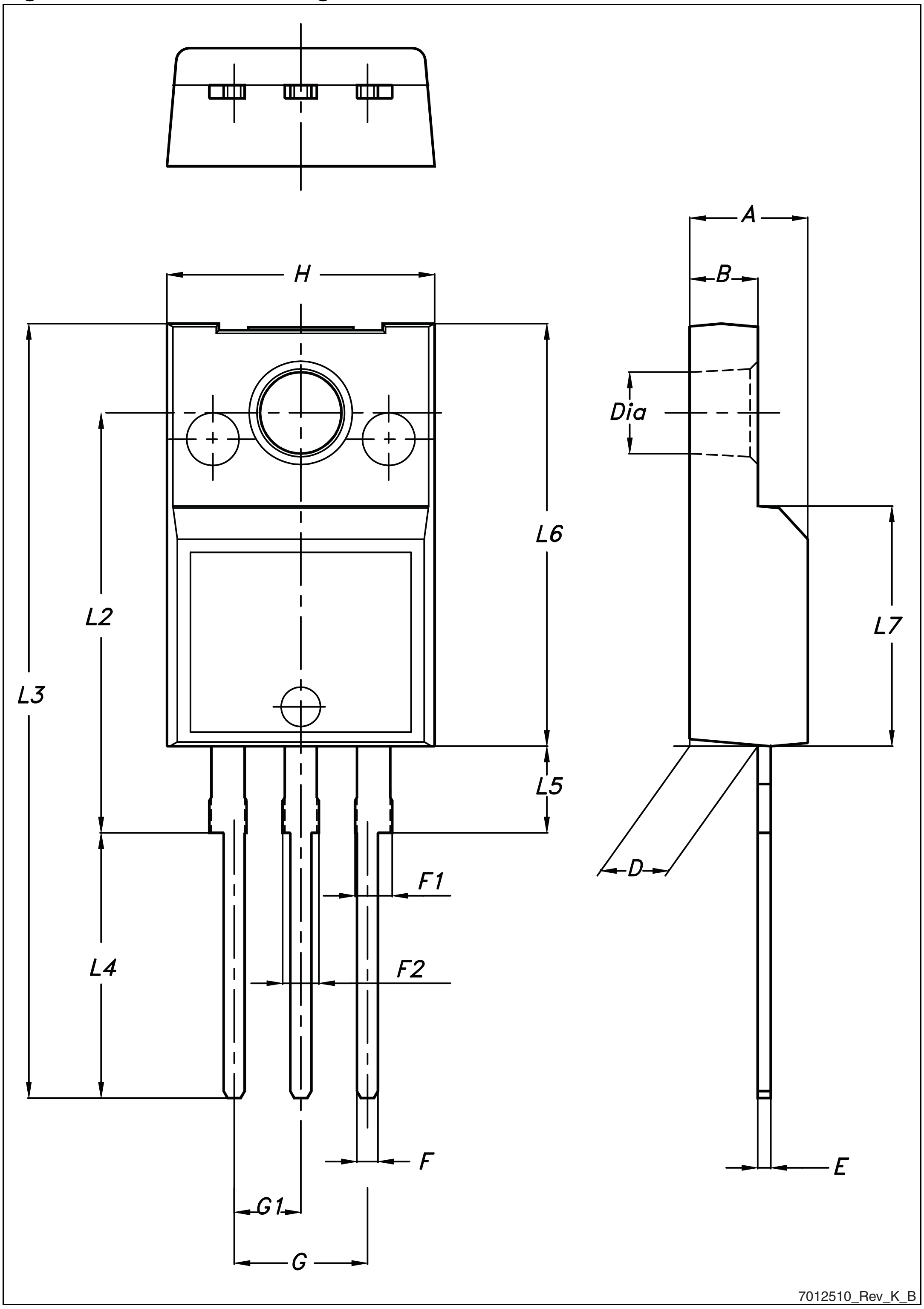
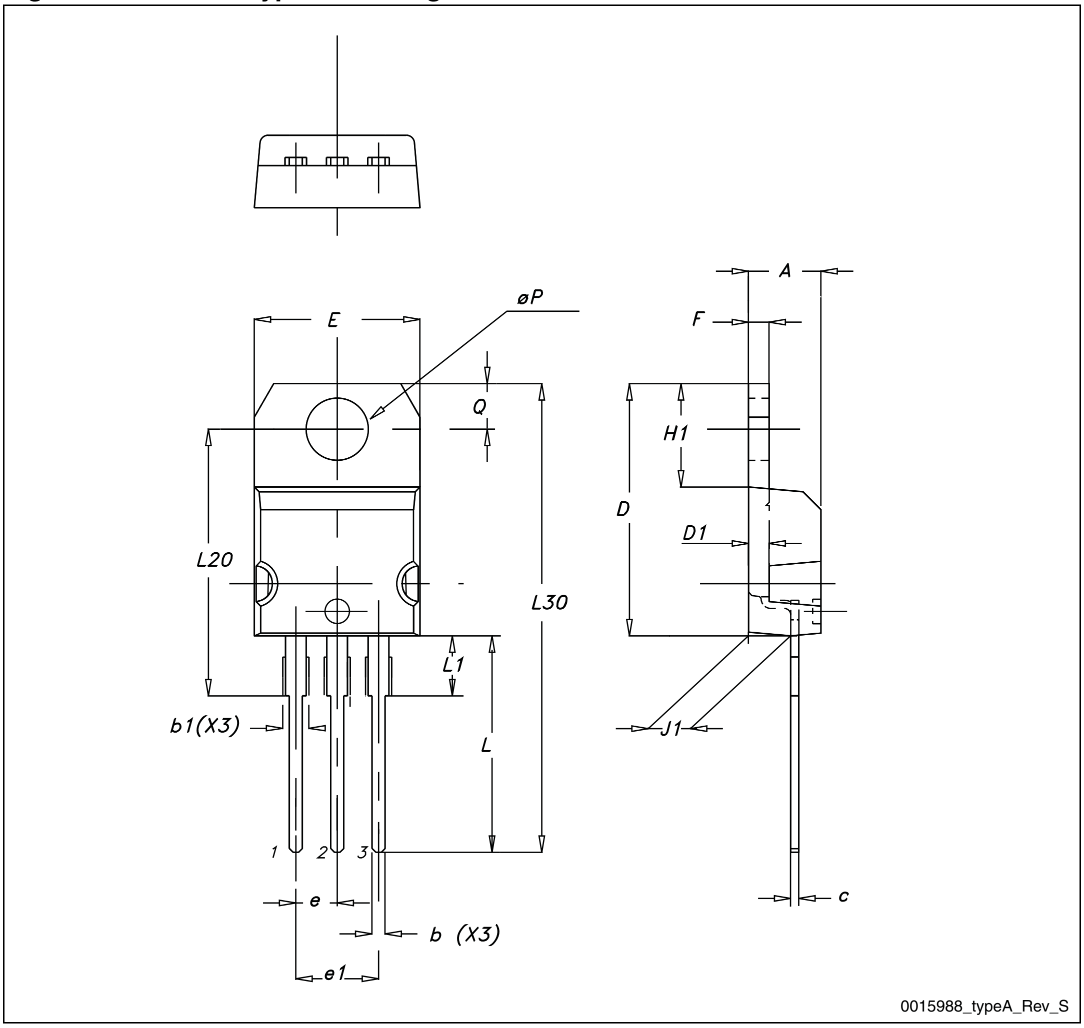


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 30. TO-220 type A drawing



5 Package mechanical data

Table 13. D^2PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500

Table 14. DPAK (TO-252) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 31. Tape for DPAK (TO-252) and D²PAK (TO-263)

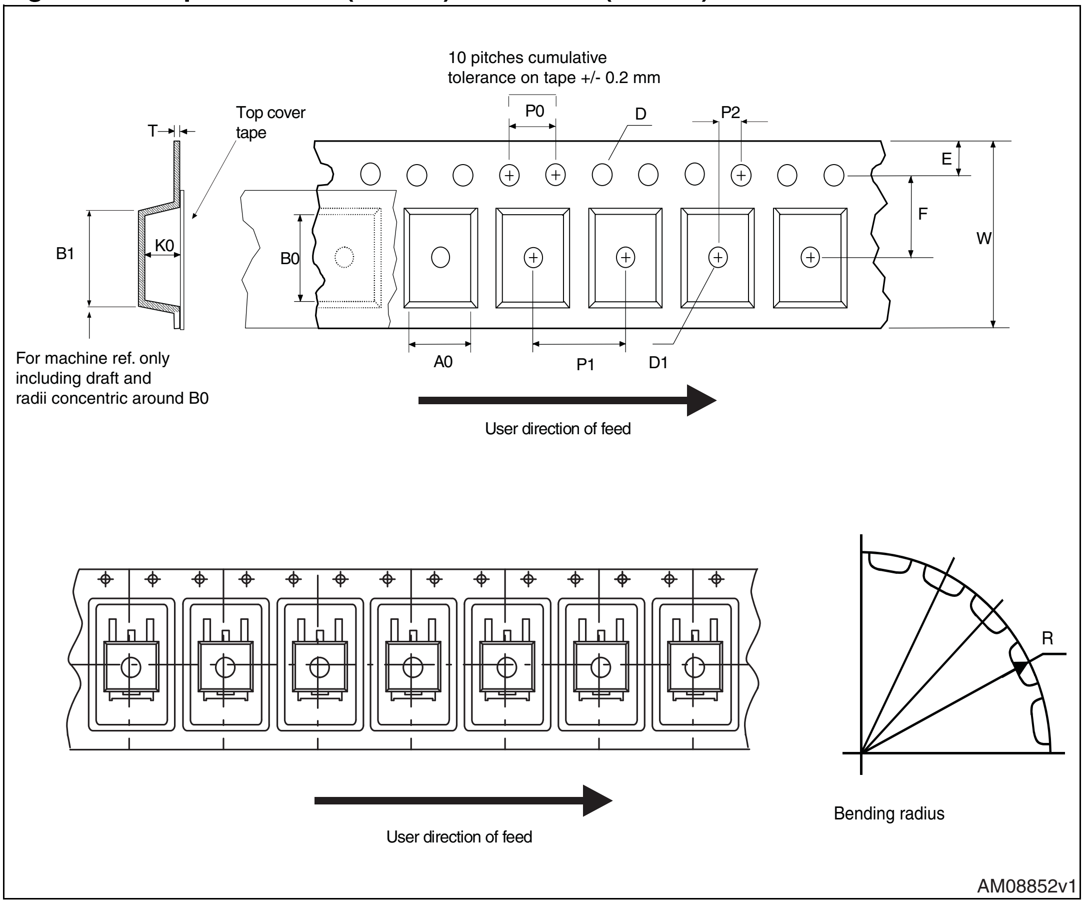
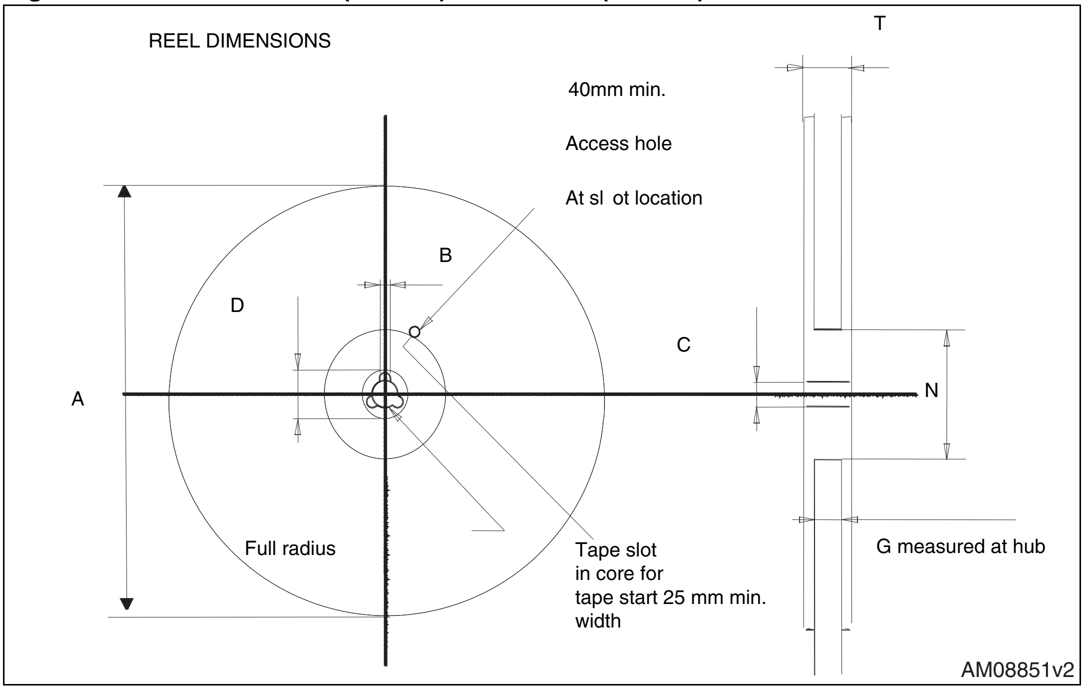


Figure 32. Reel for DPAK (TO-252) and D²PAK (TO-263)



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
07-Jul-2008	1	First release.
10-Sep-2009	2	Document status promoted from preliminary data to datasheet.
27-Jun-2011	3	*Section 2.1: Electrical characteristics (curves)* has been updated.
07-Mar-2012	4	Updated *Section 4: Package mechanical data*. Minor text changes.