

N-channel 500 V, 0.73 Ω , 5 A MDmesh™II Power MOSFET
in TO-220FP

Features

Order codes	$V_{DSS}@T_{JMAX}$	$R_{DS(on)}\text{max.}$	I_D
STF8NM50N	550 V	< 0.79 Ω	5 A

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

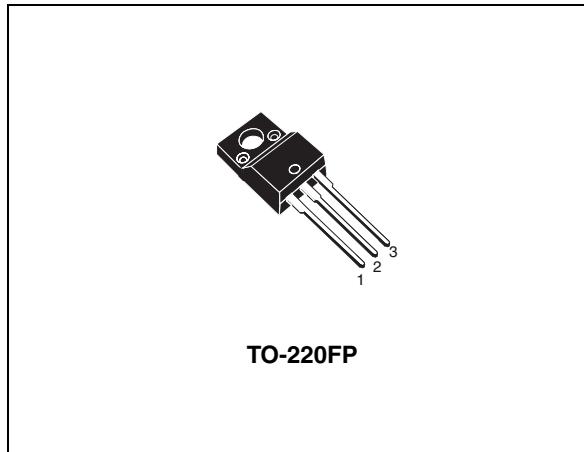


Figure 1. Internal schematic diagram

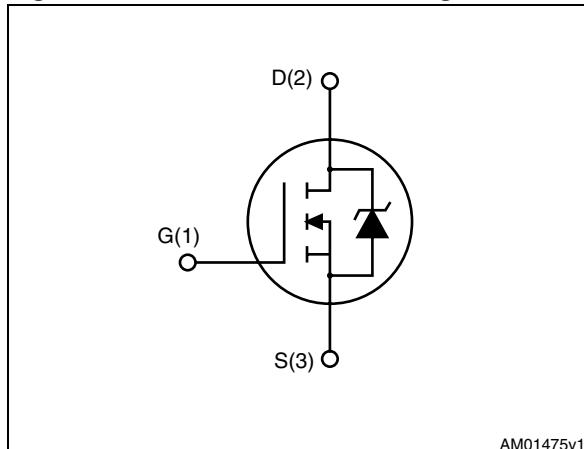


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STF8NM50N	8NM50N	TO-220FP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	5 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	20	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1 \text{ s}; T_C = 25^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Limited by maximum junction temperature.

2. $I_{SD} \leq 7 \text{ A}, di/dt \leq 400 \text{ A}/\mu\text{s}, V_{Peak} < V_{(BR)DSS}, V_{DS} = 80\% V_{(BR)DSS}$ **Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	6.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	140	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1 \text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500 \text{ V}$ $V_{DS} = 500 \text{ V}, T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{\text{DS}(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		0.73	0.79	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			364		pF
C_{oss}	Output capacitance		-	33	-	pF
C_{rss}	Reverse transfer capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		1.2		pF
$C_{\text{oss(eq)}}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0 \text{ to } 50 \text{ V}, V_{GS} = 0$	-	147.5	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	5.4	-	Ω
Q_g	Total gate charge			14		nC
Q_{gs}	Gate-source charge	$V_{DD} = 400 \text{ V}, I_D = 5 \text{ A}, V_{GS} = 10 \text{ V}$	-	3	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)		7		nC

1. $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(\text{on})}$	Turn-on delay time			7		ns
t_r	Rise time			4.4		ns
$t_{d(\text{off})}$	Turn-off-delay time		-	25	-	ns
t_f	Fall time	$V_{DD} = 250 \text{ V}, I_D = 5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 13)		8.8		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		5 20	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 5 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 18)	-	187 1.3 14		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 5 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 18)	-	224 1.5 13		ns μC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

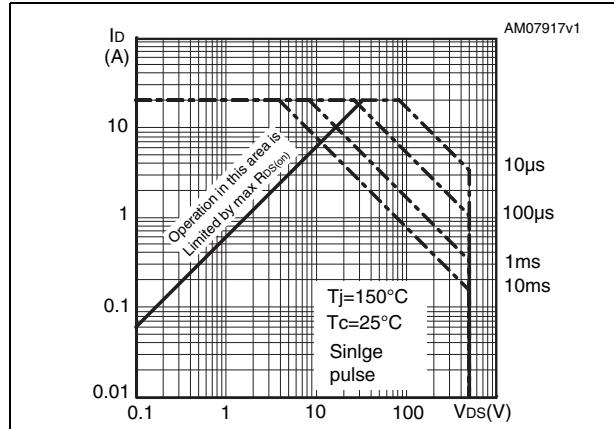


Figure 3. Thermal impedance

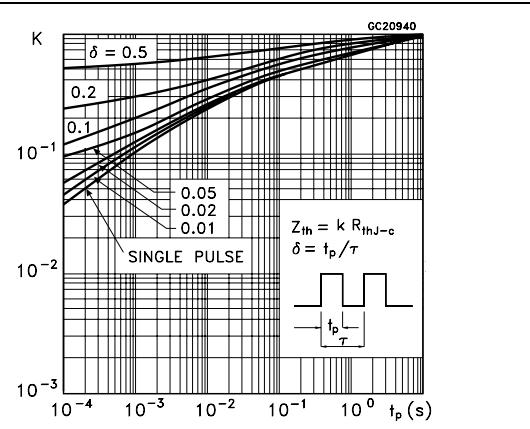


Figure 4. Output characteristics

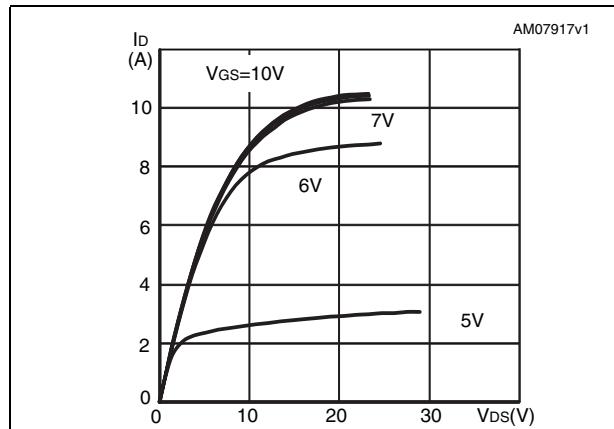


Figure 5. Transfer characteristics

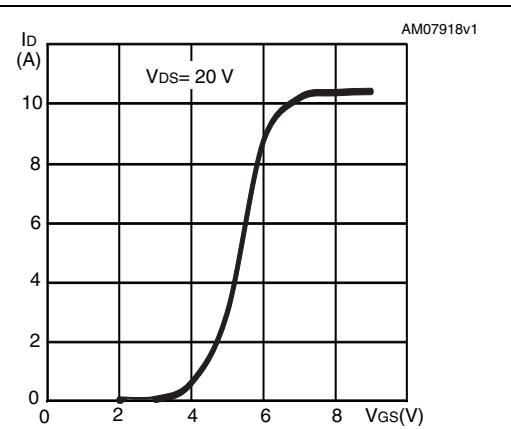


Figure 6. Static drain-source on resistance

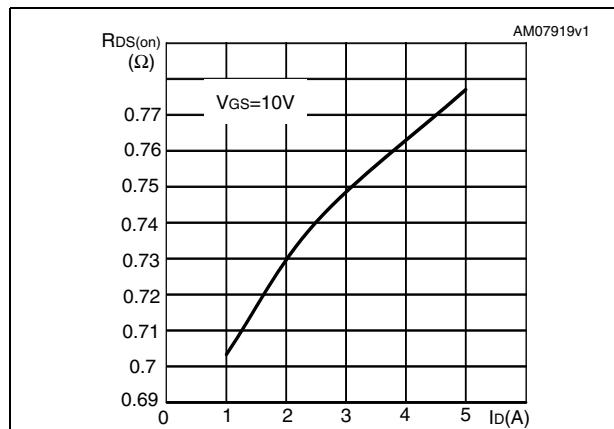


Figure 7. Gate charge vs gate-source voltage

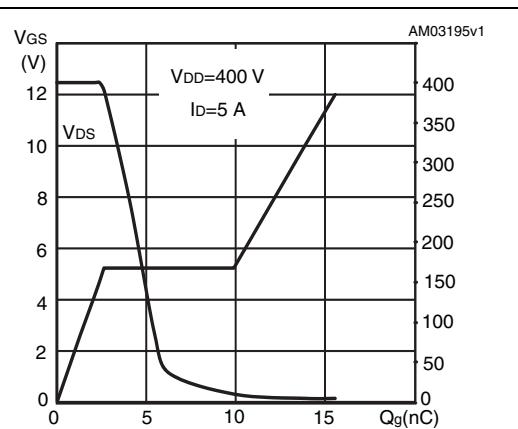
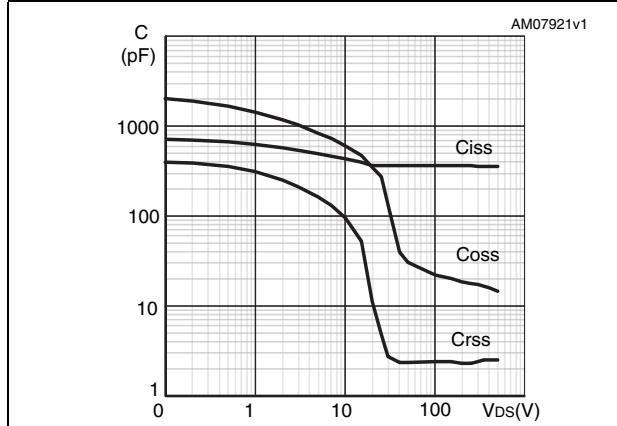
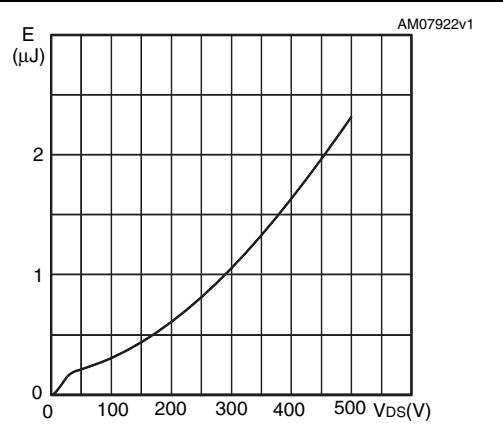
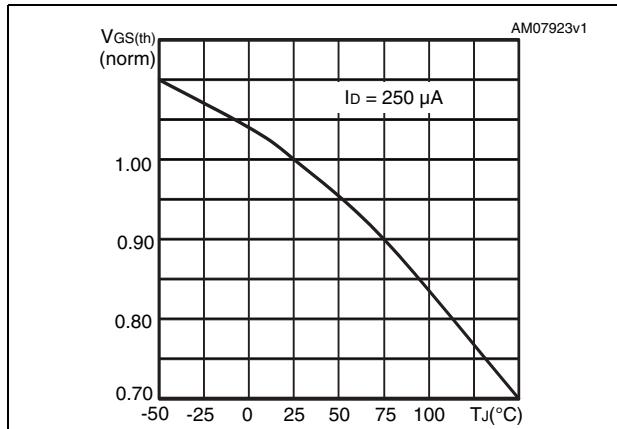
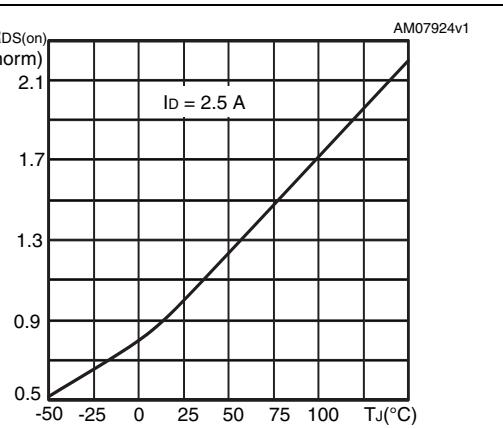
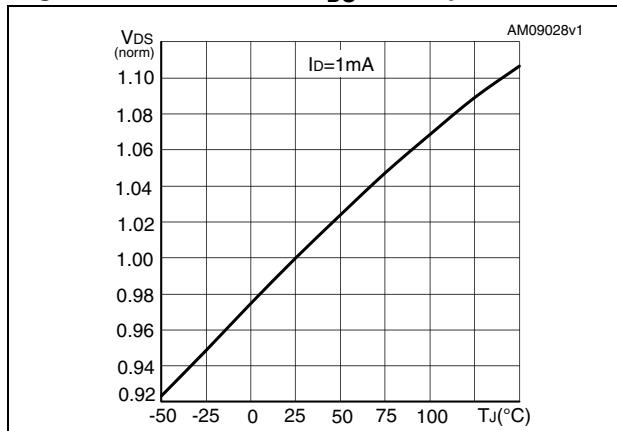


Figure 8. Capacitance variations**Figure 9. Output capacitance stored energy****Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Normalized V_{DS} vs temperature**

3 Test circuits

Figure 13. Switching times test circuit for resistive load

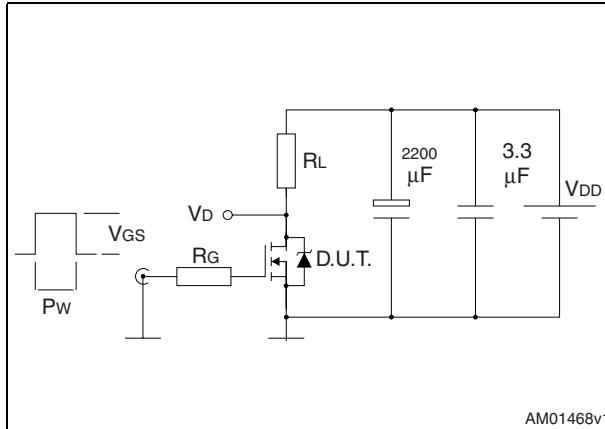


Figure 14. Gate charge test circuit

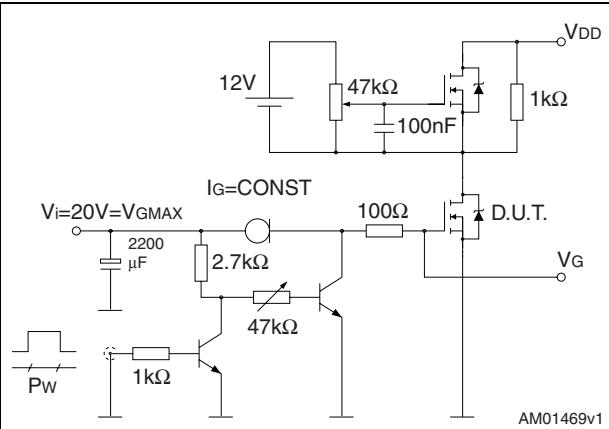


Figure 15. Test circuit for inductive load switching and diode recovery times

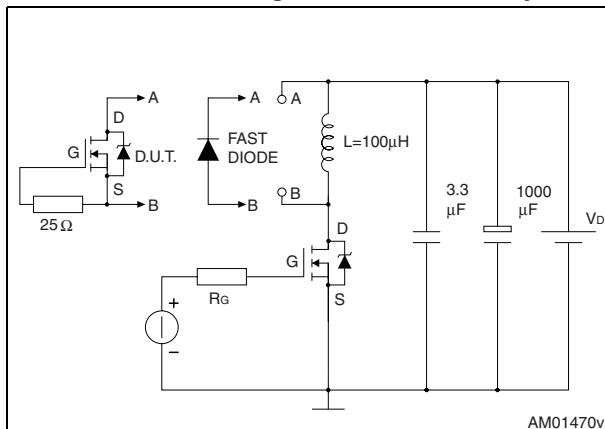


Figure 16. Unclamped inductive load test circuit

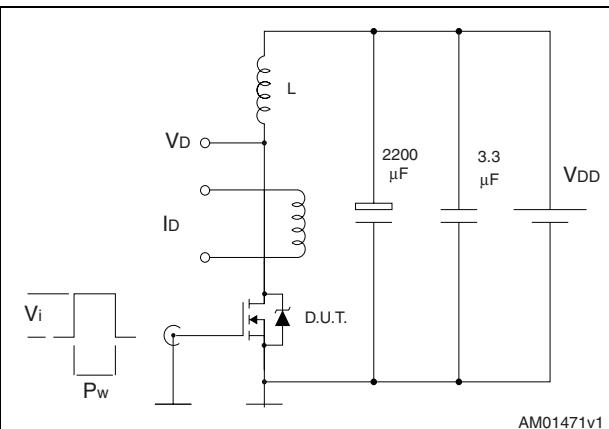


Figure 17. Unclamped inductive waveform

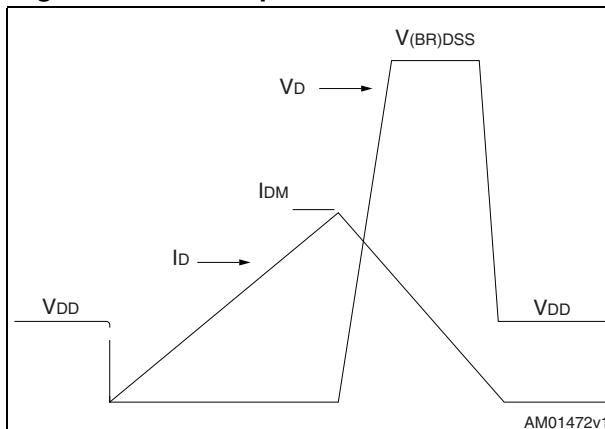
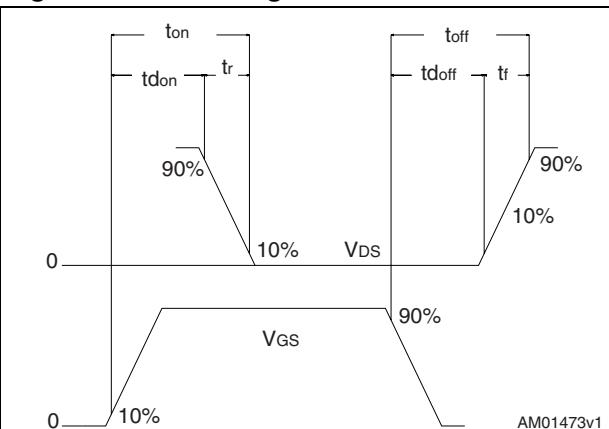


Figure 18. Switching time waveform

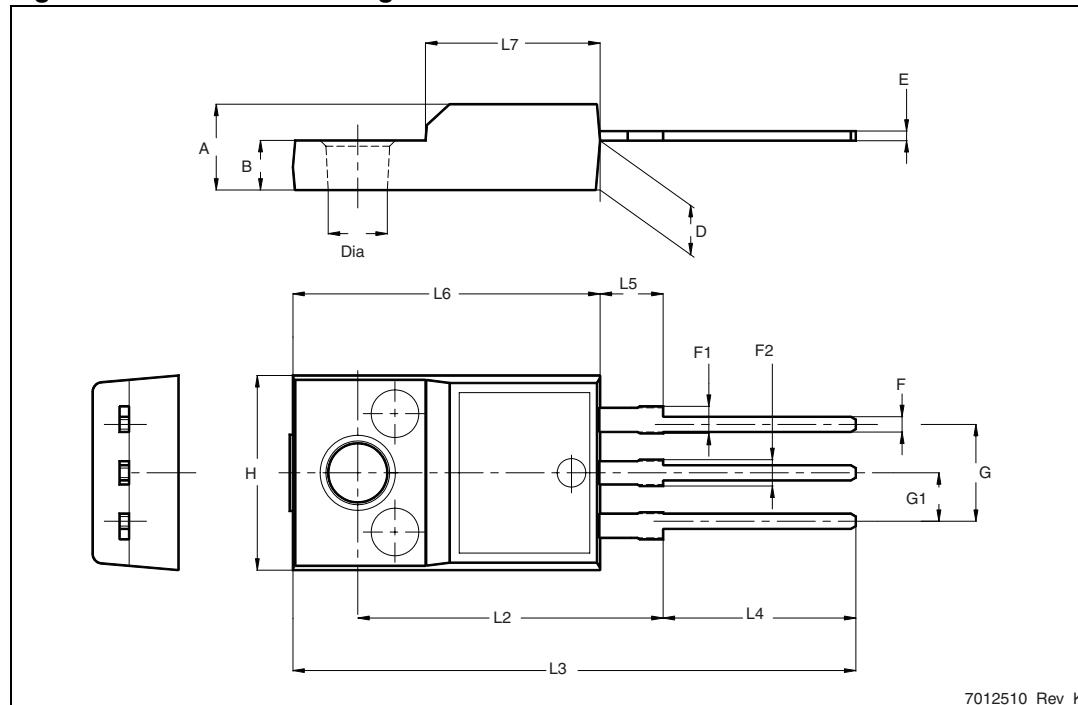


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 19. TO-220FP drawing

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Nov-2011	1	First release.
18-Nov-2011	2	Updated dv/dt in Table 2: Absolute maximum ratings .

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