

# PMN50XP

## P-channel TrenchMOS extremely low level FET

Rev. 02 — 2 October 2007

Product data sheet

## 1. Product profile

### 1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features

- Low on-state losses
- Low threshold voltage

### 1.3 Applications

- Battery management
- Battery powered portable equipment
- Load Switching
- Low power DC to DC converters

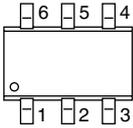
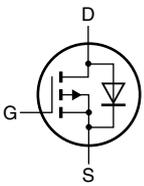
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	-20	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ °C};$ see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	-4.8	A
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = -4.5\text{ V}; I_D = -4.7\text{ A};$ $V_{DS} = -10\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	1.3	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2.8\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 7</a> and <a href="#">8</a>	-	48	60	mΩ

## 2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	D	drain		
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

003aaa671

## 3. Ordering information

Table 3. Ordering information

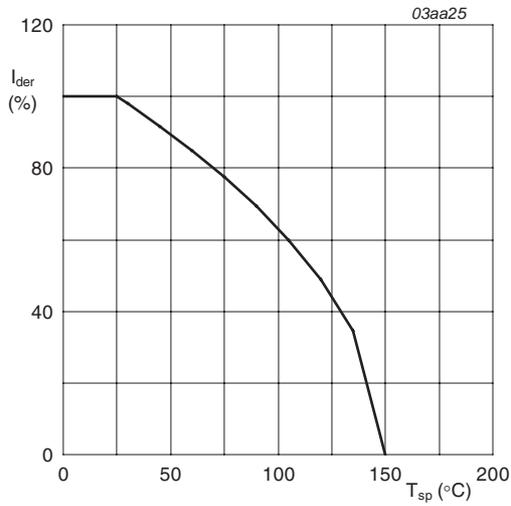
Type number	Package		
	Name	Description	Version
PMN50XP	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

## 4. Limiting values

Table 4. Limiting values

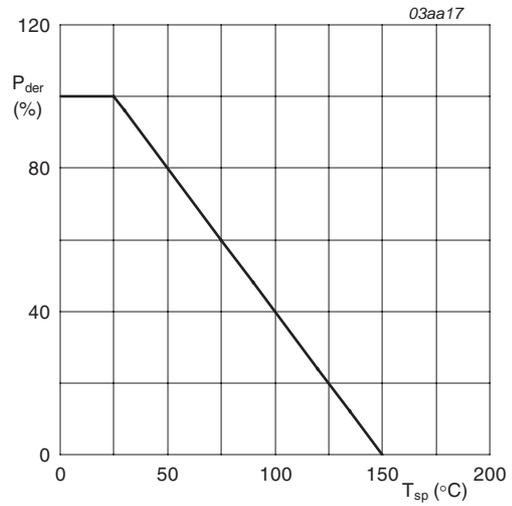
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-20	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	-20	V
$V_{GS}$	gate-source voltage		-12	12	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = -4.5\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-4.8	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = -4.5\text{ V}$	-	-3	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; $t_p < 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	-19.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	2.2	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	-1.9	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed	-	-7.5	A



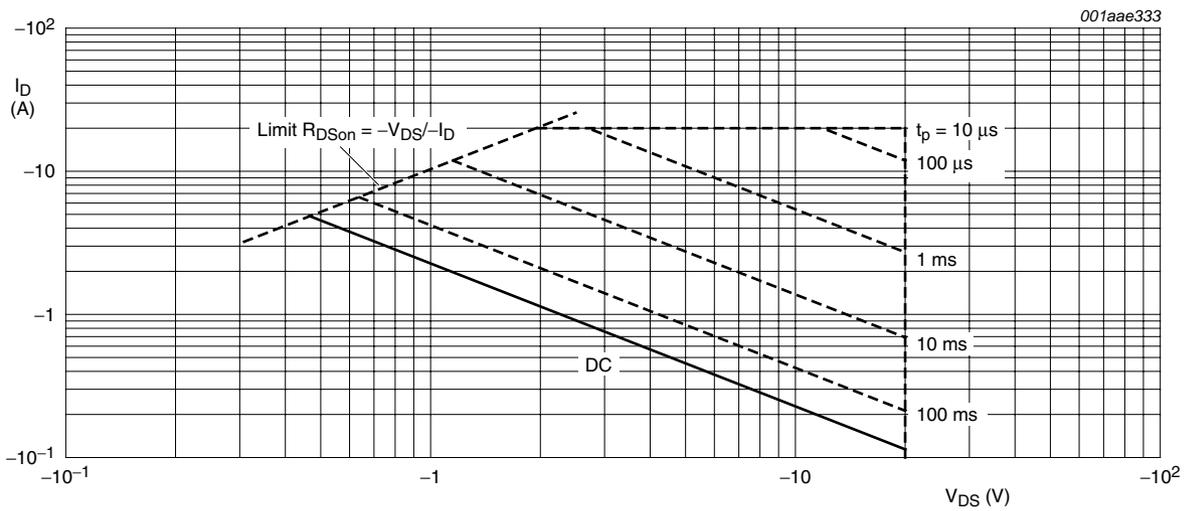
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	55	K/W

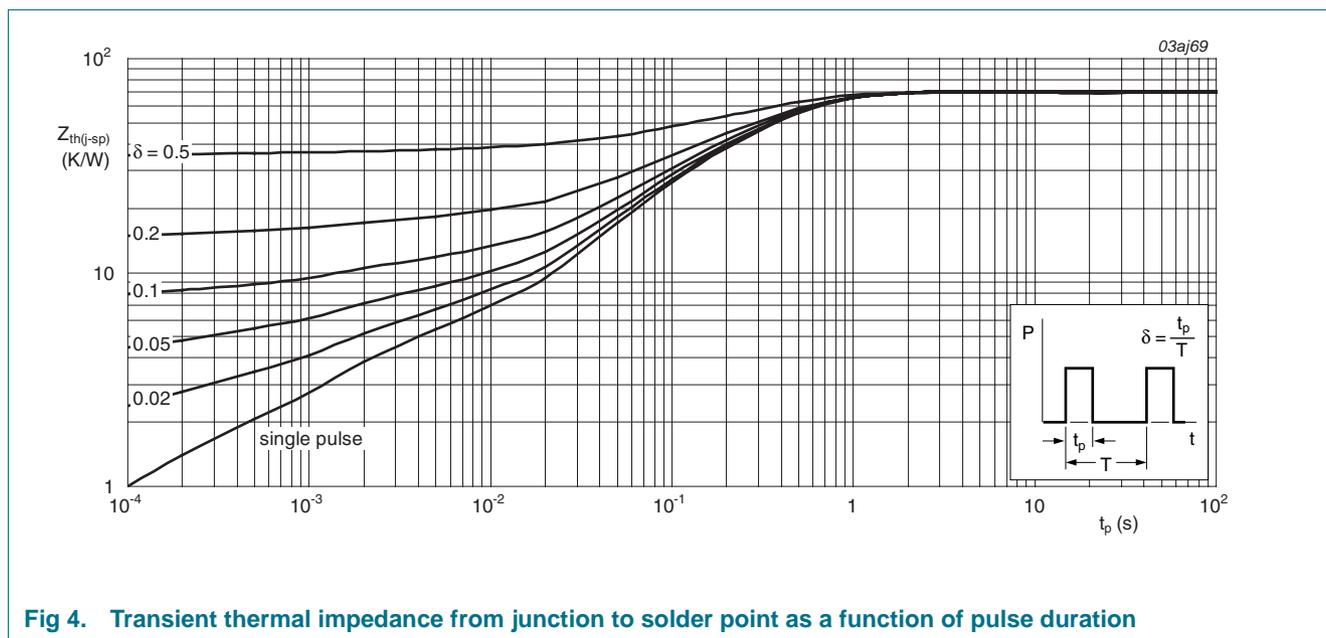


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

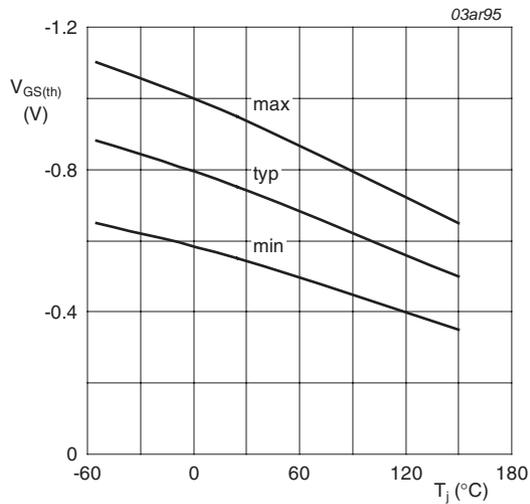
## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
		$I_D = -250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	-18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 5</a> and <a href="#">6</a>	-0.55	-0.75	-0.95	V
		$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 5</a> and <a href="#">6</a>	-0.35	-	-	V
		$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 5</a> and <a href="#">6</a>	-	-	-1.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 70 \text{ }^\circ C$	-	-	-5	$\mu A$

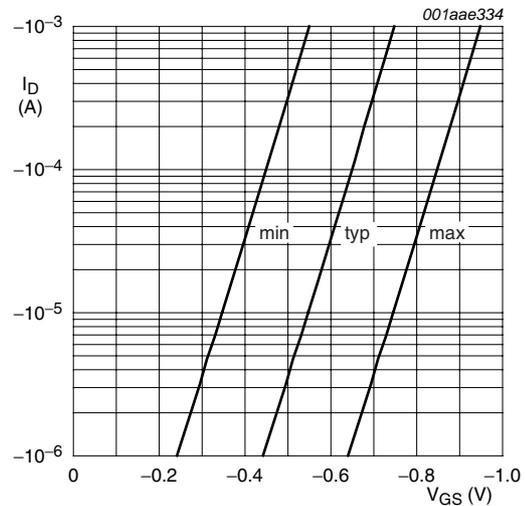
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> ≤ 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-10	-100	nA
		V <sub>GS</sub> ≥ 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-10	-100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -2.8 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 7</a> and <a href="#">8</a>	-	48	60	mΩ
		V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -2.8 A; T <sub>j</sub> = 150 °C; see <a href="#">Figure 7</a> and <a href="#">8</a>	-	77	96	mΩ
		V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -2.3 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 7</a> and <a href="#">8</a>	-	65	80	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = -4.7 A; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	10	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = -4.7 A; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	2.2	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = -4.7 A; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	1.3	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	1020	-	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = -20 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	140	-	pF
C <sub>rss</sub>	reverse transfer capacitance	V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	100	-	pF
t <sub>d(on)</sub>	turn-on delay time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 10 Ω; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C	-	8.5	-	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 10 Ω; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C	-	7.5	-	ns
t <sub>d(off)</sub>	turn-off delay time	V <sub>DS</sub> = -10 V; R <sub>L</sub> = 10 Ω; V <sub>GS</sub> = -4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	82	-	ns
t <sub>f</sub>	fall time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 6 Ω; V <sub>DS</sub> = -10 V; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C	-	35	-	ns
V <sub>GS(pl)</sub>	gate-source plateau voltage	V <sub>DS</sub> = -10 V; I <sub>D</sub> = -4.7 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	-1.6	-	V
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = -1.7 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-0.77	-1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 3.5 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C	-	-	-	ns



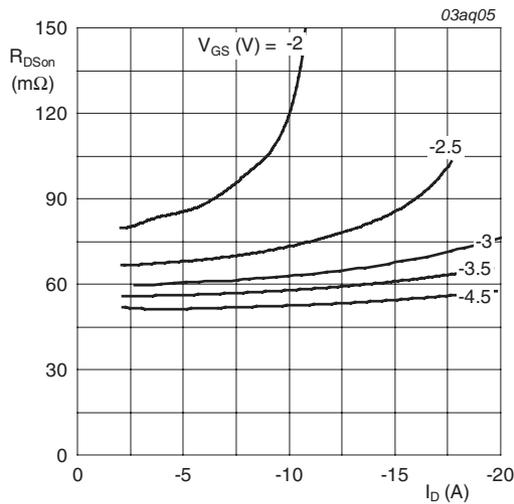
$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature



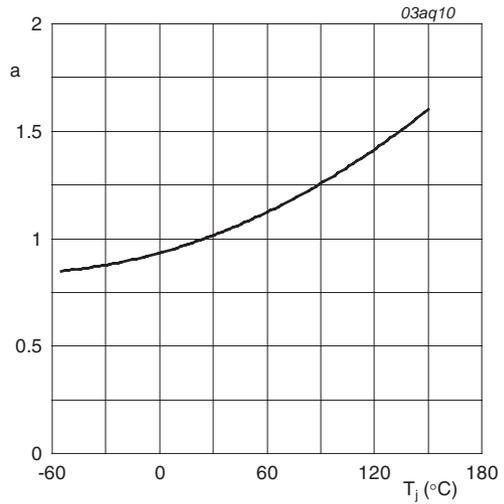
$T_j = 25 \text{ °C}; V_{DS} = -5 \text{ V}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



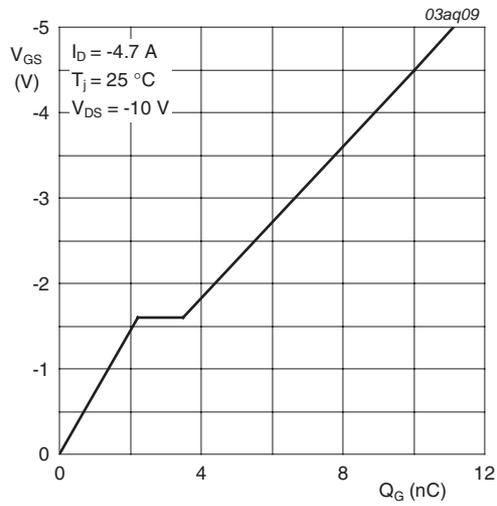
$T_j = 25 \text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = -4.7 \text{ A}; T_j = 25 \text{ }^\circ\text{C}; V_{DS} = -10 \text{ V}$

Fig 9. Gate-source voltage as a function of gate charge; typical values

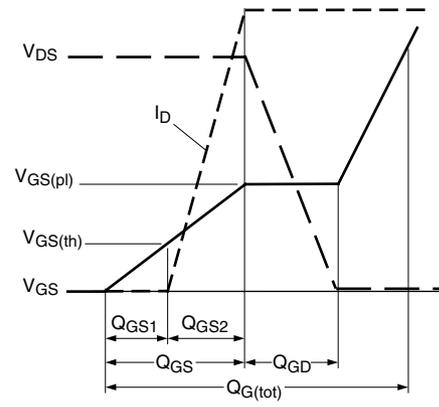
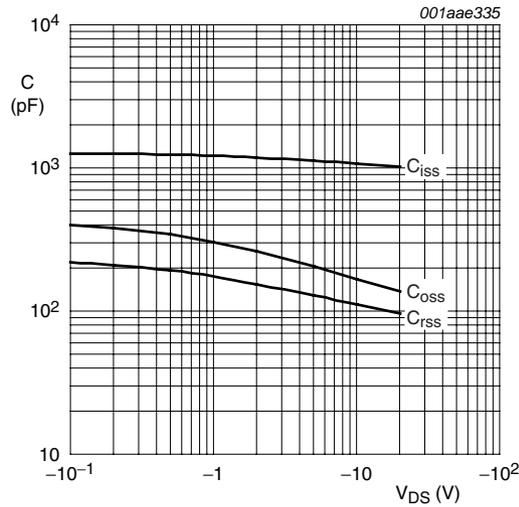


Fig 10. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

## 7. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

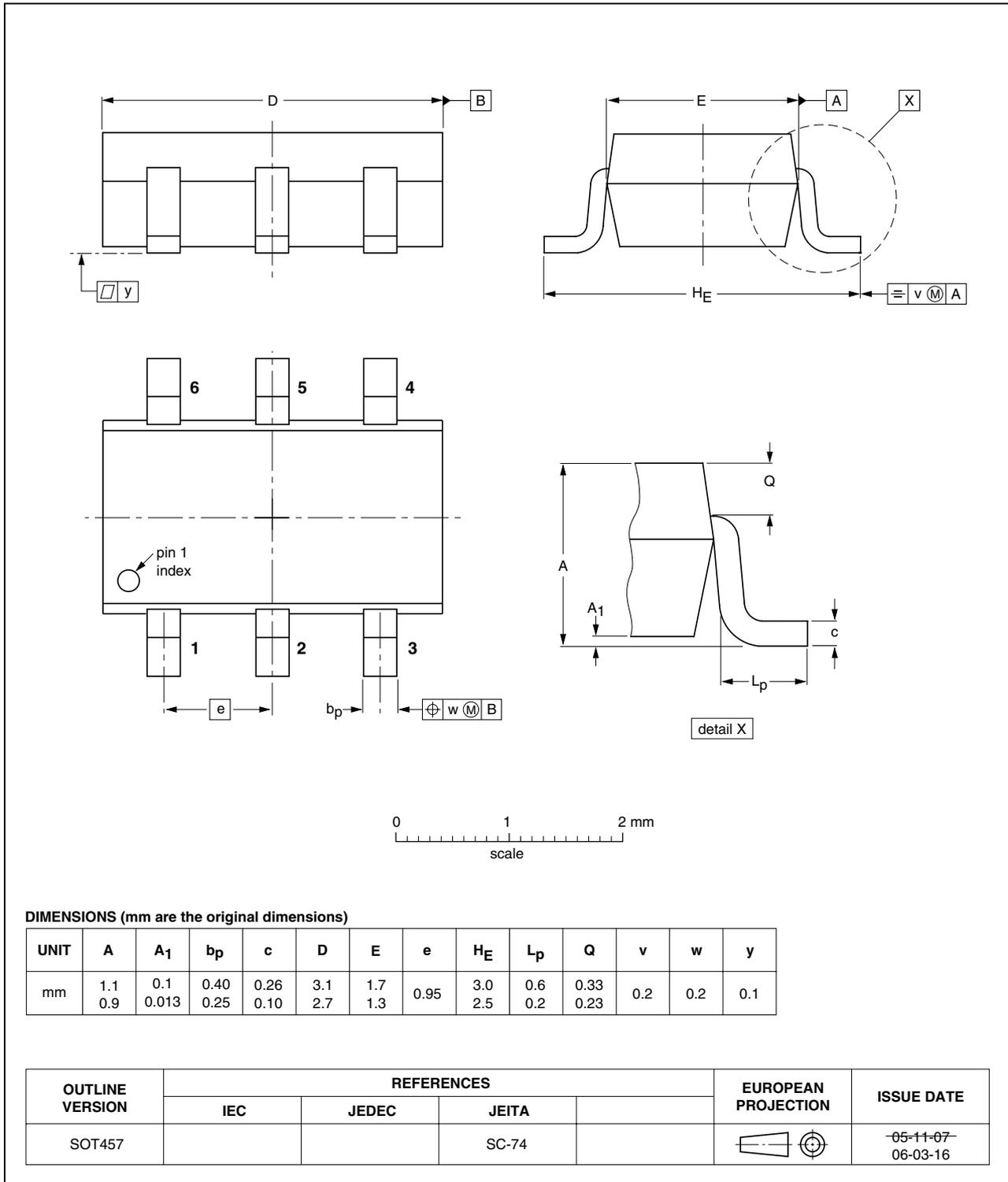


Fig 12. Package outline SOT457 (TSOP6)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN50XP_2	20071002	Product data sheet	-	PMN50XP_1
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the company name where appropriate.</li></ul>		
PMN50XP_1	20060123	Product data sheet	-	-

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### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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