

Triple/Quad, 2:1 Video Multiplexer-Amplifiers with Input Clamps

General Description

The MAX4028/MAX4029 are 5V, triple/quad, 2:1 voltagefeedback multiplexer-amplifiers with input clamps and a fixed gain of +2V/V (6dB). Channel 1 (IN1A and IN1B) inputs are clamped to the video sync tip of the input signal, while the remaining inputs can be clamped to either the video sync tip or the video sync of channel 1 (IN1_). The latter is referred to as a key clamp and is pin selectable. Selectable clamp/key-clamp inputs and fixed-gain video output buffers make the MAX4028/MAX4029 ideal for video-source switching applications such as automotive entertainment systems, video projectors, and displays/TVs. Both devices have 20ns channel switching times and low ± 10 mVP-P switching transients, making them ideal for high-speed video switching applications such as on-screen display (OSD) insertion.

The MAX4028/MAX4029 have a -3dB large-signal (2VP-P) bandwidth of 130MHz, a -3dB small-signal bandwidth of 210MHz, and a 300V/ μ s slew rate. Low differential gain and phase errors of 0.2% and 0.4°, respectively, make these devices ideal for broadcast video applications.

The MAX4028/MAX4029 are specified over the -40°C to +85°C extended temperature range and are offered in 16-pin and 20-pin TSSOP/SO packages.

Applications
In-Car Navigation/Entertainment
Blade Servers
Security Systems
Video Projectors
Displays and Digital Televisions
Broadcast and Graphics Video
Set-Top Boxes
Notebook Computers
Video Crosspoint Switching

Selector Guide

PART	NO. OF 2:1 MUX-AMPS	GAIN
MAX4028	3	2V/V
MAX4029	4	2V/V

Pin Configurations appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Features

- Single +5V Operation
- Independently Selectable Sync-Tip or Key-Clamp Inputs
- Adjustable Key-Clamp Voltage
- 130MHz Large-Signal -3dB Bandwidth
- 210MHz Small-Signal -3dB Bandwidth
- ♦ 300V/µs Slew Rate
- 20ns Switching Time
- ♦ Ultra-Low ±10mVP-P Switching Transient
- 0.2% Differential Gain/0.4° Phase Error
- ♦ Low-Power, High-Impedance Disable Mode

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4028EUE	-40°C to +85°C	16 TSSOP
MAX4028EWE	-40°C to +85°C	16 Wide SO
MAX4029EUP	-40°C to +85°C	20 TSSOP
MAX4029EWP	-40°C to +85°C	20 Wide SO



Typical Operating Circuit

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC} to GND)0.3V to +6V IN_A, IN_B, OUT0.3V to (V _{CC} + 0.3V DISABLE, A/B, KEYREF, CLAMP/KEY0.3V to (V _{CC} + 0.3V)
Current Into IN_A, IN_B±0.5mA	
Short-Circuit Duration (VOUT to GND)Continuous	S
Short-Circuit Duration (VOUT to VCC)(Note 1)
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
16-Pin TSSOP (derate 9.4mW/°C above +70°C)755mW	V
16-Pin Wide SO (derate 9.5mW/°C above +70°C)762mW	V

Note 1: Do not short VOUT to VCC.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +5V, GND = 0V, R_L = 150\Omega \text{ to GND}, V_{\overline{DISABLE}} = +5V, R_{KEYREF} = 6k\Omega, C_{IN} = 0.1\mu\text{F to GND}, T_A = T_{MIN} \text{ to } T_{MAX}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C.}$ (Note 2)

PARAMETER	SYMBOL	CONDI	TIONS	MIN	ТҮР	MAX	UNITS
Operating Supply Voltage Range	V _{CC}	Guaranteed by PSF	R	4.5		5.5	V
		MAX4028, R _L = ∞			29	40	
Quiescent Supply Current	Icc	MAX4029, R _L = ∞			38	55	mA
			MAX4028		9	15	
Disable Supply Current		$V_{\overline{\text{DISABLE}}} = 0V$	MAX4029		11	20	mA
	Maxim	Clamp (Note 3)		0.32	0.4	0.48	v
Output Clamp Voltage	VCLAMP	Key clamp (Note 4)	i i		1.1		V
Input Clamping Current	I _{IN}	Input voltage = input	ut clamp + 0.5V		5	18	μA
Clamp Voltage Matching	ΔV_{CLAMP}	Measured at output	t		10		mV
Clamp Voltage Drift	TCVCLAMP	Measured at output	t		80		µV/°C
Input Resistance	R _{IN}				7		MΩ
Output Resistance	Rout				0.7		Ω
Disable Output Resistance	Rout	V _{DISABLE} = 0V			2		kΩ
Power-Supply Rejection Ratio	PSRR	$4.5V < V_{CC} < 5.5V$	(Note 5)	48	58		dB
Voltage Gain	Avcl			1.9	2.0	2.1	V/V
Channel-to-Channel Gain Matching	ΔA_{VCL}				±1	±2	%
Output-Voltage High	VOH			V _{CLAMP} + 2.4			V
Output-Voltage Low	VOL					VCLAMP	V
Output Current	IOUT			30			mA
LOGIC INPUT CHARACTERISTICS	(DISABLE ,	A/B, CLAMP/KEY_)					
Logic-Low Threshold	VIL					0.8	V
Logic-High Threshold	VIH			2.0			V
Logic-Low Input Current	١ _١ ٢	$V_{IL} = 0V$			6.6	25	μA
Logic-High Input Current	IIН	VIH = VCC			1.2	25	μA

AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +5V, GND = 0V, R_L = 150\Omega \text{ to GND}, V_{DISABLE} = +5V, R_{KEYREF} = 6k\Omega, C_{IN} = 0.1\mu\text{F}, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted}.$ Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Small-Signal -3dB Bandwidth	BWSS	V _{OUT} = 100mV _{P-P}		210		MHz
Large-Signal -3dB Bandwidth	BWLS	V _{OUT} = 2V _{P-P}		130		MHz
Small-Signal 0.1dB Gain Flatness Bandwidth	BW _{0.1dBSS}	V _{OUT} = 100mV _{P-P}		30		MHz
Large-Signal 0.1dB Gain Flatness Bandwidth	BW _{0.1dBLS}	V _{OUT} = 2V _{P-P}		30		MHz
Slew Rate	SR	$V_{OUT} = 2V_{P-P}$		300		V/µs
Settling Time to 0.1%	ts	V _{OUT} = 2V step		20		ns
Power-Supply Rejection Ratio	PSRR	f = 100kHz		55		dB
Output Impedance	ZO	f = 100 kHz		0.7		Ω
Differential Gain Error	DG	5-step modulated staircase		0.2		%
Differential Phase Error	DP	5-step modulated staircase		0.4		degrees
Group Delay	D/dT	f = 3.58MHz or 4.43MHz		1.0		ns
Peak Signal to RMS Noise	SNR	100kHz to 30MHz		70		dB
Channel-to-Channel Crosstalk	X _{TALK}	f = 100kHz		73		dB
A/B Crosstalk	XTALKAB	f = 100kHz		91		dB
Off-Isolation	AISO	$V_{OUT} = 2V_{P-P}, f = 100 \text{kHz}$		108		dB
Droop	DR	Guaranteed by input clamp current			2	%
SWITCHING CHARACTERISTICS						
Channel Switching Time	tsw			20		ns
Enable Time	ton			0.1		μs
Disable Time	toff			0.1		μs
Switching Transient				±10		mV _{P-P}

Note 2: All devices are 100% production tested at $T_A = +25$ °C. Specifications over temperature are guaranteed by design.

Note 3: The clamp voltage at the input is V_{CLAMP} (measured at the output) divided by gain + V_{BE} .

Note 4: The key-clamp voltage is above the sync-tip clamp voltage by approximately 0.7V, and is adjusted by varying R_{KEYREF} . **Note 5:** Measured at f = 100Hz at thermal equilibrium.

 $(V_{CC} = +5V, GND = 0V, V_{DISABLE} = +5V, R_L = 150\Omega$ to GND, $C_{IN} = 0.1\mu$ F, $R_{KEYREF} = 6.04k\Omega \pm 1\%$, $T_A = +25^{\circ}$ C, unless otherwise noted.)

Typical Operating Characteristics

1G

1G

1G

/N/IXI/N

FREQUENCY (Hz)

SMALL-SIGNAL BANDWIDTH **SMALL-SIGNAL GAIN FLATNESS** LARGE-SIGNAL BANDWIDTH vs. FREQUENCY vs. FREQUENCY vs. FREQUENCY 8 6.2 8 $V_{OUT} = 100 m V_{P-P}$ $V_{OUT} = 100mV_{P-P}$ $V_{OUT} = 2V_{P-P}$ 7 6.1 7 SMALL-SIGNAL BANDWIDTH (dB) -ARGE-SIGNAL BANDWIDTH (dB) 6 6.0 6 5 5.9 5 GAIN FLATNESS (dB) 4 5.8 4 3 5.7 3 2 5.6 2 1 5.5 1 0 5.4 0 5.3 -1 -1 -2 5.2 -2 100k 1M 10M 100M 1G 100k 1M 10M 100M 1G 100k 1M 10M 100M FREQUENCY (Hz) FREQUENCY (Hz) FREQUENCY (Hz) LARGE-SIGNAL GAIN FLATNESS **POWER-SUPPLY REJECTION RATIO** vs. FREQUENCY **DIFFERENTIAL GAIN AND PHASE** vs. FREQUENCY 6.2 **DIFFERENTIAL GAIN (%)** 0.3 0 $V_{OUT} = 2V_{P-P}$ 0.2 6.1 ARGE-SIGNAL GAIN FLATNESS (dB) -10 0.1 6.0 0 -20 5.9 -0.1 -0.2 5.8 (dB) -30 -0.3 5.7 PSRR (4th 6th 1st 2nd 3rd 5th (deg) 0.06 -40 5.6 0.04) 30.04 0.02 5.5 -50 0 5.4 0 -0.02 -0.04 -0.06 -60 5.3 5.2 -70 2nd 3rd 4th 5th 6th 1st 100k 100M 10M 1M 10M 1G 1k 10k 100k 1M 100M FREQUENCY (Hz) FREQUENCY (Hz) ALL-HOSTILE CROSSTALK (A TO B ON ANY **OFF-ISOLATION ALL-HOSTILE CROSSTALK (CHANNEL TO CHANNEL) vs. FREQUENCY** vs. FREQUENCY **CHANNEL) vs. FREQUENCY** 0 0 0 -10 -10 -20 -20 -20 -40 -30 OFF-ISOLATION (dB) CROSSTALK (dB) CROSSTALK (dB) -30 -40 -60 -50 -40 -80 -60 -50 -70 -100 -60 -80 -120 -70 -90 -100 -140 -80 10M 100k 1M 100M 100k 1M 10M 100M 1G 10k 100k 10M 100M 1G

1M

FREQUENCY (Hz)

FREQUENCY (Hz)

Typical Operating Characteristics (continued)

 $(V_{CC} = +5V, GND = 0V, V_{\overline{DISABLE}} = +5V, R_L = 150\Omega$ to GND, $C_{IN} = 0.1\mu$ F, $R_{KEYREF} = 6.04k\Omega \pm 1\%$, $T_A = +25^{\circ}$ C, unless otherwise noted.)



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Typical Operating Characteristics (continued)

 $(V_{CC} = +5V, GND = 0V, V_{\overline{DISABLE}} = +5V, R_L = 150\Omega$ to GND, $C_{IN} = 0.1\mu$ F, $R_{KEYREF} = 6.04k\Omega \pm 1\%$, $T_A = +25^{\circ}$ C, unless otherwise noted.)





Pin Description

PIN			FUNCTION	
MAX4028	MAX4029	NAME	FUNCTION	
_	1	IN4A	Amplifier Input 4A	
1	2	IN3A	Amplifier Input 3A	
2	3	IN2A	Amplifier Input 2A	
3	4	IN1A	Amplifier Input 1A	
4	5	A/B	Channel-Select Input. Drive A/\overline{B} high or leave floating to select channel A. Drive A/\overline{B} low to select channel B.	
5	6	KEYREF	Key-Clamp Reference Output. Connect an external resistor from KEYREF to GND to generate the key-clamp voltage.	
6	7	IN1B	Amplifier Input 1B	
7	8	IN2B	Amplifier Input 2B	
8	9	IN3B	Amplifier Input 3B	
_	10	IN4B	Amplifier Input 4B	
_	11	OUT4	Amplifier Output 4	
9	12	CLAMP/KEY_3	Output 3 Clamp or Key-Clamp Input. Drive CLAMP/KEY_3 high to clamp OUT3. Drive CLAMP/KEY_3 low to key clamp OUT3.	
10	13	GND	Ground	
11	14	OUT3	Amplifier Output 3	
12	15	CLAMP/KEY_2	Output 2 Clamp or Key-Clamp Input. Drive CLAMP/KEY_2 high to clamp OUT2. Drive CLAMP/KEY_2 low to key clamp OUT2.	
13	16	OUT2	Amplifier Output 2	
14	17	Vcc	Power-Supply Voltage. Bypass V_{CC} to GND with 0.1 μF and 0.01 μF capacitors as close to the pin as possible.	

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Pin Description (continued)

P	IN	NAME	FUNCTION
MAX4028	MAX4029	NAME	FUNCTION
15 18 OUT1 Amplifier Output 1		Amplifier Output 1	
16	19	9 DISABLE Disable Input. Pull DISABLE high for normal operation. Drive DISABLE lov all outputs.	
20 CLAMP/KEY_4 Output 4 Clamp or Key-Clamp Input. Drive CLAMP/KEY_4 high to clamp Drive CLAMP/KEY_4 low to key clamp OUT4.		Output 4 Clamp or Key-Clamp Input. Drive CLAMP/KEY_4 high to clamp OUT4. Drive CLAMP/KEY_4 low to key clamp OUT4.	



Figure 1. MAX4029 Functional Diagram

_Detailed Description

The MAX4028/MAX4029 are 5V. triple/quad. 2:1 voltagefeedback multiplexer-amplifiers with input clamps and a fixed gain of +2V/V (6dB). Channel 1 (IN1A and IN1B) inputs are clamped to the video sync tip of the input IN1_ channel, while the remaining inputs can be clamped to either the video sync tip of the respective input channel (IN_A and IN_B) or the video sync of channel 1 (IN1_). The latter is referred to as a key clamp and is pin selectable. Selectable clamp/keyclamp inputs and fixed-gain video output buffers make the MAX4028/MAX4029 ideal for video-source switching applications such as automotive entertainment systems, video projectors, and displays/TVs. Both devices have 20ns channel switching times and low ±10mVP-P switching transients, making them ideal for both high-speed video switching applications such as OSD insertion.

The MAX4028/MAX4029 have a -3dB large-signal ($2V_{P-P}$) bandwidth of 130MHz, a -3dB small-signal bandwidth of 210MHz, and a 300V/µs slew rate. Low differential gain and phase errors of 0.2% and 0.4°, respectively, make these devices ideal for broadcast video applications.

Sync Tip and Key Clamps

The MAX4028/MAX4029 have AC-coupled inputs, with either a sync tip or key clamp to provide bias for the video signal. Channel 1 of the MAX4028/MAX4029 always has a sync tip clamp at the input, while the remaining channels are selectable as either sync tip or key clamps to accommodate the various video waveforms (see the *Clamp/Key-Clamp Settings for Video Formats* section). The value of the sync-tip clamp voltage is set internally for the lowest value, consistent with linear operation, and cannot be adjusted. The key-clamp voltage is adjustable, to compensate for variations in the voltage between component video inputs such as Linear RGB, YPbPr, and Y-C, by varying R_{KEYREF}. The keyclamp voltage can be computed from:

 $V_{Key-Clamp} = 0.40 + 2000/[(5000 \times R_{KEYREF}) / (5000 + R_{KEYREF})]$

Therefore, a $6k\Omega$ resistor will produce a 1.13V keyclamp voltage as shown in Figure 2. The clamp voltage (V_{CLAMP}) is measured at the output; the voltage at the input is V_{CLAMP} (sync tip or key clamp) divided by the gain (+2V/V) + V_{BE}.

In order for these clamps (sync tip or key) to work properly, the input must be coupled with a 0.1μ F capacitor (typ) with low leakage (<1 μ A to 2 μ A, max). Without proper coupling, the clamp voltage will change during the horizontal line time causing the "black level" to vary, changing the image brightness from left to right on the display. In addi-



Figure 2. Key-Clamp Reference Voltage vs. RKEYREF

 Table 1. MAX4028 Clamp Settings for Video Formats

INPUT	FORMAT	CLAMP/KEY
1	Cvbs1	Clamp
2	Cvbs2	Clamp
3	Cvbs3	Clamp

INPUT	FORMAT	CLAMP/KEY
1	G'	Clamp
2	B'	Clamp
3	R'	Clamp

R, G, B have sync on all.

INPUT	FORMAT	CLAMP/KEY
1	Gs	Clamp
2	В	Key
3	R	Key

Gs, B, R have sync only on Green.

tion to the capacitor, a low resistance ($\leq 75\Omega$) is required on the source side to return the capacitor to ground. The clamps used here are active devices with the coupling capacitor serving two functions; first, as a charge reservoir to maintain the clamp voltage, and second, as the compensation capacitor for the clamp itself. If an input is not used, it must be terminated to avoid causing oscillations that could couple with another input.

In general, a sync-tip clamp is used for composite video (Cvbs), gamma-corrected primaries (R'G'B'), and the luma signal (Y) in S-video. A key clamp is preferred for component color difference signals (Pb and Pr), linear primaries (RGB in PCs), and chroma (C) in S-video. The rule is to sync tip clamp a signal if sync is present and key clamp all others. Several examples are given in the *Clamp/Key-Clamp Settings for Video Formats* section.

Clamp/Key-Clamp Settings for Video Formats

Tables 1 and 2 provide the clamp settings on the MAX4028/MAX4029 to interface with various video formats.

Low-Power, High-Impedance Disable Mode All parts feature a low-power, high-impedance disable mode that is activated by driving the DISABLE input low. Placing the amplifier in disable mode reduces the quiescent supply current and places the output impedance at $2k\Omega$ typically. Multiple devices can be paralleled to construct larger switch matrices by connecting the outputs of several devices together and disabling

all but one of the paralleled amplifiers' outputs.

INPUT	FORMAT	CLAMP/KEY
1	Y	Clamp
2	С	Key
3	Cvbs	Clamp

INPUT	FORMAT	CLAMP/KEY
1	Y	Clamp
2	Pb	Key
3	Pr	Key

M/IXI/M

Table 2. MAX4029 Clamp Settings for Video Formats

INPUT	FORMAT	CLAMP/KEY
1	Cvbs1	Clamp
2	Cvbs2	Clamp
3	Cvbs3	Clamp
4	Cvbs4	Clamp

INPUT	FORMAT	CLAMP/KEY
1	H-Sync	Clamp
2	G	Key
3	В	Key
4	R	Key

R, G, B have sync on none.

INPUT	FORMAT	CLAMP/KEY
1	Y	Clamp
2	С	Key
3	Cvbs	Clamp
4	Cvbs	Clamp

The MAX4028/MAX4029 have a fixed gain of +2V/V that is internally set with two $1k\Omega$ thin-film resistors. The impedance of the internal feedback resistors must be taken into account when operating multiple MAX4028/MAX4029s in large multiplexer applications.

Applications Information

Video Line Driver

The MAX4028/MAX4029 are well suited to drive coaxial transmission lines when the cable is terminated at both ends, as shown in Figure 3, where the fixed gain of +2V/V compensates for the loss in the resistors, R_T.

Driving Capacitive Loads

A correctly terminated transmission line is purely resistive and presents no capacitive load to the amplifier. Reactive loads decrease phase margin and may produce excessive ringing and oscillation.

Another concern when driving capacitive loads is the amplifier's output impedance, which appears inductive at high frequencies. This inductance forms an L-C reso-

INPUT	FORMAT	CLAMP/KEY
1	Gs	Clamp
2	R	Key
3	В	Key
4	Cvbs	Clamp

Gs, B, R have sync only on Green.

INPUT	FORMAT	CLAMP/KEY
1	Y	Clamp
2	Pr	Key
3	Pb	Key
4	Cvbs	Clamp

INPUT	FORMAT	CLAMP/KEY
1	Cvbs	Clamp
2	G'	Clamp
3	B'	Clamp
4	R'	Clamp

R, G, B have sync on all.



Figure 3. Video Line Driver

nant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's phase margin.

///XI//



Figure 4. Small-Signal Gain vs. Frequency with Capacitive Load and No Isolation Resistor



Figure 5. Using an Isolation Resistor (RISO) for a High-Capacitive Load

Although the MAX4028/MAX4029 are optimized for AC performance and are not designed to drive highly capacitive loads, they are capable of driving up to 15pF without oscillations. However, some peaking may occur in the frequency domain (Figure 4). To drive larger capacitive loads or to reduce ringing, add an isolation resistor between the amplifier's output and the load (Figure 5). The value of RISO depends on the circuit's



Figure 6. Optimal Isolation Resistance vs. Capacitive Load

gain (+2V/V) and the capacitive load (Figure 6). Also note that the isolation resistor forms a divider that decreases the voltage delivered to the load.

Layout and Power-Supply Bypassing

The MAX4028/MAX4029 have high bandwidths and consequently require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. Whether or not a constant-impedance board is used, it is best to observe the following guidelines when designing the board:

- 1) Do not use wire-wrapped boards or breadboards.
- Do not use IC sockets; they increase parasitic capacitance and inductance.
- 3) Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- 4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
- 5) Use surface-mount components. They generally have shorter bodies and lower parasitic reactance, yielding better high-frequency performance than through-hole components.



MAX4028/MAX4029

The bypass capacitors should include a 0.1μ F, ceramic surface-mount capacitor between V_{CC} and the ground plane, located as close to the package as possible. Optionally, place a 10 μ F capacitor at the power supply's point-of-entry to the PC board to ensure the integrity of incoming supplies. The power-supply traces should lead

directly from the capacitor to the $V_{CC}\ pin.$ To minimize parasitic inductance, keep PC traces short and use surface-mount components.

If input termination resistors and output back-termination resistors are used, they should be surface-mount types, and should be placed as close to the IC pins as possible.



Chip Information

TRANSISTOR COUNT: 1032 PROCESS: Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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