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Kind regards,

Team Nexperia



BUK7E4R3-75C

N-channel TrenchMOS standard level FET

Rev. 02 — 19 April 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	75	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 4	[1][2] -	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	333	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 7 ; see Figure 8	-	3.7	4.3	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$; $V_{sup} \leq 75\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	630	mJ

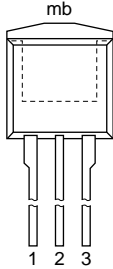
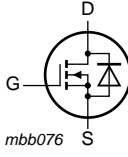
[1] Continuous current is limited by package.

[2] Refer to document 9397 750 12572 for further information.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7E4R3-75C	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	75	V	
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	75	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 ; see Figure 4	[1][2]	-	100	A
		$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 ; see Figure 4	[1][2]	-	100	A
			[3][2]	-	192	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see Figure 4	-	769	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	333	W	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[2][1]	-	100	A
			[2][3]	-	192	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	769	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}; V_{sup} \leq 75\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	630	mJ	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[4][5][6][7]	-	mJ	

[1] Continuous current is limited by package.

[2] Refer to document 9397 750 12572 for further information.

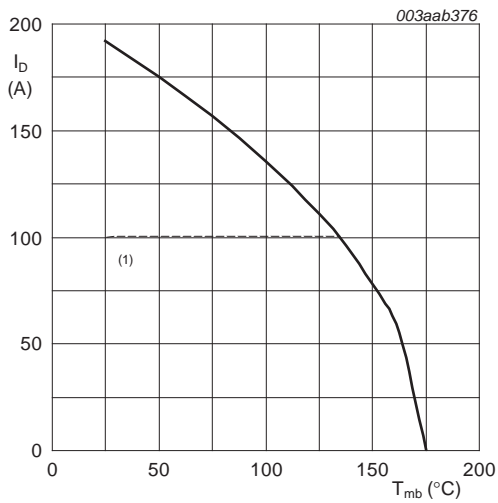
[3] Current is limited by power dissipation chip rating.

[4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

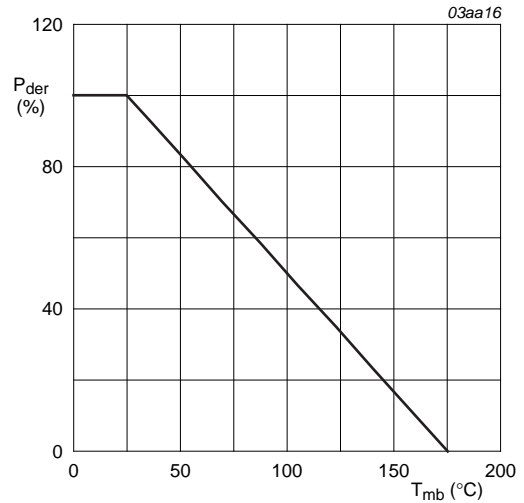
[6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[7] Refer to application note AN10273 for further information.



$V_{GS} \geq 10\text{ V}$
 (1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

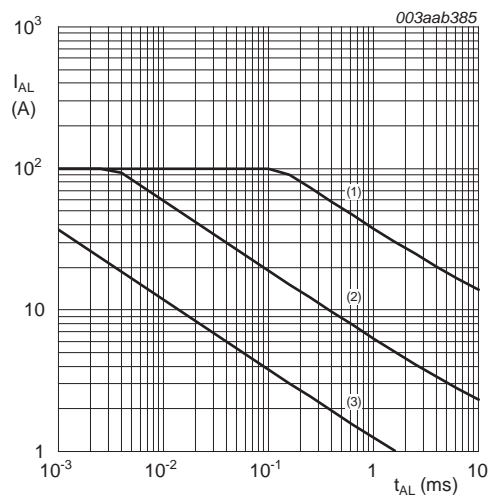
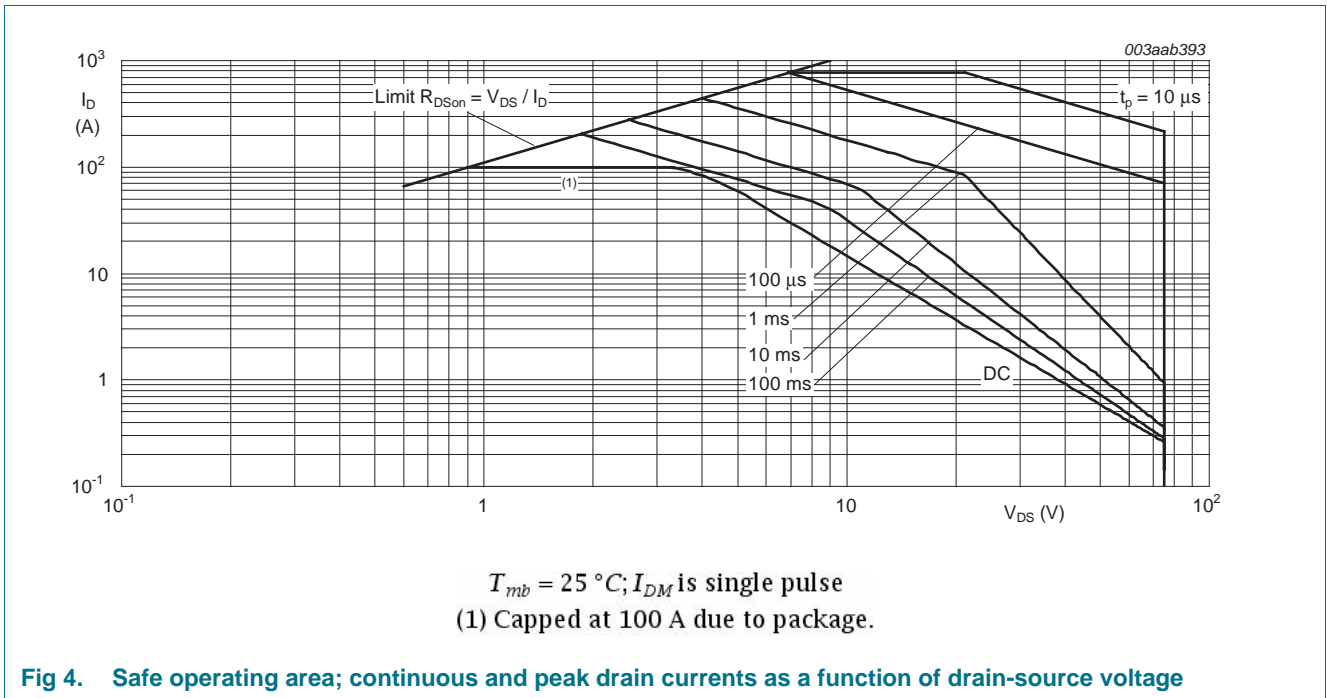


Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.



5. Thermal characteristics

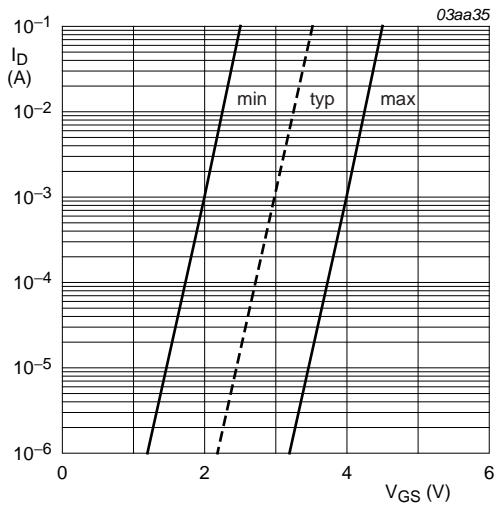
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	50	-	K/W

6. Characteristics

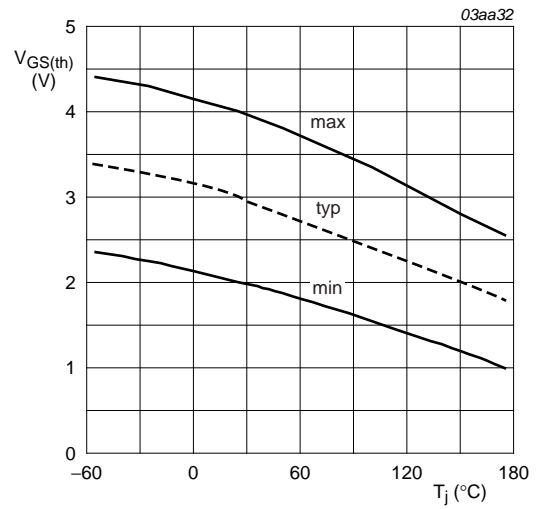
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	70	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 5 ; see Figure 6	-	-	4.4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 5 ; see Figure 6	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 5 ; see Figure 6	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$; see Figure 7 ; see Figure 8	-	-	9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 7 ; see Figure 8	-	3.7	4.3	m Ω
I_{DSS}	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 9	-	142	-	nC
Q_{GS}	gate-source charge		-	36	-	nC
Q_{GD}	gate-drain charge		-	67	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$; see Figure 10	-	8744	11659	pF
C_{oss}	output capacitance		-	923	1108	pF
C_{rss}	reverse transfer capacitance		-	579	793	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V}$; $R_{G(ext)} = 10 \text{ } \Omega$	-	61	-	ns
t_r	rise time		-	100	-	ns
$t_{d(off)}$	turn-off delay time		-	194	-	ns
t_f	fall time		-	90	-	ns
L_D	internal drain inductance	from contact screw on mounting base to centre of die	-	3.5	-	nH
		from drain lead 6mm from package to centre of die	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$; see Figure 11	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$	-	83	-	ns
Q_r	recovered charge		-	155	-	nC



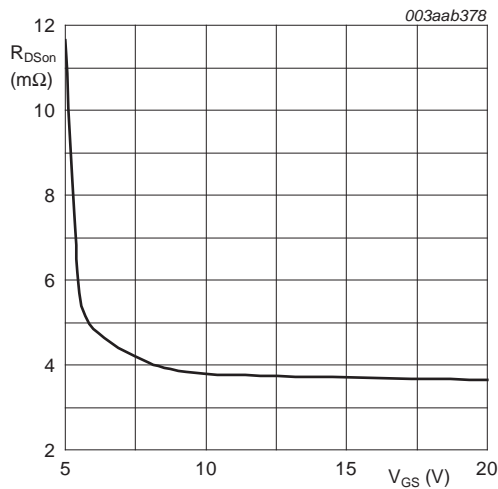
$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

Fig 5. Sub-threshold drain current as a function of gate-source voltage



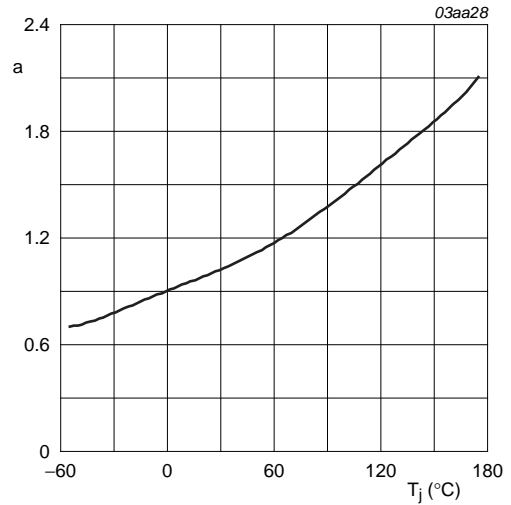
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 6. Gate-source threshold voltage as a function of junction temperature



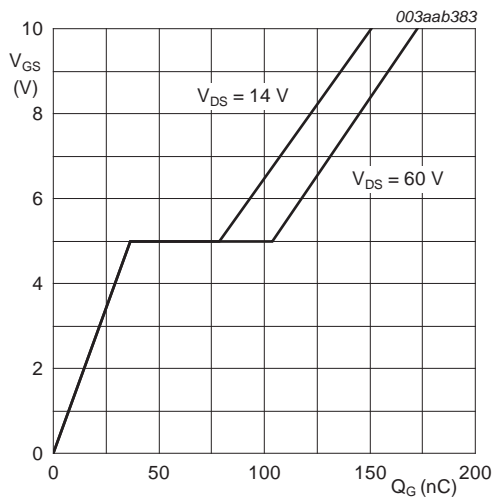
$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$

Fig 7. Drain source on-state resistance as a function of gate-source voltage; typical values



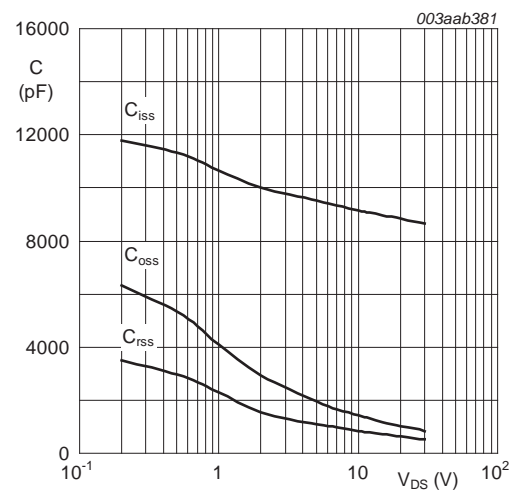
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



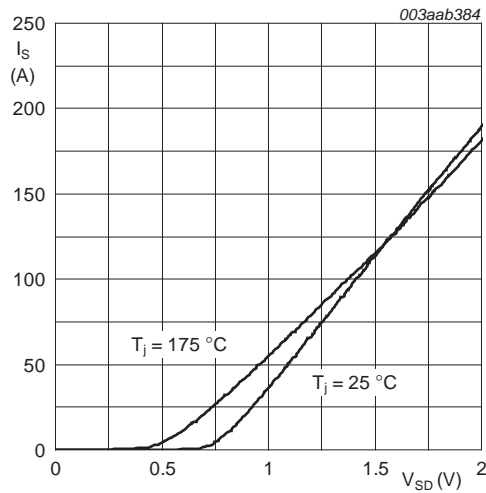
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 9. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 11. Source current as a function of source-drain diode; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

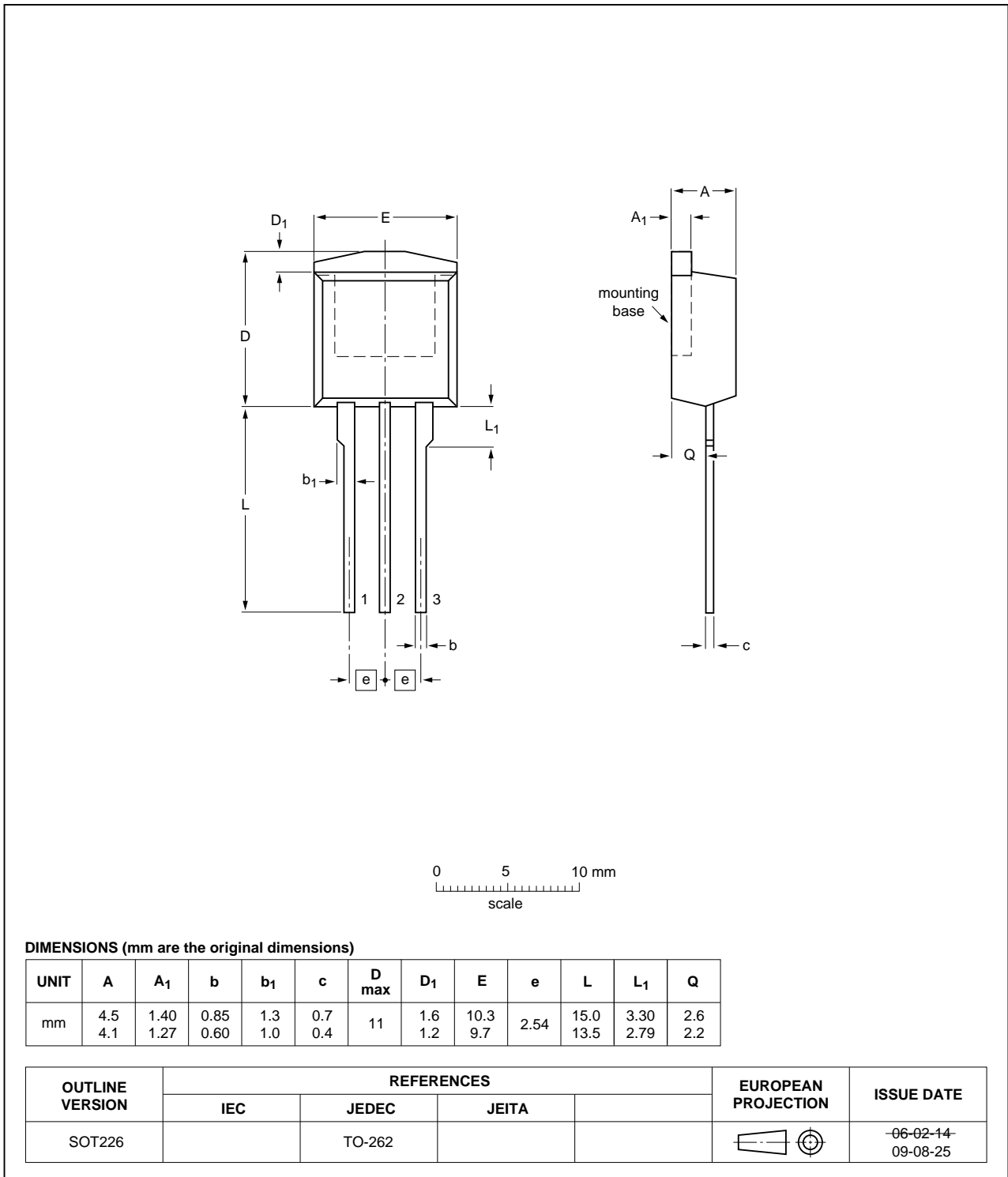


Fig 12. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7E4R3-75C v.2	20110419	Product data sheet	-	BUK75_7E4R3-75C v.1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Type number BUK7E4R3-75C separated from data sheet BUK75_7E4R3-75C v.1.			
BUK75_7E4R3-75C v.1	20060810	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 19 April 2011

Document identifier: BUK7E4R3-75C