THCV226

V-by-One® HS High-speed Video Data Receiver

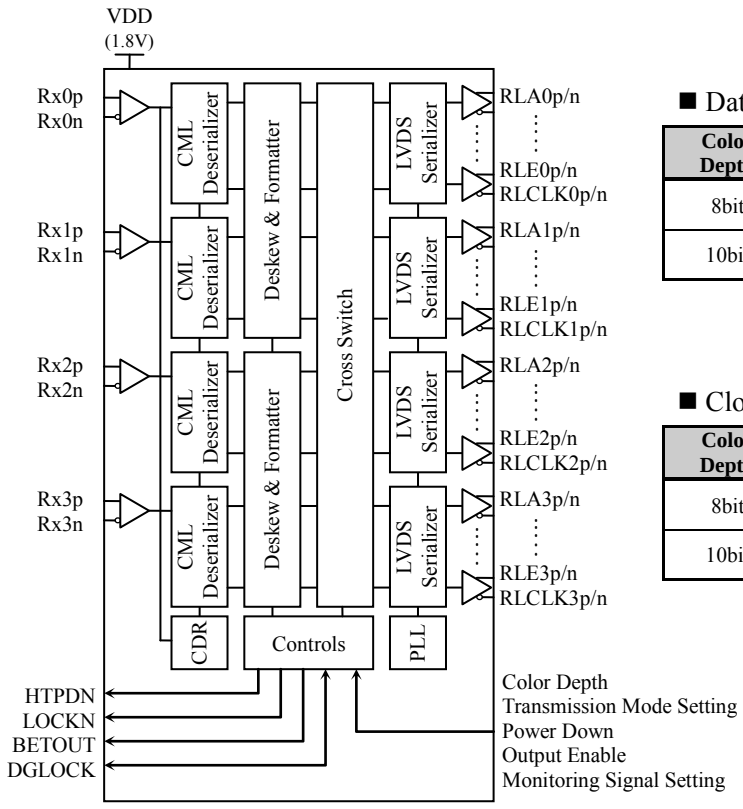
General Description

THCV226 is designed to support video data transmission between the host and display. This chip can receive 32bit video data and 3bit control data via four differential pairs of V-by-One® HS lanes. This chip in TQFP package supports the video data transmission up to 1080p/10b/120Hz. The maximum serial data rate is 3.4Gbps/lane.

Features

- Normal / High-speed LVDS output selectable
- 1.8V single power supply
- Color depth selectable: 8/10 bits per colors
- Crossing / Distribution mode selectable
- Monitoring signal function
- 1.8V LVTTL I/O interface
- Package: 128pin 0.4mm-pitch TQFP (16mm x 16mm)
- Wide frequency range
- AC coupling for CML inputs
- CDR requires no external frequency reference
- Supports Spread Spectrum Clocking tolerance with up to 30kHz/±0.5%(center spread)
- V-by-One® HS standard compliant
- PLL requires no external components
- Power down / Output enable mode

Block Diagram



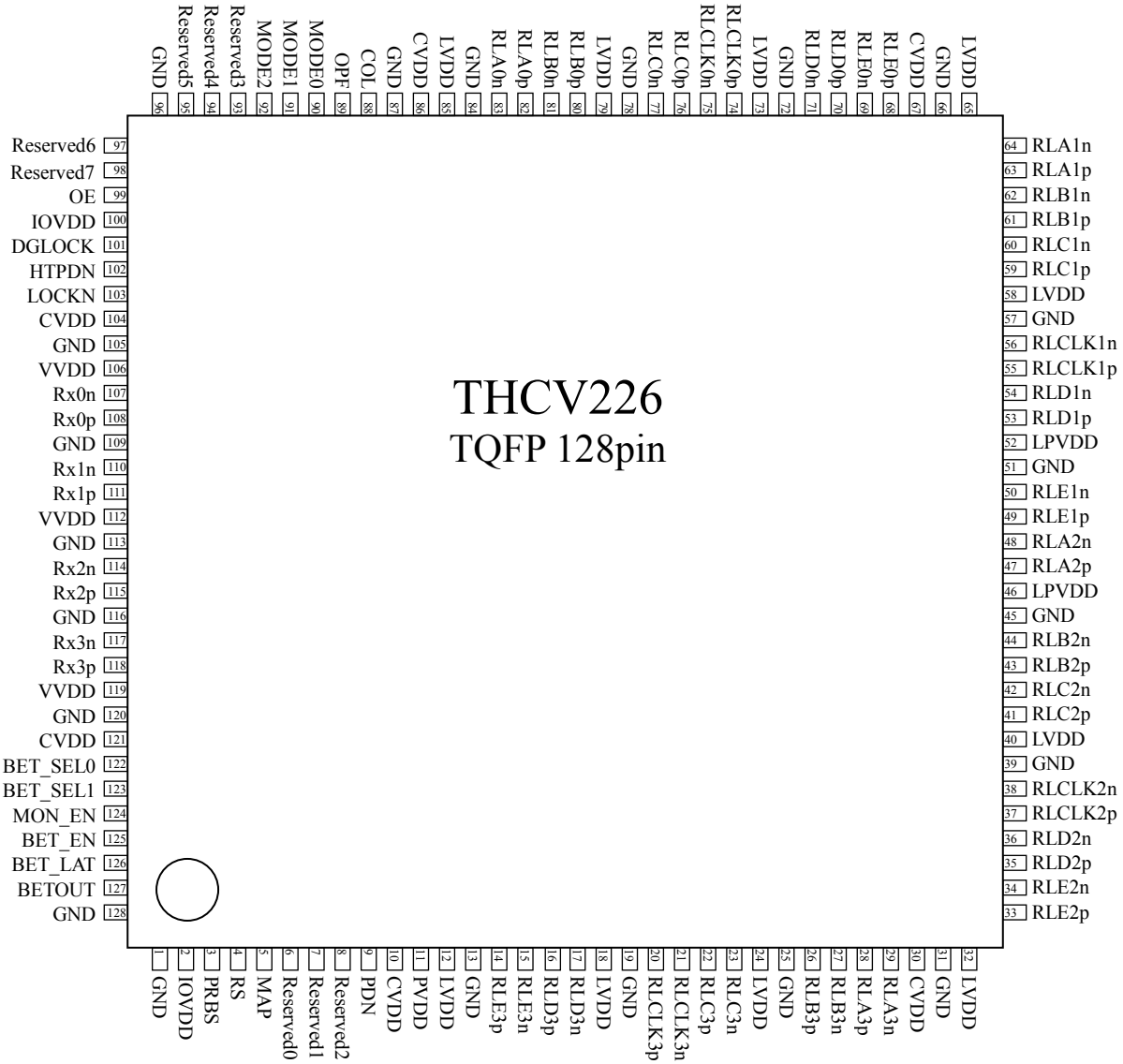
■ Data Transmission Rate of CML Input

Color Depth	Normal Speed LVDS Mode	High-Speed LVDS Mode
8bit	1.2 to 2.7Gbps	1.2 to 2.36Gbps
10bit	1.6 to 3.4Gbps	1.6 to 3.14Gbps

■ Clock Frequency of LVDS Output

Color Depth	Normal Speed LVDS Mode	High-Speed LVDS Mode
8bit	40 to 90MHz	80 to 157MHz
10bit	40 to 85MHz	80 to 157MHz

PIN Configuration



PIN Description

PIN Name	PIN No	Type	Description
Rx0n , Rx0p	107, 108	CI	CML Data Input
Rx1n , Rx1p	110, 111	CI	CML Data Input
Rx2n , Rx2p	114, 115	CI	CML Data Input
Rx3n , Rx3p	117, 118	CI	CML Data Input
RLA0n , RLA0p	83, 82	LO	LVDS Data Output
RLB0n , RLB0p	81, 80	LO	LVDS Data Output
RLC0n , RLC0p	77, 76	LO	LVDS Data Output
RLCLK0n , RLCLK0p	75, 74	LO	LVDS Data Output
RLD0n , RLD0p	71, 70	LO	LVDS Data Output
RLE0n , RLE0p	69, 68	LO	LVDS Data Output
RLA1n , RLA1p	64, 63	LO	LVDS Data Output
RLB1n , RLB1p	62, 61	LO	LVDS Data Output
RLC1n , RLC1p	60, 59	LO	LVDS Data Output
RLCLK1n , RLCLK1p	56, 55	LO	LVDS Data Output
RLD1n , RLD1p	54, 53	LO	LVDS Data Output
RLE1n , RLE1p	50, 49	LO	LVDS Data Output
RLA2n , RLA2p	48, 47	LO	LVDS Data Output
RLB2n , RLB2p	44, 43	LO	LVDS Data Output
RLC2n , RLC2p	42, 41	LO	LVDS Data Output
RLCLK2n , RLCLK2p	38, 37	LO	LVDS Data Output
RLD2n , RLD2p	36, 35	LO	LVDS Data Output
RLE2n , RLE2p	34, 33	LO	LVDS Data Output
RLA3n , RLA3p	29, 28	LO	LVDS Data Output
RLB3n , RLB3p	27, 26	LO	LVDS Data Output
RLC3n , RLC3p	23, 22	LO	LVDS Data Output
RLCLK3n , RLCLK3p	21, 20	LO	LVDS Data Output
RLD3n , RLD3p	17, 16	LO	LVDS Data Output
RLE3n , RLE3p	15, 14	LO	LVDS Data Output
DGLOCK	101	BI	Connect all DGLOCK pins in multiple-chip configuration. Must be left OPEN for single-chip configuration
HTPDN	102	OD	Hot plug detect output Must be connected to Tx HTPDN with a 10KΩ pull-up resistor
LOCKN	103	OD	Lock detect output Must be connected to Tx LOCKN with a 10KΩ pull-up resistor
COL	88	I	Color depth select 1 : 10bit mode 0 : 8bit mode
OPF	89	I	Output Pattern at CDR Fail Condition (LOCKN=1) 1 : LVDS output Low data 0 : LVDS output Hi-Z data
MODE2,1,0	92,91,90	I	Input / Output mode select
OE	99	I	LVDS Output Enable 1 : Normal Operation 0 : Output Disable
BET_SEL1,0	123, 122	I	Monitoring pin select

BET_EN	125	I	Field-BET enable 1 : Enable 0 : Normal operation
BET_LAT	126	I	Latch select input under Field BET operation 1 : Latched result output 0 : Reset latched result
MON_EN	124	I	Monitoring mode enable 1 : Monitoring enable 0 : Monitoring disable
PRBS	3	I	Must be tied to GND or used for Monitoring Signal Function, refer to Table10.
RS	4	I	LVDS swing level select 1 : Normal swing (350mV) 0 : Reduced swing (200mV)
MAP	5	I	LVDS output format select 1 : JEIDA format 0 : VESA format
PDN	9	I	Power down 1 : Normal operation 0 : Power down operation
BETOUT	127	O	Field BET result output
Reserved 0,1,2,3,4,5	6, 7, 8, 93, 94, 95	I	Must be tied to GND
Reserved 6,7	97, 98	O	Must be open
CVDD	10, 30, 67, 86, 104, 121	PWR	1.8V power supply for Logic block
VVDD	106, 112, 119	PWR	1.8V power supply for V-by-One® HS block
LVDD	12, 18, 24, 32, 40, 58, 65, 73, 79, 85	PWR	1.8V power supply for LVDS block
PVDD	11	PWR	1.8V power supply for PLL block
LPVDD	46, 52	PWR	1.8V power supply for LVDS analog block
IOVDD	2, 100,	PWR	1.8V power supply for LVTTL I/O buffer
GND	1, 13, 19, 25, 31, 39, 45, 51, 57, 66, 72, 78, 84, 87, 96, 105, 109, 113, 116, 120, 128	GND	Ground

CI : CML Input buffer , LO : LVDS Output buffer , BI : LVTTL Bi-directional buffer
I : LVTTL Input buffer , O : LVTTL Output buffer , OD : Open Drain buffer
PWR : 1.8V Power supply , GND : Ground

Functional Description

Functional Overview

With V-by-One® HS's proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV226 enables the transmission of 8 or 10-bit video data, 2-bit synchronizing control data of HSYNC, VSYNC, and Data Enable(DE), by a pair cable with minimal external components.

THCV226 automatically extracts the clock from the incoming data streams and converts the serial data into video data with DE being high or synchronizing control data with DE being low, recognizing which type of serial data is being sent by the transmitter. Also, THCV226 outputs the recovered data in the LVDS data format.

THCV226 can operate for a wide range of a serial bit rate from 1.2Gbps to 3.4Gbps. It is unnecessary to use any external frequency reference, such as a crystal oscillator.

Data Enable Requirement (DE)

There are some requirements for DE signal as described in Figure1 and Figure2.
If DE=Low, control data of same cycle and particular assigned data bit 'CTL' except the first and last pixel are transmitted. Otherwise video data is transmitted during DE=High.
Control data from source device in DE=High period is previous data of DE transition. See Figure2.
The length of DE being low and high must be at least 8 clock cycles long, as described in Figure17 and Table17.
DE must be toggled as High -> Low -> High at regular interval.

CTL Bit Transmission

There is particular assigned data bit 'CTL' which can be transmitted at blanking period except the first and the last pixel on DE=Low.

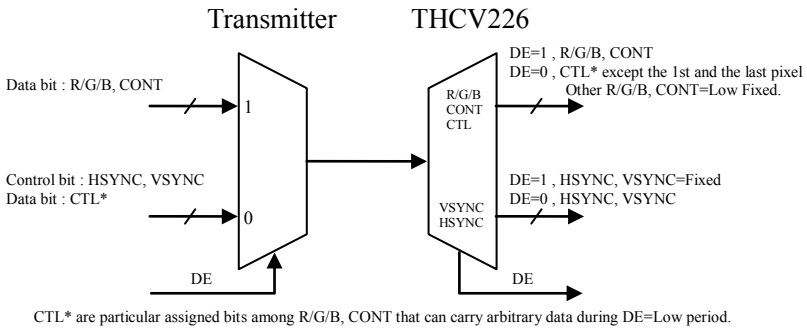


Figure 1. Conceptual Diagram of Basic Operation of Chipset

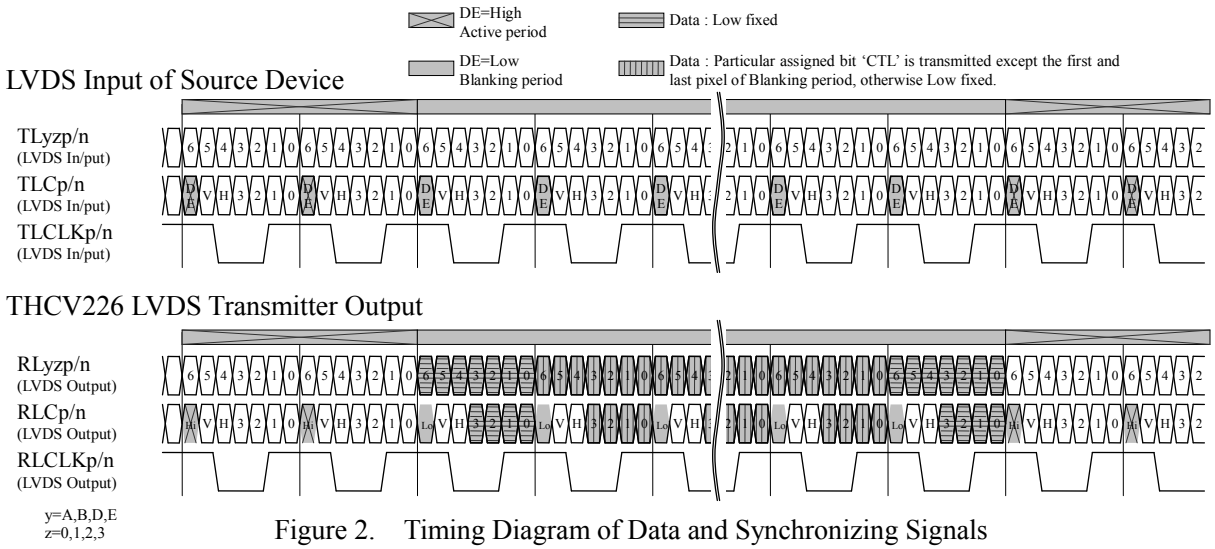


Figure 2. Timing Diagram of Data and Synchronizing Signals

Color Depth Mode Function

COL	Operation Mode
1	10-bit R/G/B data (4byte mode for V-by-One® HS Standard)
0	8-bit R/G/B data (3byte mode for V-by-One® HS Standard)

Table 1. Color Depth Mode Select

Transmission Mode Select

MODE 2, 1, 0	COL	V-by-One HS	LVDS	Operation Mode
111	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Distribution mode2
	0	40 – 78.5MHz	80 – 157MHz	
110	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Distribution mode2
	0	40 – 90MHz	40 – 90MHz	
101	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Distribution mode1
	0	40 – 78.5MHz	80 – 157MHz	
100	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Distribution mode1
	0	40 – 90MHz	40 – 90MHz	
011	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Crossing Mode
	0	40 – 78.5MHz	80 – 157MHz	
010	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Crossing mode
	0	40 – 90MHz	40 – 90MHz	
001	1	40 – 78.5MHz	80 – 157MHz	HSLVDS mode
	0	40 – 78.5MHz	80 – 157MHz	
000	1	40 – 85MHz	40 – 85MHz	Normal LVDS mode
	0	40 – 90MHz	40 – 90MHz	

Table 2. Transmission Mode Select

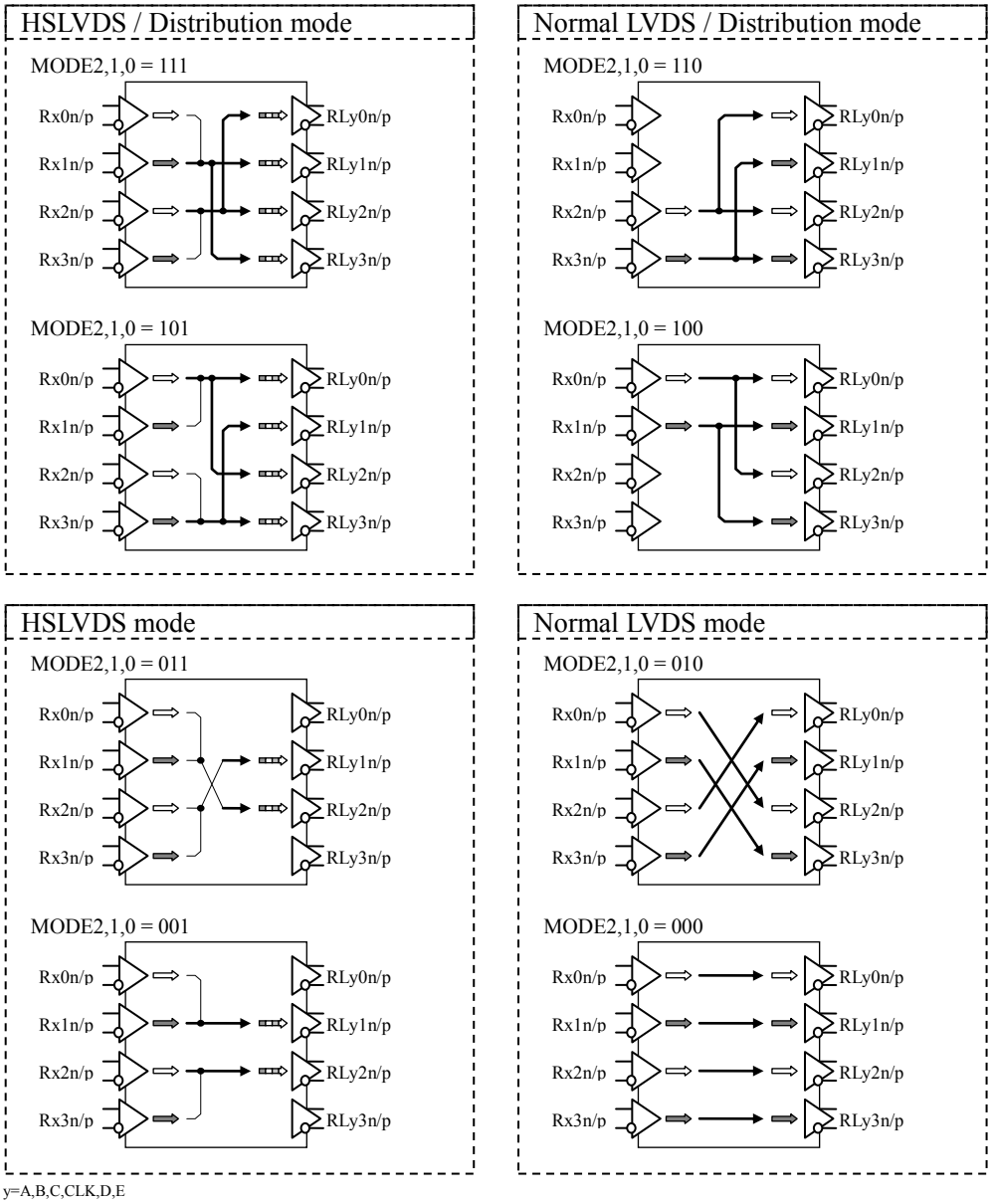


Figure 3. Transmission Mode Select Diagram

Power Down Mode

PDN	Operation
1	Normal operation
0	Power down operation

Table 3. Power Down Mode

Hot-plug and Lock Detect Function

HTPDN and LOCKN are both open drain outputs from THCV226. Pull-up resistors must be placed at V-by-One® HS transmitter side. See Figure.4 and 5.

If THCV226 is not active (power down mode (PDN=0) or powered off), HTPDN is open. Otherwise, HTPDN is pulled down by THCV226.

HTPDN at V-by-One® HS transmitter side is High when THCV226 is not active or the receiver board is not connected. Then V-by-One® HS transmitter side enters into the power down mode. When HTPDN transits from High to Low, V-by-One® HS transmitter starts up and transmits training pattern for link training.

LOCKN indicates whether THCV226 is in CDR state or not. If THCV226 is in the CDR unlock state, LOCKN is open. Otherwise (in the CDR lock state), it is pulled down by THCV226.

V-by-One® HS transmitter side keeps transmitting training pattern until LOCKN transition to Low. After training is done, THCV226 sinks current, and LOCKN turns to Low. Then V-by-One® HS transmitter side starts transmitting normal video pattern.

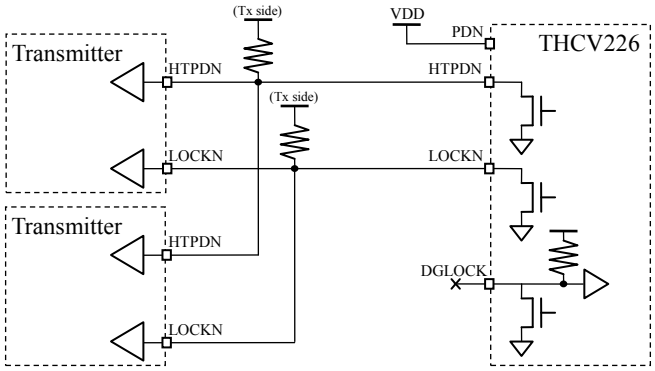


Figure 4. HTPDN and LOCKN Scheme

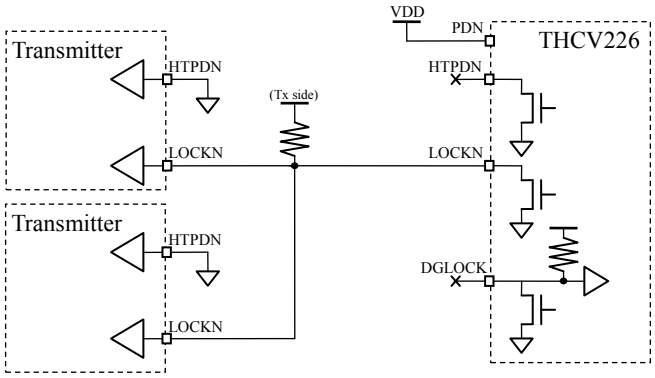


Figure 5. HTPDN and LOCKN Scheme without HTPDN Connection

Multiple-chip Configuration

In order to reduce the number of cables needed for HTPDN and LOCKN in multiple-chip configuration, THCV226 is equipped with the DGLOCK pin. When all the DGLOCK pins are connected as in Figure 6 , the connected Rx chips can share the CDR lock status via DGLOCK, making all the Rx chips in the same operation status.

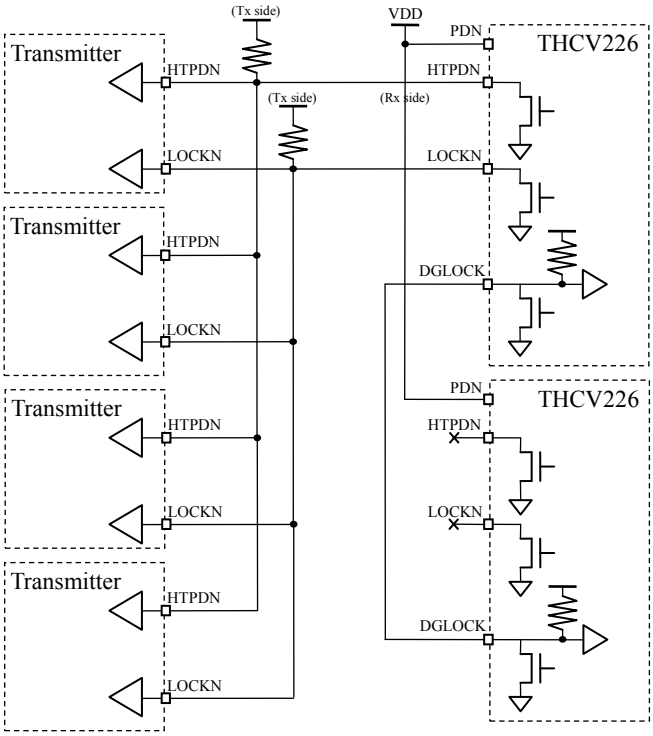


Figure 6. Usage of DGLOCK in Multiple-Rx Configuration

Field BET Operation

In order to help to debug high-speed serial links of CML lines, THCV226 has an operation mode acted as the bit error tester (Field BET). In the Field BET mode, the on-chip pattern generator on V-by-One® HS transmitter side is enabled and generates a test pattern. THCV217, which is an example of Tx device, has this function mode. In this mode, THCV217 internally generates the test pattern, encodes the data according to the 8b10b protocol, scrambles, and then serializes onto the CML high-speed lines.
THCV226 receives the data stream and checks whether the sampled data has bit error.

"Field BET" mode of THCV226 is activated by setting BET_EN=1.

As for THCV226, when the internal test pattern check circuit is enabled, the pattern check result can be monitored at the BETOUT pin. The BETOUT pin goes Low whenever bit errors occur and stays High when there is no bit error. Please refer to Figure 7 and Figure 8.

Table 5 shows possible combination of Tx and Rx for normal and Field BET operation.

BETOUT	Result
L	Bit error occurred
H	No error

Table 4. Field BET Result

THCV217	THCV226				Condition	
BET	**BET_EN**	**BET_LAT**	**BET_SEL1**	**BET_SEL0**	**Operation**	**Output Latch Select**
0	0	0	-	-	Normal Operation	-
		1	-	-	Forbidden	-
0	1	-	-	-	Forbidden	-
1	0	-	-	-	Forbidden	-
1	1	0	0	0	Field BET Operation (Lane0)	Reset latched result
		1				Latched result
		0	0	1	Field BET Operation (Lane1)	Reset latched result
		1				Latched result
		0	1	0	Field BET Operation (Lane2)	Reset latched result
		1				Latched result
		0	1	1	Field BET Operation (Lane3)	Reset latched result
		1				Latched result

Table 5. Field BET Operation

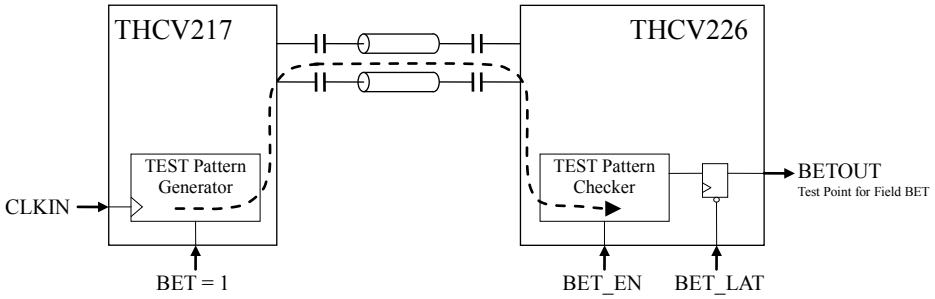


Figure 7. Field BET Configuration

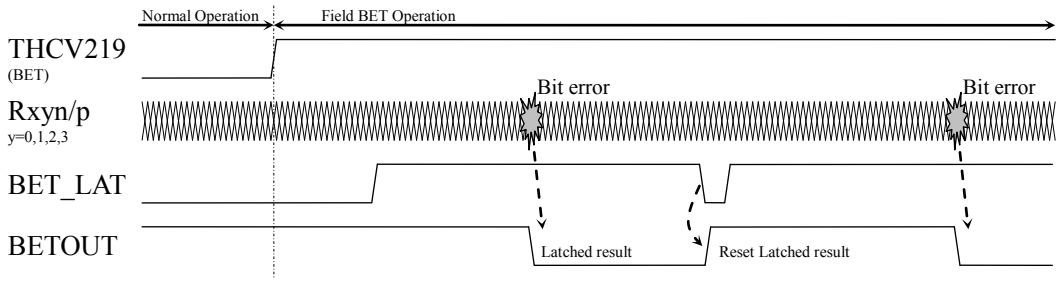


Figure 8. Relationship between Bit Error and BETOUT

LVDS Reduced Swing Output Function

RS pin controls LVDS output swing level.

RS	Output Swing Level
0	Reduced Swing Level (200mV typical)
1	Normal Swing Level (350mV typical)

Table 6. LVDS Output Level Select

LVDS Output Enable Function

By setting the OE and OPF pins, the following output enable function can be selected.

In output disable condition, all the outputs take low fixed data or High-Z except for HTPDN, LOCKN and DGLOCK.

LOCKN	OE	OPF	LVDS Outputs	
			Status	Output Condition
H	1	1	Output Enable	Low Fixed Data
		0		Hi-Z
	0	1	Output Disable	Low Fixed Data
		0		Hi-Z
L	1	1	Output Enable	Normal Data
		0		
	0	1	Output Disable	Low Fixed Data
		0		Hi-Z

Table 7. LVDS Output Enable Function

LVDS Data Mapping

LVDS data (video data, control data, DE) are mapped as Figure 9. RLC[6] is special bit for DE (data enable). RLC[5:4] are for control data bits, and the other bits are for video data. Also there are special assigned bits, 'CTL' transmitted under DE=0 condition.

The number of LVDS channels depends on color depth mode, COL.

RLD[6] is not available at COL=0, 8-bit color depth mode.

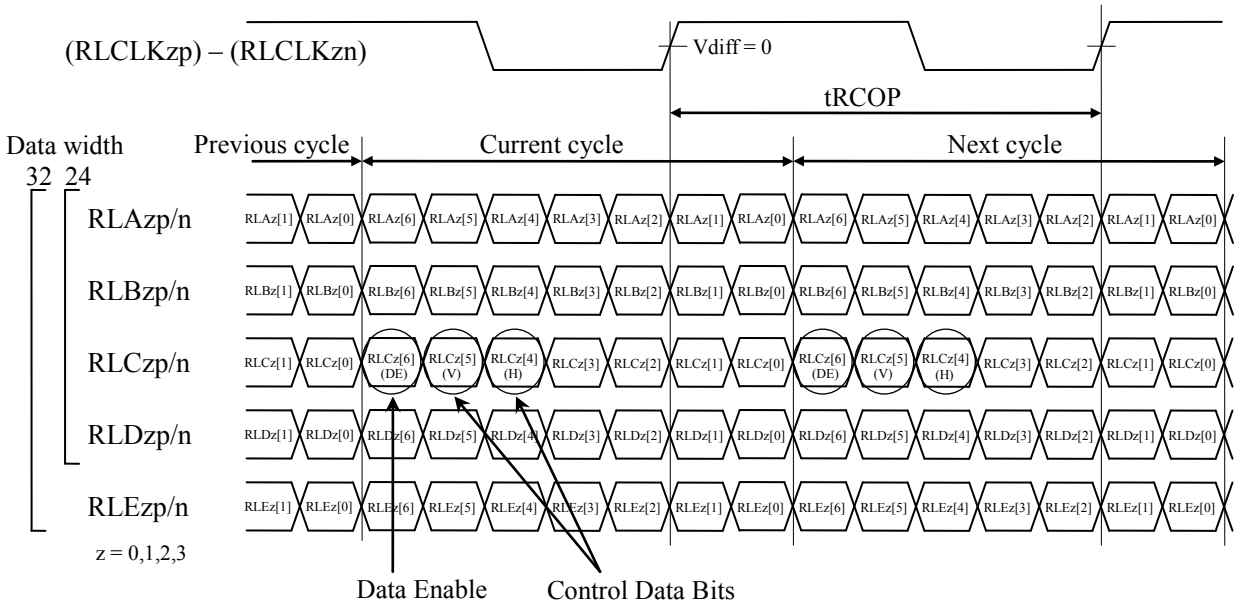


Figure 9. LVDS Output Switching Timing Diagram

THCV226 Output	COL		Comment
	0 (8bit)	1 (10bit)	
RLAz[0]	R[2]	R[4]	Data bit
RLAz[1]	R[3]	R[5]	Data bit
RLAz[2]	R[4]	R[6]	Data bit
RLAz[3]	R[5]	R[7]	Data bit
RLAz[4]	R[6]	R[8]	Data bit
RLAz[5]	R[7]	R[9]	Data bit
RLAz[6]	G[2]	G[4]	Data bit
RLBz[0]	G[3]	G[5]	Data bit
RLBz[1]	G[4]	G[6]	Data bit
RLBz[2]	G[5]	G[7]	Data bit
RLBz[3]	G[6]	G[8]	Data bit
RLBz[4]	G[7]	G[9]	Data bit
RLBz[5]	B[2]*2	B[4]*2	Data bit
RLBz[6]	B[3]*2	B[5]*2	Data bit
RLCz[0]	B[4]*2	B[6]*2	Data bit
RLCz[1]	B[5]*2	B[7]*2	Data bit
RLCz[2]	B[6]*2	B[8]*2	Data bit
RLCz[3]	B[7]*2	B[9]*2	Data bit
RLCz[4]	HSYNC	HSYNC	Control bit
RLCz[5]	VSYNC	VSYNC	Control bit
RLCz[6]	DE	DE	Data Enable*2
RLDz[0]	R[0]	R[2]	Data bit
RLDz[1]	R[1]	R[3]	Data bit
RLDz[2]	G[0]	G[2]	Data bit
RLDz[3]	G[1]	G[3]	Data bit
RLDz[4]	B[0]*2	B[2]*2	Data bit
RLDz[5]	B[1]*2	B[3]*2	Data bit
RLDz[6]	N/A*1	CONT[1]*2*3	Data bit
RLEz[0]	Channel Power Down	R[0]*2	Data bit
RLEz[1]		R[1]*2	Data bit
RLEz[2]		G[0]*2	Data bit
RLEz[3]		G[1]*2	Data bit
RLEz[4]		B[0]*2	Data bit
RLEz[5]		B[1]*2	Data bit
RLEz[6]		CONT[2]*2*3	Data bit

Table 8. LVDS Data Mapping Table for JEIDA Format (MAP=1)

*1 N/A : Not available. THCV226 outputs RLDz[6]=0

*2 CTL bits, which are carried during DE=0 expect the 1st and the last pixel.

*3 3D flags defined in the V-by-One® HS Standard are assigned to the following bits.
V-by-One® HS Standard Packer/Unpacker D[24](3DLR) ⇔ LVDS RLEz[6].
V-by-One® HS Standard Packer/Unpacker D[25](3DEN) ⇔ LVDS RLDz[6].
(z=0,1,2,3)

THCV226 Output	COL		Comment
	0 (8bit)	1 (10bit)	
RLAz[0]	R[0]	R[0]*2	Data bit
RLAz[1]	R[1]	R[1]*2	Data bit
RLAz[2]	R[2]	R[2]	Data bit
RLAz[3]	R[3]	R[3]	Data bit
RLAz[4]	R[4]	R[4]	Data bit
RLAz[5]	R[5]	R[5]	Data bit
RLAz[6]	G[0]	G[0]*2	Data bit
RLBz[0]	G[1]	G[1]*2	Data bit
RLBz[1]	G[2]	G[2]	Data bit
RLBz[2]	G[3]	G[3]	Data bit
RLBz[3]	G[4]	G[4]	Data bit
RLBz[4]	G[5]	G[5]	Data bit
RLBz[5]	B[0]*2	B[0]*2	Data bit
RLBz[6]	B[1]*2	B[1]*2	Data bit
RLCz[0]	B[2]*2	B[2]*2	Data bit
RLCz[1]	B[3]*2	B[3]*2	Data bit
RLCz[2]	B[4]*2	B[4]*2	Data bit
RLCz[3]	B[5]*2	B[5]*2	Data bit
RLCz[4]	HSYNC	HSYNC	Control bit
RLCz[5]	VSYNC	VSYNC	Control bit
RLCz[6]	DE	DE	Data Enable*2
RLDz[0]	R[6]	R[6]	Data bit
RLDz[1]	R[7]	R[7]	Data bit
RLDz[2]	G[6]	G[6]	Data bit
RLDz[3]	G[7]	G[7]	Data bit
RLDz[4]	B[6]*2	B[6]*2	Data bit
RLDz[5]	B[7]*2	B[7]*2	Data bit
RLDz[6]	N/A*1	CONT[1]*2*3	Data bit
RLEz[0]	Channel Power Down	R[8]	Data bit
RLEz[1]		R[9]	Data bit
RLEz[2]		G[8]	Data bit
RLEz[3]		G[9]	Data bit
RLEz[4]		B[8]*2	Data bit
RLEz[5]		B[9]*2	Data bit
RLEz[6]		CONT[2]*2*3	Data bit

Table 9. LVDS Data Mapping Table for VESA Format (MAP=0)

*1 N/A : Not available. THCV226 outputs RLDz[6]=0

*2 CTL bits, which are carried during DE=0 expect the 1st and the last pixel.

*3 3D flags defined in the V-by-One® HS Standard are assigned to the following bits.
V-by-One® HS Standard Packer/Unpacker D[24](3DLR) ⇔ LVDS RLEz[6].
V-by-One® HS Standard Packer/Unpacker D[25](3DEN) ⇔ LVDS RLDz[6].
(z=0,1,2,3)

Monitoring Signal Function

The recovered HSYNC, VSYNC, DE or CLK from V-by-One® HS signals can be monitored by "Monitoring Signal Function". The monitoring lane out of four high-speed data lane is selectable. This function is used for debugging purpose and set by five pins, MON_EN, BET_SEL1, BET_SEL0, BET_LAT and PRBS.

The monitoring signal is outputted from BETOUT pin as 1.8V LVTTL signal.

All signals operate as normal mode except these setting pins and monitoring output pin when "Monitoring Signal Function" is enabled. See the table below.

Pin Option					Monitoring Output	Description
Function	Lane Selection		Signal Selection			
MON_EN	BET_SEL1	BET_SEL0	BET_LAT	PRBS	BETOUT	
0	BET_SEL1	BET_SEL0	BET_LAT	0	BETOUT	Normal mode
1	0	0	0	0	DE	Monitoring Signal Mode to Check Lane0
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	0	1	0	0	DE	Monitoring Signal Mode to Check Lane1
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	1	0	0	0	DE	Monitoring Signal Mode to Check Lane2
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	1	1	0	0	DE	Monitoring Signal Mode to Check Lane3
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	

Table 10. Monitoring Signal Function

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage (VVDD,LVDD,LPVDD,PVDD,CVDD,IOVDD)	-0.3	-	2.1	V
CMOS/TTL Input Voltage	-0.3	-	IOVDD+0.3	V
CMOS/TTL Output Voltage	-0.3	-	IOVDD+0.3	V
Open Drain Input Voltage	-0.3	-	3.6	V
CML Receiver Input Voltage	-0.3	-	VVDD+0.3	V
LVDS Transmitter Output Voltage	-0.3	-	LVDD+0.3	V
Output Current	-50	-	50	mA
Storage temperature	-55	-	125	˚C
Junction temperature	-	-	125	˚C
Reflow Peak Temperature/Time	-	-	260/10	˚C/sec
Maximum Power Dissipation @+25deg	-	-	2.5	W

Table 11. Absolute Maximum Ratings

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage (VVDD,LVDD,LPVDD,PVDD,CVDD,IOVDD)	1.62	1.80	1.98	V
Ta	Operating Temperature	-40	-	85	˚C

Table 12. Recommended Operating Condition

Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage		0.65VDD	-	VDD+0.3	V
VIL	Low Level Input Voltage		-0.3	-	0.35VDD	V
VOH	High Level Output Voltage (IO Type : O) *1	IOH = -2mA	VDD-0.2	-	VDD	V
VOL	Low Level Output Voltage (IO Type : O,OD) *1	IOL = 2mA	GND	-	0.2	V
	Low Level Output Voltage (IO Type : BI) *1	IOL = 160uA	GND	-	0.2	V
IOZH	Output Leak Current High in Hi-Z State		-10	-	10	uA
IOZL	Output Leak Current Low in Hi-Z State		-10	-	10	uA
IIH	High Level Input Leakage Current		-10	-	10	uA
IIL	Low Level Input Leakage Current		-10	-	10	uA

Table 13. Electrical Specifications

*1 IO Type : O = BETOUT , Reserved6,7
OD = HTPDN, LOCKN
BI = DGLOCK

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VRTH	CML Differential Input High Threshold		-	-	50	mV
VRTL	CML Differential Input Low Threshold		-50	-	-	mV
IRIH	CML Input High Leak Current	PDN=0, Rxzp/n=VDD	-10	-	10	uA
IRIL	CML Input Low Leak Current	PDN=0 Rxzp/n=GND	-10	-	10	uA
IRRIH	CML Input High Current	Rxzp/n=VDD	-	-	2	mA
IRRIL	CML Input Low Current	Rxzp/n=GND	-6	-	-	mA
RRIN	CML Differential Input Resistance		80	100	120	Ω

Table 14. Electrical Specifications (z=0,1,2,3)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VROD	LVDS Differential Mode Output Voltage	RL = 100Ω RS = 1	250	350	450	mV
	LVDS Differential Mode Output Voltage	RL = 100Ω RS = 0	100	200	300	mV
⊿ROD	Change in VROD between Complementary Output States	RL = 100Ω	-	-	35	mV
VROC	LVDS Common Mode Output Voltage	RL = 100Ω	1.125	1.25	1.375	V
⊿ROC	Change in VROD between Complementary Output States	RL = 100Ω	-	-	35	mV
IROS	LVDS Output Short Circuit Current	RLyzp/n = GND RL = 100Ω	-	-	100	mA
IROZ	LVDS Output Tri-State Current	PDN = 0 RLyzp/n =GND～VDD	-20	-	20	uA

Table 15. Electrical Specifications (y=A,B,C,CLK,D,E / z=0,1,2,3)

Supply Current

Symbol	Parameter	Conditions	Min	Typ(*1)	Max	Unit
IRCCW	Power Supply Current (Worst case pattern) 10bit mode	MODE2,1,0=111	-	450	515	mA
		MODE2,1,0=001		360	415	
		MODE2,1,0=000		420	475	
		MODE2,1,0=100		295	335	
	Power Supply Current (Gray scale pattern) 10bit mode	MODE2,1,0=111		370	440	
		MODE2,1,0=001		300	355	
		MODE2,1,0=000		345	405	
		MODE2,1,0=100		245	285	
IRCCS	Power Down Supply Current	PDN = 0	-	-	1	mA

Table 16. Supply Current

*1 : VDD=1.8V, Room temperature

Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tRBIT	Unit Interval (UI)	COL = 0	370	tRCOP/30	833	ps
		COL = 1	294	tRCOP/40	625	ps
tRISK	CML Lane0/1/2/3 Input Inter Pair Skew Margin	COL = 0	-30	-	30	UI
		COL = 1	-40	-	40	UI
tRIJT	CML Lane0/1/2/3 Input Jitter Margin	COL = 0	-	-	15	UI
		COL = 1	-	-	20	UI
tRCOP	Clock Out Period		6.37	-	25	ns
tRLVT	LVDS Differential Output Transition Time		-	0.6	1.5	ns
tROP1	LVDS Output Data Position0	HSLVDS mode (tRCOP= 6.37ns – 8.33ns)	-0.20	-	0.20	ns
tROP0	LVDS Output Data Position1		tRCOP/7 -0.20	tRCOP/7	tRCOP/7 +0.20	ns
tROP6	LVDS Output Data Position2		2tRCOP/7 -0.20	2tRCOP/7	2tRCOP/7 +0.20	ns
tROP5	LVDS Output Data Position3		3tRCOP/7 -0.20	3tRCOP/7	3tRCOP/7 +0.20	ns
tROP4	LVDS Output Data Position4		4tRCOP/7 -0.20	4tRCOP/7	4tRCOP/7 +0.20	ns
tROP3	LVDS Output Data Position5		5tRCOP/7 -0.20	5tRCOP/7	5tRCOP/7 +0.20	ns
tROP2	LVDS Output Data Position6		6tRCOP/7 -0.20	6tRCOP/7	6tRCOP/7 +0.20	ns
tROP1	LVDS Output Data Position0	Normal LVDS mode (tRCOP= 11.1ns -16.6ns)	-0.25	-	0.25	ns
tROP0	LVDS Output Data Position1		tRCOP/7 -0.25	tRCOP/7	tRCOP/7 +0.25	ns
tROP6	LVDS Output Data Position2		2tRCOP/7 -0.25	2tRCOP/7	2tRCOP/7 +0.25	ns
tROP5	LVDS Output Data Position3		3tRCOP/7 -0.25	3tRCOP/7	3tRCOP/7 +0.25	ns
tROP4	LVDS Output Data Position4		4tRCOP/7 -0.25	4tRCOP/7	4tRCOP/7 +0.25	ns
tROP3	LVDS Output Data Position5		5tRCOP/7 -0.25	5tRCOP/7	5tRCOP/7 +0.25	ns
tROP2	LVDS Output Data Position6		6tRCOP/7 -0.25	6tRCOP/7	6tRCOP/7 +0.25	ns
tROSK	Link0/1/2/3 LVDS Output Clock Skew		-250	-	250	ps
tRDC	Input Data to Output Data Delay	MODE0 = 0 COL = 0	(17+27/30) tRCOP+4.5	-	(17+27/30) tRCOP+13.5	ns
		MODE0 = 1 COL = 0	(34+24/30) tRCOP+5.0	-	(34+24/30) tRCOP+15.5	

		MODE0 = 0 COL = 1	(17+7/40) tRCOP+4.5	-	(17+7/40) tRCOP+13.5	ns
		MODE0 = 1 COL = 1	(33+14/40) tRCOP+5.0	-	(33+14/40) tRCOP+15.5	
tRPD	Power On to PDN High Delay		0	-	-	ns
tRHPD0	PDN High to HTPDN Low Delay		-	-	1	us
tRHPD1	PDN Low to HTPDN High Delay		-	-	1	us
tRPLL0	Training Pattern Input to LOCKN Low Delay		-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay		-	-	10	us
tRPLL2	LOCKN Low to LVDS CLK Lock Time		-	-	10	ms
tRLCK0	LOCKN Low to LVDS Output Delay		-	-	1	ms
tRLCK1	LOCKN High to LVDS Output High-Z/Low Delay		-	-	1	ms
tRDLH	DGLOCK High to LOCKN Low		0	-	-	ns
tRDLL	DGLOCK Low to LOCKN High		0	-	-	ns
tRDEH	DE=1 Duration	MODE0 = 0	8tRCOP	-	-	ns
		MODE0 = 1	16tRCOP	-	-	ns
tRDEL	DE=0 Duration	MODE0 = 0	8tRCOP	-	-	ns
		MODE0 = 1	16tRCOP	-	-	ns

Table 17. Switching Characteristics

AC Timing Diagram and Test Circuit

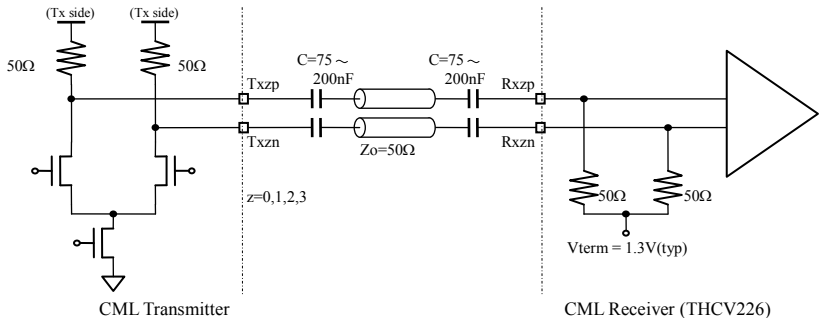


Figure 10. CML Buffer Scheme

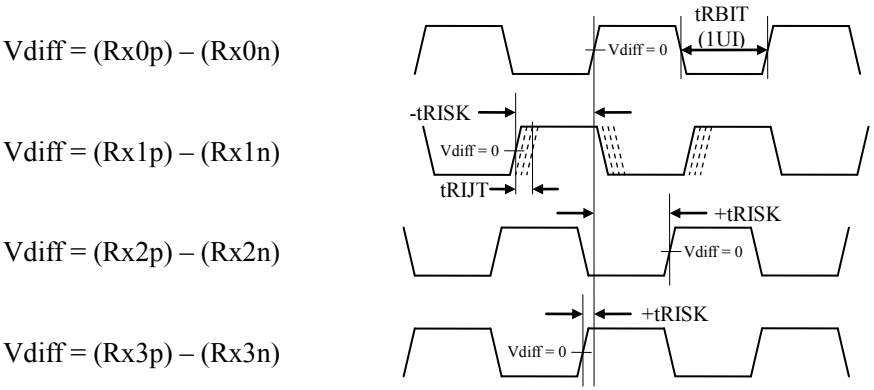


Figure 11. CML Input Timing Diagram

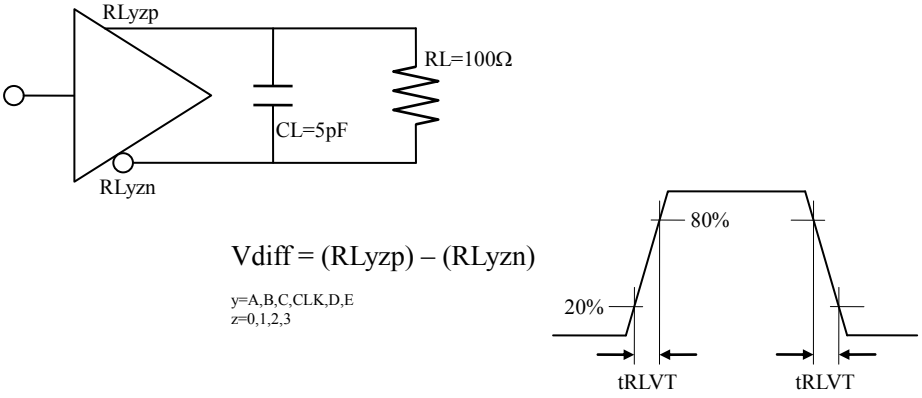


Figure 12. LVDS Output Switching Timing Diagram and Test Circuit

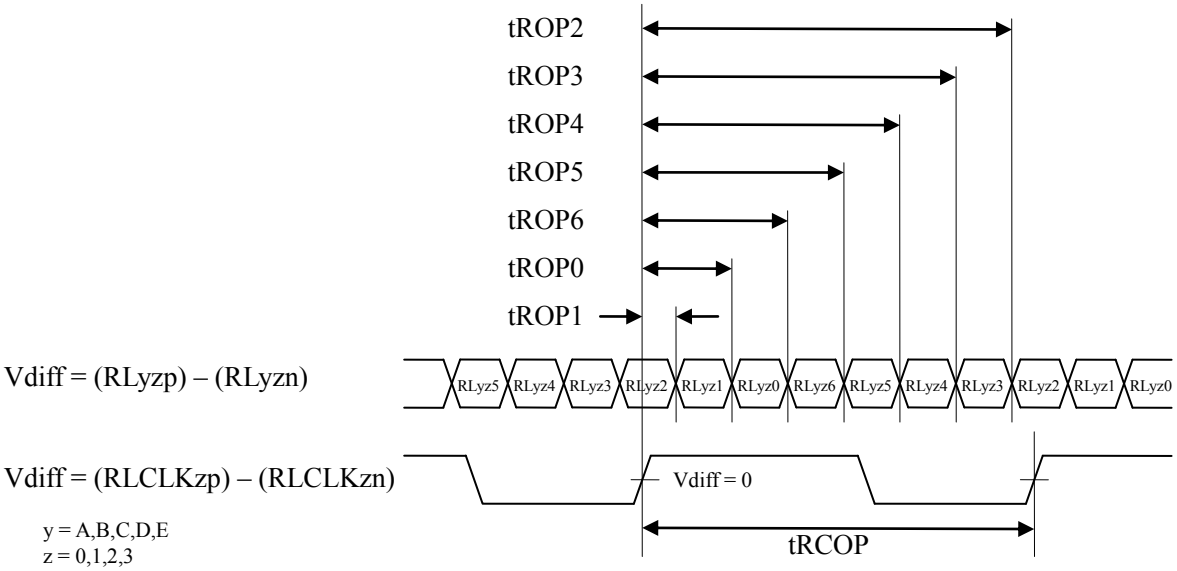


Figure 13. LVDS Output Switching Timing Diagram

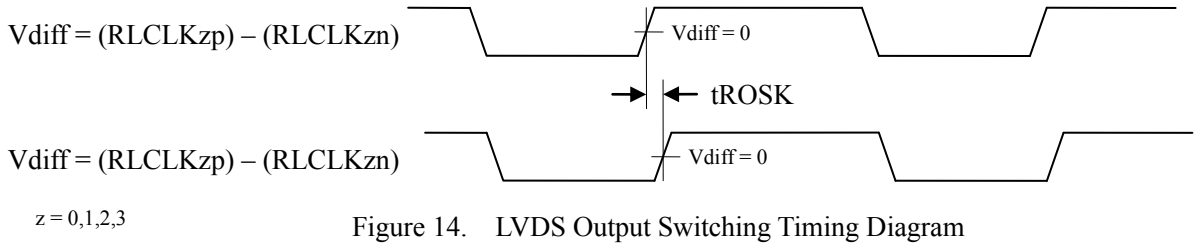


Figure 14. LVDS Output Switching Timing Diagram

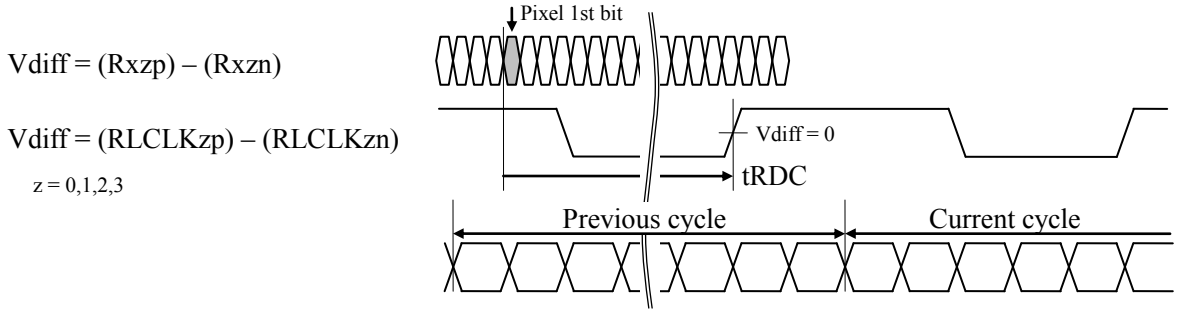


Figure 15. V-by-One® HS Input to LVDS Output Latency

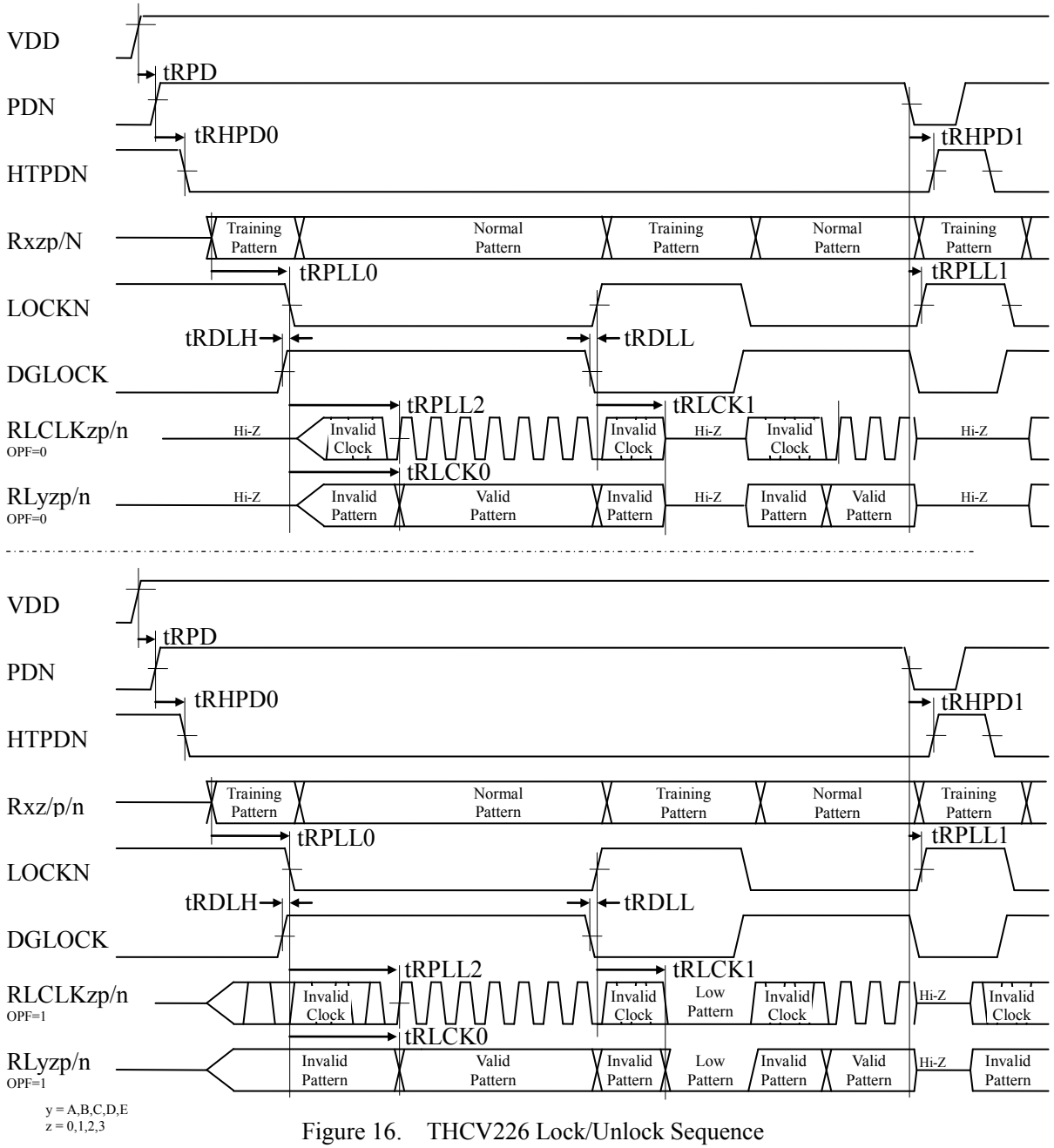


Figure 16. THCV226 Lock/Unlock Sequence

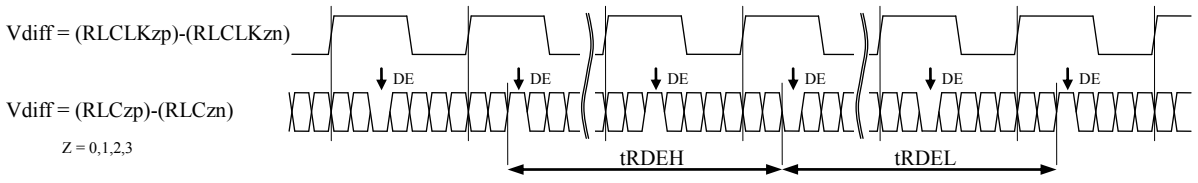


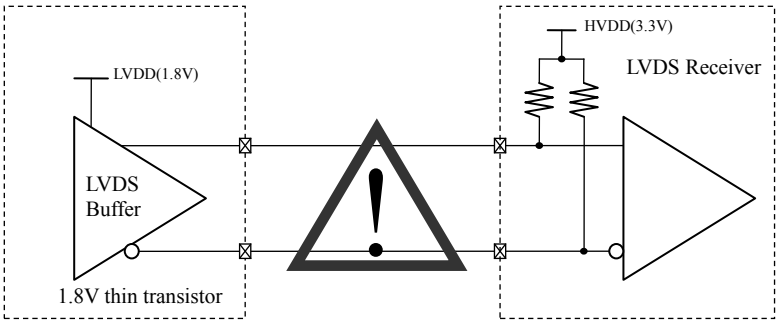
Figure 17. DE Period Requirement

Note

1) LVDS Output Pin Connection

In case that the LVDS Rx of destination device is equipped with pull-up resistors connected to higher than THCV226's VDD voltage, this can cause violation of absolute maximum ratings to THCV226. This phenomenon may be happened at power-on phase and Hi-Z state of the whole system including LVDS Rx device.

One solution for this problem is power-down control for LVDS Rx device during no LVDS input or Hi-Z state period, if its pull-up resistors can be cut off at power-down state. Another solution is to set THCV226's OPF option pin to VDD. This setting provides low fixed data output mode at PDN=1, not Hi-Z state mode.



2) Cable Connection and Disconnection

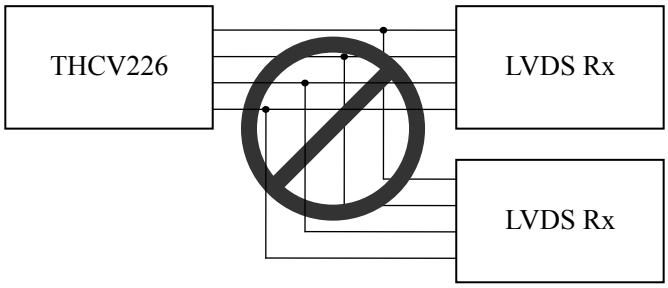
Do not connect and disconnect the LVDS and CML cables, when the power is supplied to the system.

3) GND Connection

Connect the each GND of the PCB which Transmitter and Receiver. It is better for EMI reduction to place GND cables as close to LVDS and CML cables as possible.

4) Multi-drop Connect

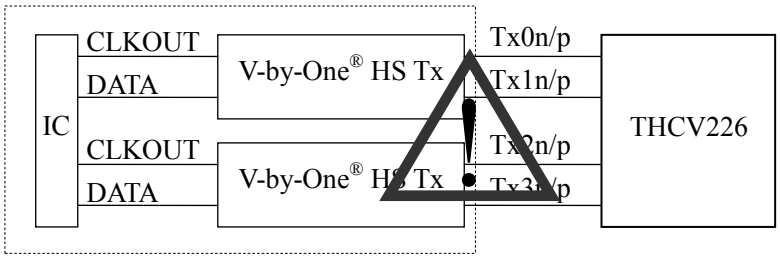
Multi-drop connect is not recommended.



5) Multiple Counterpart Use

Multiple counterpart use such as the following system is not recommended. If it is not avoidable, please check whether tRISK and tRIJT spec of THCV226 can be kept or not. Furthermore, please contact to

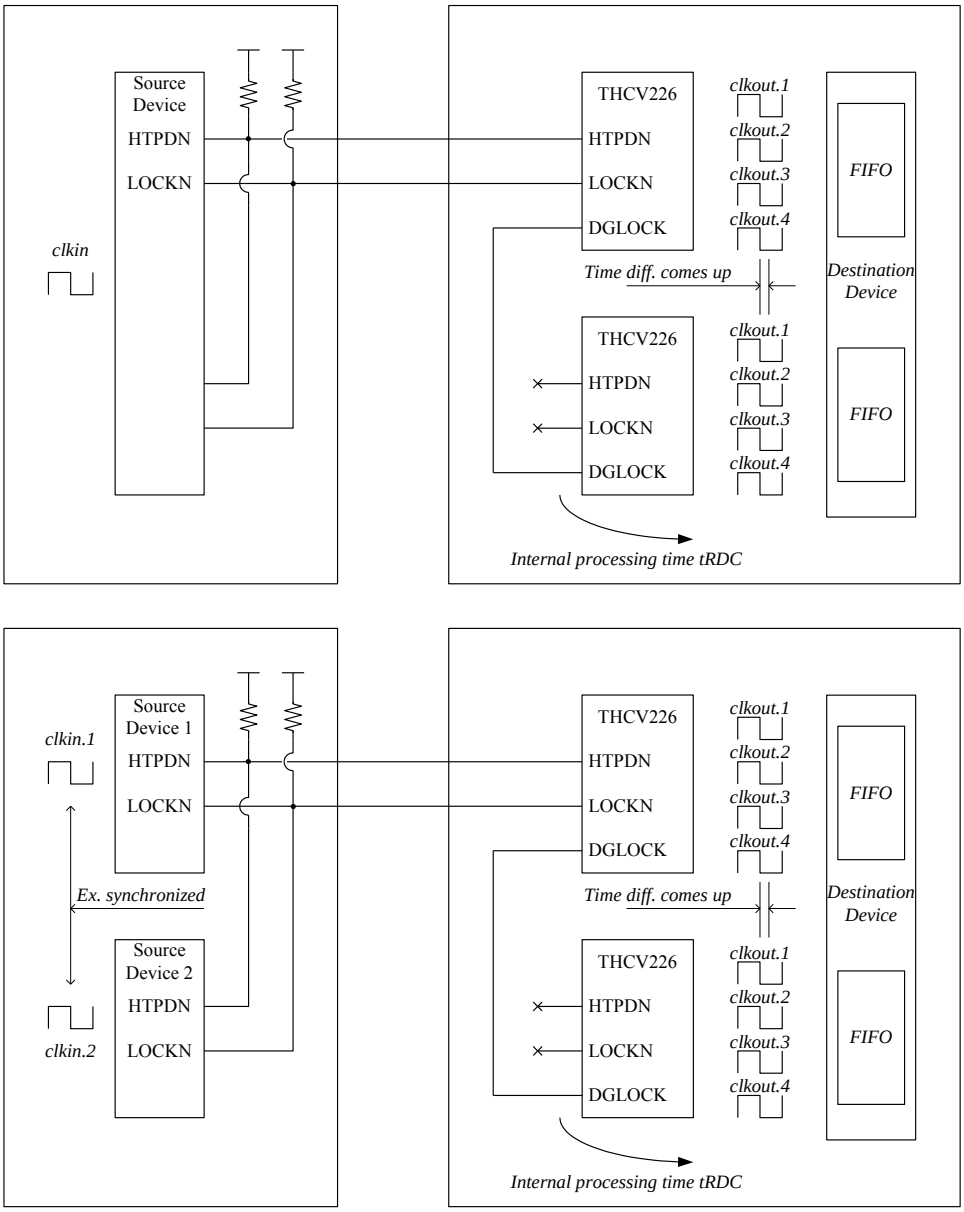
mspsupport@thine.co.jp (for FAE mailing list)



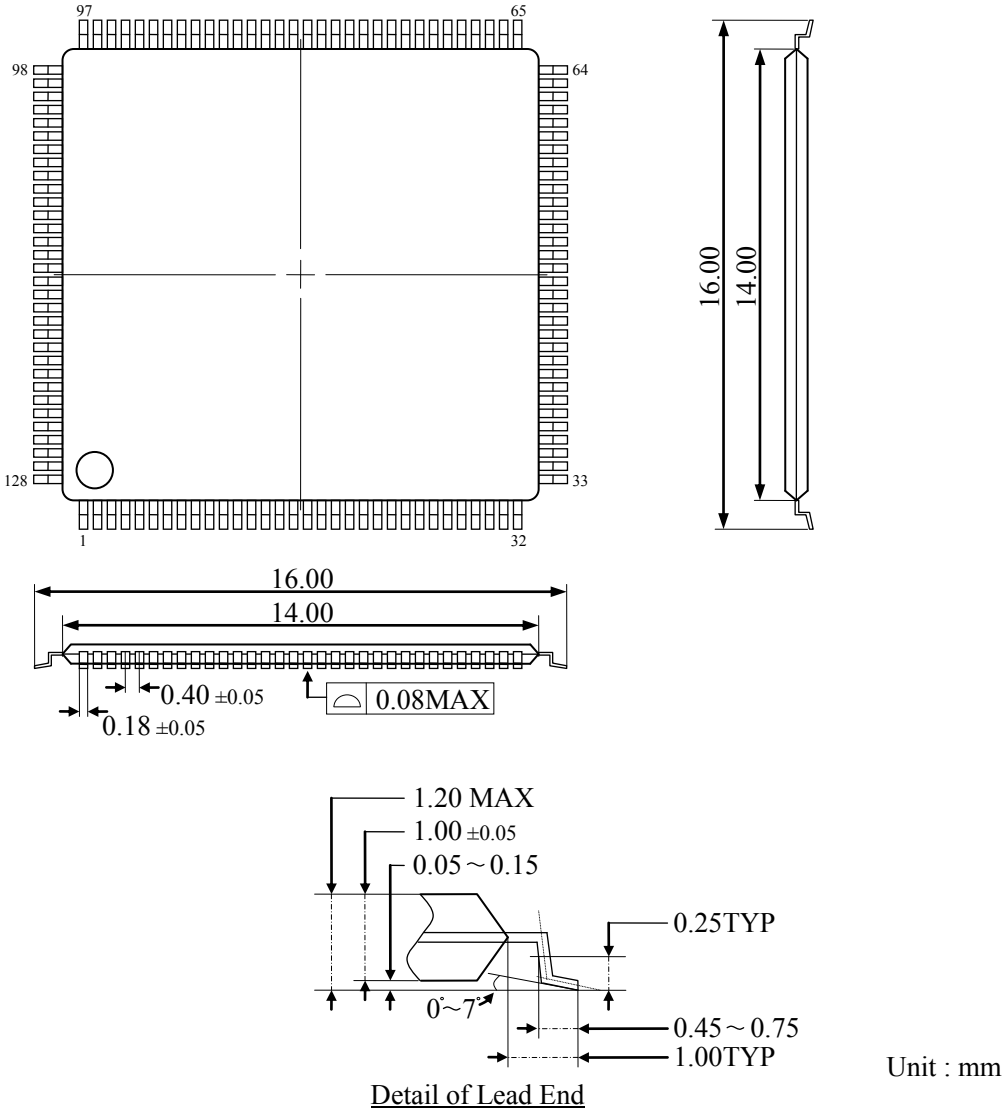
6) Multiple Device Connection

HTPDN and LOCKN signals are supposed to be connected properly for their purpose like the following figure. HTPDN should be from just one THCV226 to multiple Tx devices because its purpose is only ignition of all Tx devices. LOCKN should be connected so as to indicate that CDR status of all Rx devices becomes ready to receive normal operation data. LOCKN of Tx side can be simply split to multiple Tx devices. THCV226's DGLOCK is appropriate for multiple Rx use.

Also possible time difference of internal processing time (THCV226 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV226s, which may have internal FIFO.



Package



Unit : mm

Figure 18. 128-pin TQFP package physical dimension

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.

4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
   5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. (“THine”) accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
   5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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