

Single-chip Type with Built-in FET Switching Regulators

Simple Step-down Switching Regulators with Built-in Power MOSFET



BD9G101G

●General Description

The BD9G101G is switching regulator with integrated internal high-side 42V Power MOSFET. It provides 0.5A DC output with small SOT23 package.

Operating frequency is fixed 1.5MHz, allowing the use of small inductor and ceramic capacitor.

The components of phase compensation is built in. The BD9G101G is available in SOT-23-6(SSOP6) package.

●Features

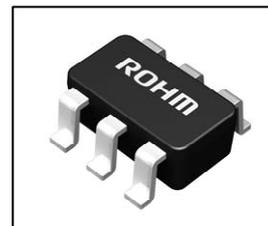
- High and Wide Input Range (VCC=6V~42V)
- 45V/800mΩ Internal Power MOSFET
- 1.5MHz Fixed Operating Frequency
- Feedback Pin Voltage 0.75V±1.5%
- Internal compensated
- Internal Over Current protection, Under Voltage Locked Out, Thermal shutdown
- 0μA Shutdown Supply Current
- 6-Lead SOT-23 package(SSOP6)

●Key Specifications

■ Input Voltage	6~42 [V]
■ Ref. Precision (Ta=25°C)	±1.5[%]
(Ta=-25~105°C)	±2.0[%]
■ Max Output Current	0.5 [A] (Max.)
■ Operating Temperature	-40°C~105°C
■ Max Junction Temperature	150°C

●Packages

SSOP6 2.90 mm × 2.80 mm × 1.25 mm



SSOP6

●Applications

- Industrial distributed power applications
- Automotive Applications
- Battery powered equipment
- OA instruments

●Typical Application Circuits

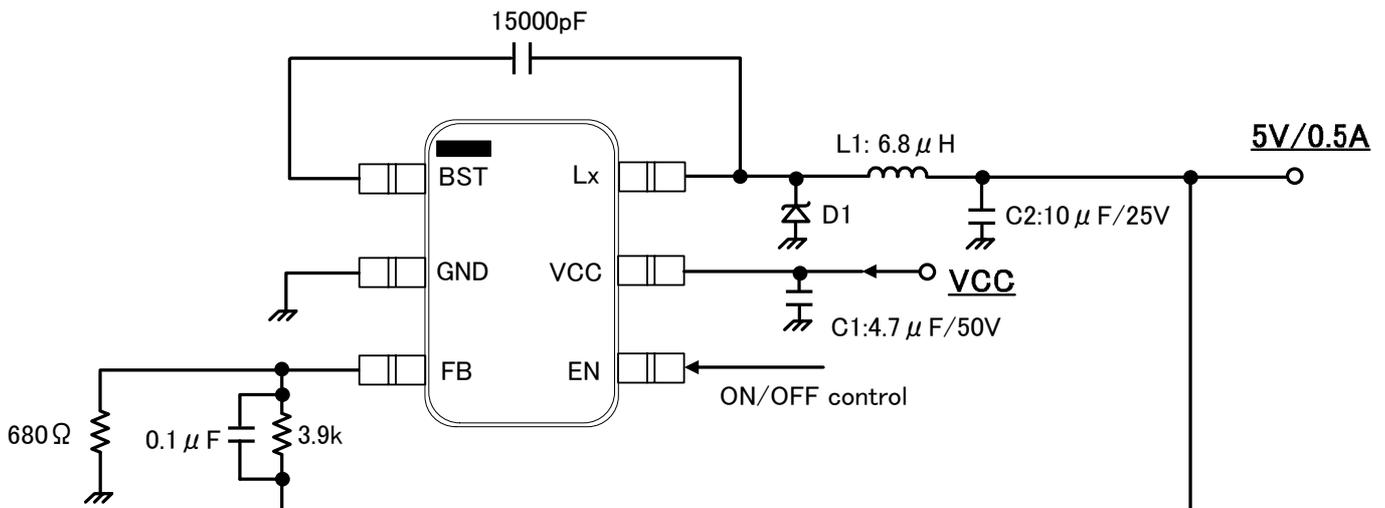


Figure 1. Typical Application Circuit

○Structure : Silicon Monolithic Integrated Circuit ○This product is not designed for normal operation with in a radioactive.

● Pin Configuration

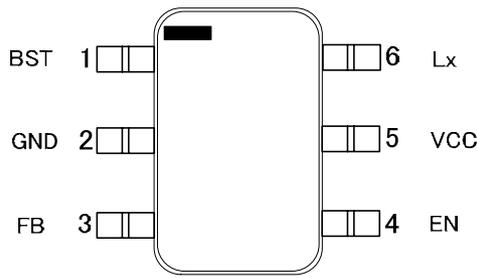


Figure 2. Pin Configuration (TOP VIEW)

● Pin Description

Pin No.	Pin Name	Description
1	BST	The pin is power supply for floating Power NMOS driver. Connected a bypass capacitor between the pin and Lx pin for bootstrap operation.
2	GND	Ground. It should be connected as possible to the output capacitor ground avoiding the high current switch paths.
3	FB	Voltage feedback pin. This pin is error-amp input, the DCDC is set 0.75V at this pin with feed-back operation.
4	EN	Enable input pin. The DCDC is start-up to apply over 2.0V. This pin is pull-down about 550kΩ, the DCDC is shutdown to open or apply under 0.8V.
5	VCC	Input supply. It should be connected as near as possible to the bypass capacitor.
6	Lx	Power FET switch output. It should be connected as near as possible to the schottky barrier diode, and inductor.

● Block Diagram

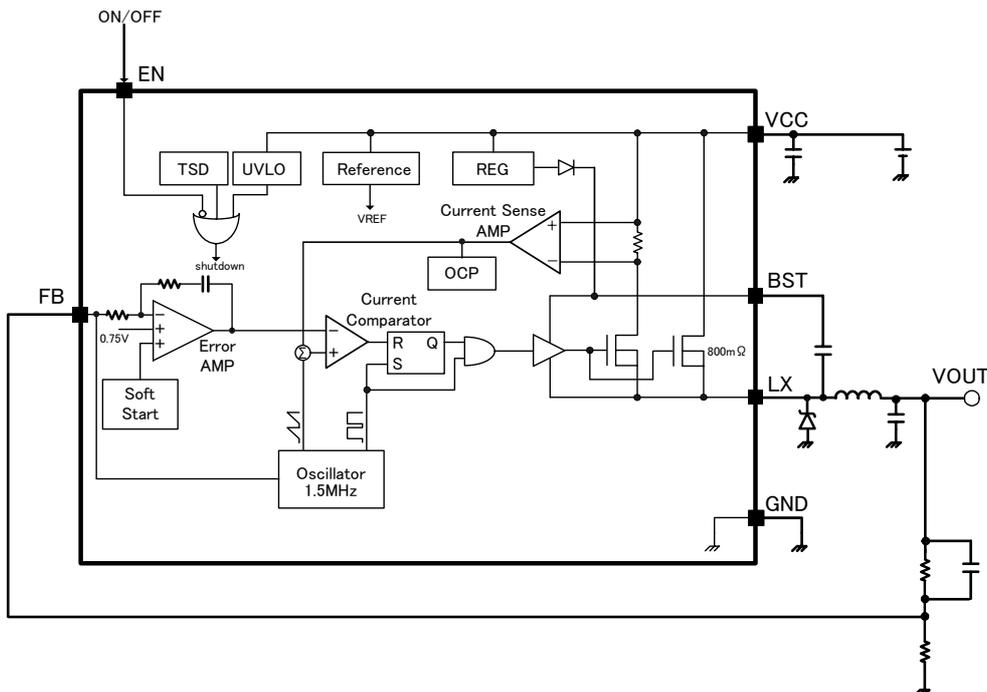


Figure 3. Block Diagram

●Description of Blocks

1. Reference
This block generates reference voltage and current. It start operation by applying EN more than 2.0V.
It provides reference voltage and current to error-amp , oscillator ,and etc.
2. REG
This is a gate drive voltage generator and 4.2V regulator for internal circuit power supply.
3. OSC
This is a precise wave oscillation circuit with operation frequency fixed to 1.5MHz fixed.
To protect from output shorted to GND, Frequency fold-back function is built in.
4. Soft Start
This block does Soft Start to the output voltage of DC/DC comparator, and prevents in-rush current during Start-up.
Soft Start Time depend on application and start-condition because Frequency fold-back function is built in.
5. ERROR AMP
This is an error amplifier what detects output signal, and outputs PWM control signal.
Internal reference voltage is set to 0.75V. Also, the BD9G101G has internal phase compensated element between input and output.
6. ICOMP
This is a comparator that outputs PWM signal from current feed-back signal and error-amp output for current-mode.
7. Nch FET SW
This is an 45V/800mΩ Power Nch MOSFET SW that converts inductor current of DC/DC converter.
8. UVLO
This is a low voltage error prevention circuit.
This prevents internal circuit error during increase of power supply voltage and during decline of power supply voltage.
It monitors VCC pin voltage and internal REG voltage, And when VCC voltage becomes 5.4V and below, it turns OFF all output FET and turns OFF DC/DC comparator output, and Soft Start circuit resets.
Now this Threshold has hysteresis of 200mV.
9. EN
When a Voltage of 2.0V or more is applied, it turns ON, at Open or 0V application, it turns OFF.
About 550kΩ Pull-down Resistance is contained within the Pin.
10. OCP
The current of power MOSFET is limited by this function.
The power MOSFET current is sensed by current sense FET. If the current of power MOSFET is over 1.2A(typ), this function reduce duty by pulse –by- pulse and restrict the and restraint on over current.
- 11.TSD
Circuit for preventing malfunction at high Temperature .
When it detects an abnormal temperature exceeding $T_j=175^{\circ}\text{C}$, it turns OFF DC/DC Comparator Output. The threshold of TSD has Hysteresis(25°C). If Temperature falls 150°C ,the IC automatically returns.

● Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
VCC	VCC	45	V
Maximum input current	I _{max}	1.0	A
BST to GND	VBST	50	V
BST to Lx	ΔVBST	7	V
EN	VEN	45	V
Lx	VLx	45	V
FB	VFB	7	V
Power Dissipation	P _d	0.675 ^(*1)	W
Operating Temperature	T _{opr}	-40~+105 ^(*2)	°C
Storage Temperature	T _{stg}	-55~+150	°C
Junction Temperature	T _{jmax}	150	°C

(*1)During mounting of 70×70×1.6t mm 1layer board.Reduce by 5.4mW for every 1°C increase. (Above 25°C)

(*2)Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. thermal shutdown engages at T_j=175°C(typ) and disengages at T_j=150°C (typ)

● Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=24V, Vo=5V,EN=3V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
【Circuit Current】						
Stand-by Current	I _{st}	—	0	5	μA	VEN=0V
Operating Current	I _{cc}	—	0.7	1.2	mA	FB=1.2V
【Under Voltage Lock Out (UVLO)】						
Threshold Voltage	V _{uv}	5.1	5.4	5.7	V	
Hysteresis width	V _{uvhy}	—	200	300	mV	
【Oscillator】						
Switching Frequency	f _{osc}	1.3	1.5	1.7	MHz	
Max Duty Cycle	D _{max}	85	-	-	%	
【Error AMP】						
FB Pin Reference Voltage	VFBN	0.739	0.750	0.761	V	Ta=25°C
	VFBA	0.735	0.750	0.765	V	Ta=-25~105°C
FB Pin Bias Current	IFB	-100	0	100	nA	VFB=2.0V
Soft-Start Time	T _{soft}	1.2	4.0	-	ms	
【Current Comparator】						
Trans-conductance	G _{cs}	-	3	-	A/V	
【Output】						
Nch MOSFET ON Resistance	R _{onH}	—	800	—	mΩ	
Min ON Time	T _{min}	—	100	—	nsec	
Switch Current Limit	I _{ocp}	0.85	1.2	—	A	
【CTL】						
EN Threshold Voltage	ON	VENON	2.0	—	VCC	V
	OFF	VENOFF	-0.3	—	0.8	V
EN Input Bias Current	REN	2.7	5.5	11	μA	VEN=3V

⊙ Not designed to withstand radiation.

●Operating Ratings

Item	Symbol	Ratings			Unit
		Min	Typ	Max	
Input Voltage	VCC	6	-	42	V
Output Voltage	VOUT	1.0 ^(*2)	-	VCC × 0.7 ^(*3)	V
Output Current	IOUT	-	-	500	mA

(*2)Restricted by minimum on pulse typ. 100nsec
 (*3)Restricted by maxduty ,Ron and BST-UVLO.

●input and output voltage restriction

The input voltage range of BD9G101G is limited by Ron, Maxduty(min85%) and preventing malfunction at low voltage between BST and LX(BST-UVLO).

①BST-UVLO

BSTUVLO is the function that prevent the IC from abnormal operation that is caused by shortage of charge of High-SideFET driving. If the voltage between BST and Lx is lower than 1.5V, High-Side FET is turned off and there are new pass to charge voltage VCC to BST. BST voltage is charged by Vcc and goes over BST-UVLO threshold. As a result , BST-UVLO is turned off.

The condition that BST-UVLO is working property is $VCC \gg (BST-UVLO \text{ threshold} + V_f) + V_{out}$.

Therefore maximum output voltage is lower than $V_{in} - 3V$.

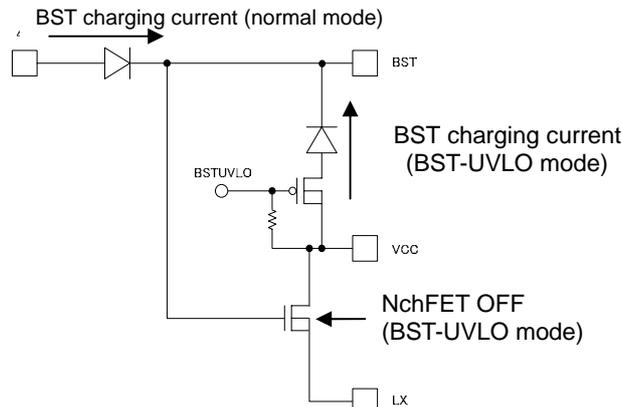


Figure 4. BST-UVLO image

※When operation can be considered by $V_{in} - V_{out} < 3V$, output voltage leaps up to near input voltage by BSTUVLO operation at the time of a light load.

The waveform of operation and a mechanism are shown.

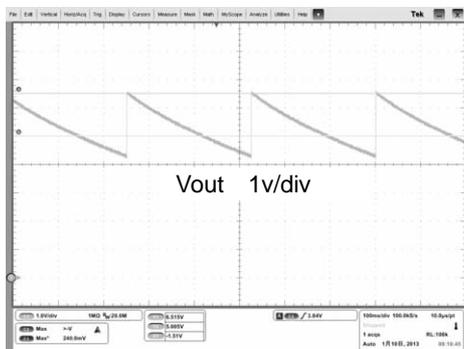
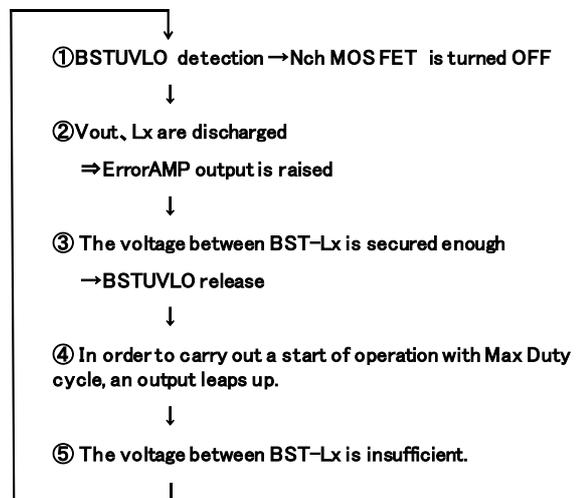


Figure 5. BSTUVLO operation waveform
 $V_{out}=5V$ $V_{in}=7V$ $I_{out}=0mA$



●Frequency fold-back function

This IC has the frequency fold-back function to prevent from over current with the circuit output is shorted. The frequency fold-back has the function that the frequency is changed by FB voltage. Figure.5 shows FB voltage vs frequency Characteristics.

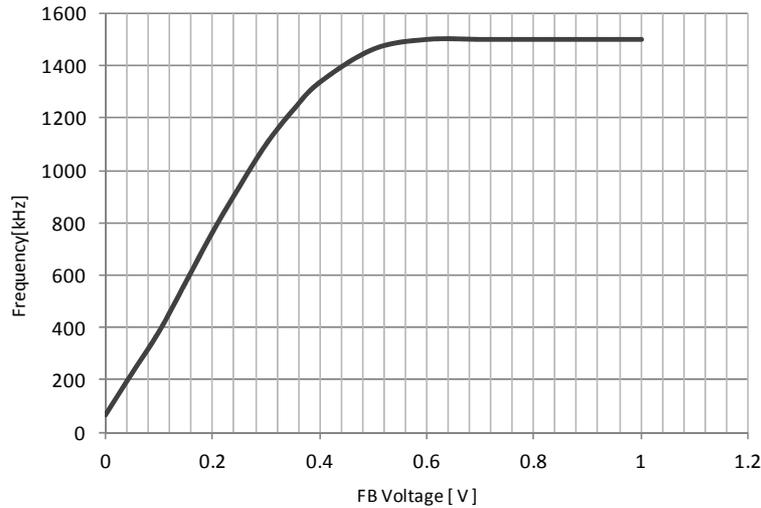


Figure 7. FB voltage -frequency Characteristics

When the output node is shorted, the IC narrows the frequency to 150kHz(typ) so that input current limiting. This IC operates on 1.5MHz in case of normal mode, the voltage of FB is about 0.75V.

●Start-up Characteristics

When the IC is starting up, frequency reacts to the voltage of FB on the function of frequency fold back. For the Softstart is operated by internal frequency clock, according to rising to the output voltage, the Softstart rising speed is more faster. Please check the using condition and the application waveform (P.11,P14) because of the Start-up characteristics changes to the output load and the output capacitor.

● Typical Performance Characteristics

(Unless otherwise specified, Ta=25°C, VCC=12V, Vo=5V, EN=3V)

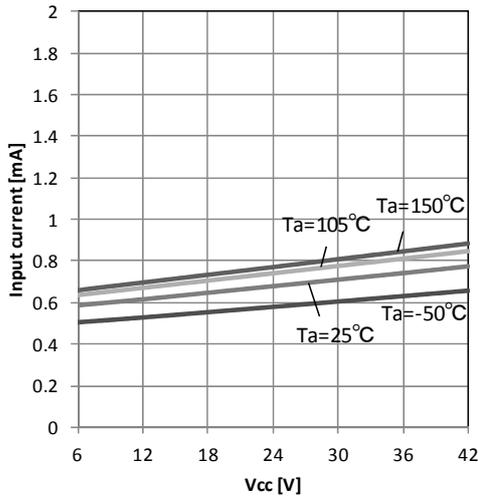


Figure 8. Operating Current - Input Voltage

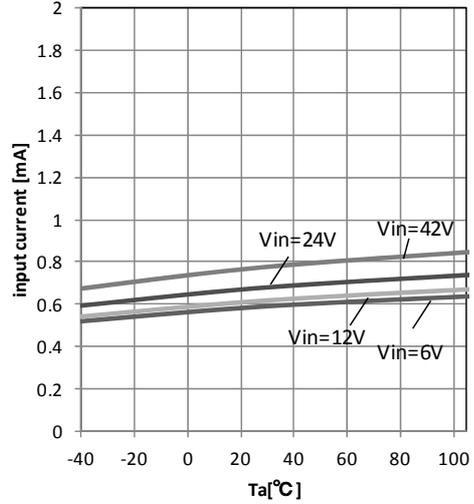


Figure 9. Operating Current - Temperature

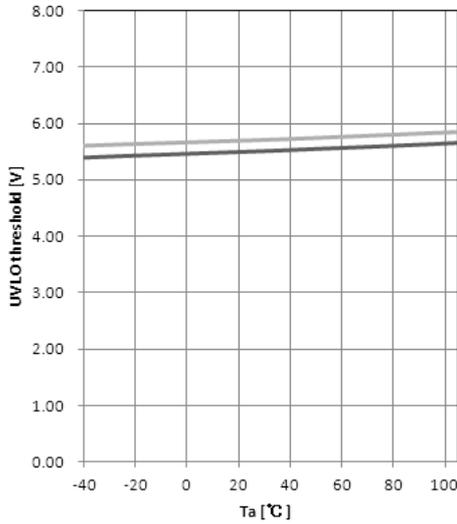


Figure 10. UVLO Threshold - Temperature

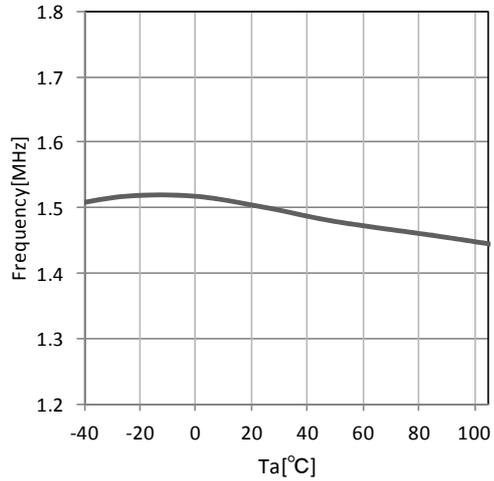


Figure 11. Oscillation frequency - Temperature

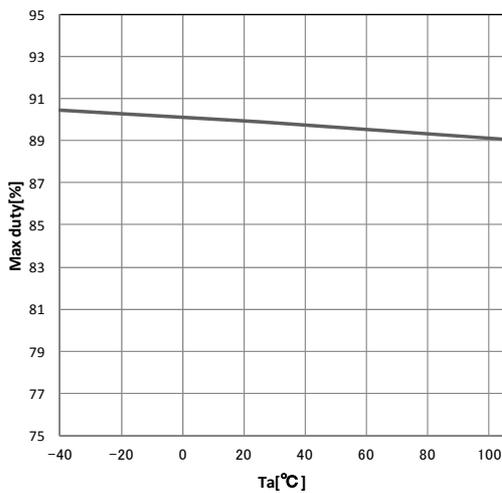


Figure 12. Max Duty - Temperature

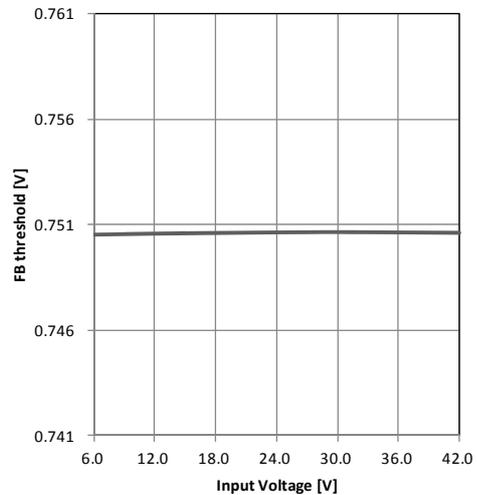


Figure 13. FB Pin Reference Voltage – Input Voltage

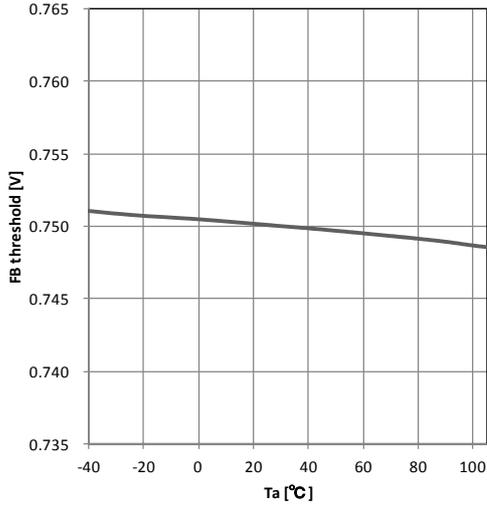


Figure 14. FB Threshold - Temperature

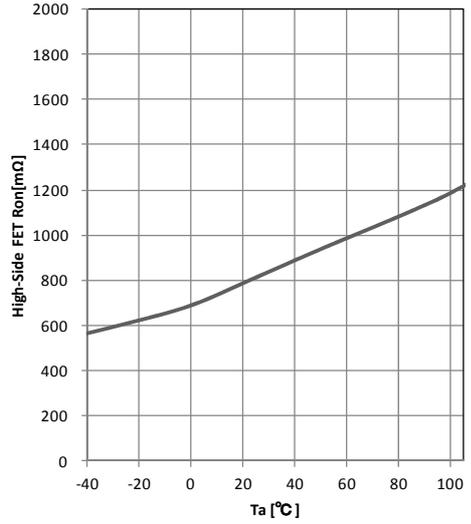


Figure 15. Nch MOSFET ON Resistance - Temperature

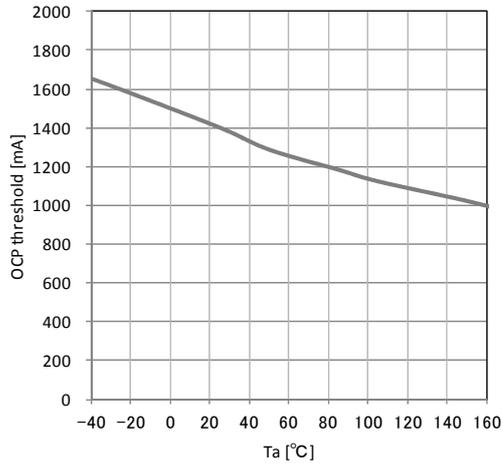


Figure 16. OCP threshold- Temperature

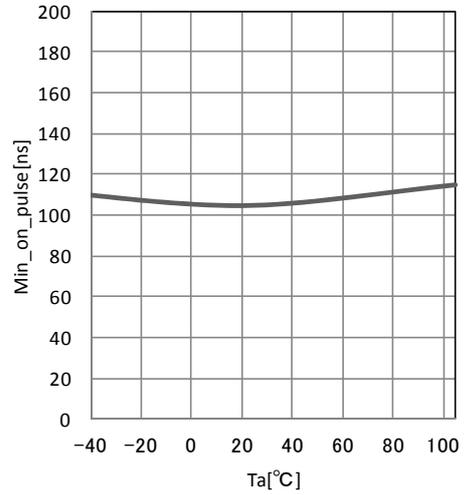


Figure 17. Min ON Time - Temperature

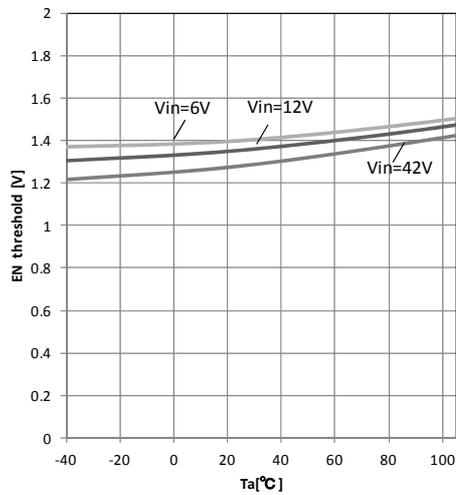


Figure 18. EN Threshold Voltage - Temperature

●Reference Characteristics of typical Application Circuits

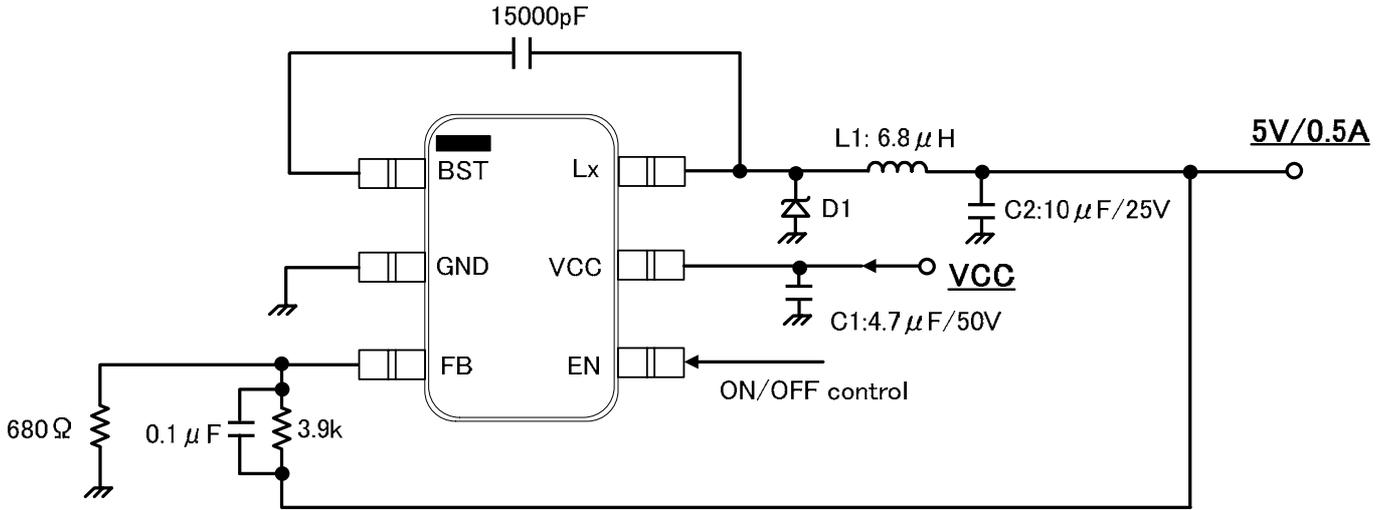


Figure 19. Typical Application Circuit (VOUT=5V)

Parts	L1	TOKO TAIYO YUDEN	DEM4518C 1235AS-H-6R8M NR4018	6.8μH 6.8μH
	C1	Murata	GRM32EB31H475KA87	4.7μF/50V
	C2	Murata	GRM31CB11A106KA01	10μF/10V
	D1	Rohm	RB060M-60	

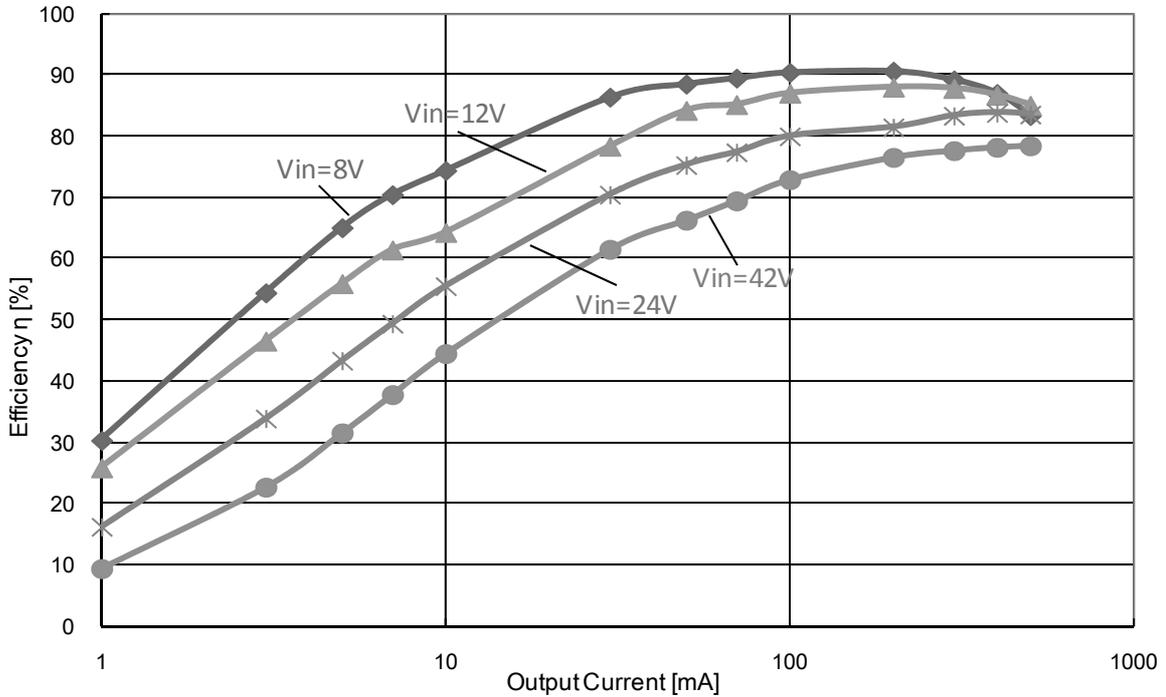


Figure 20. Efficiency - Output Current VOUT=5V

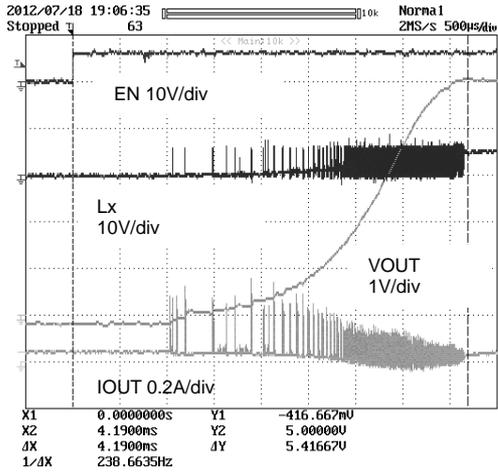


Figure 21. Start-up Characteristics
VIN=8V, IOU=0mA ,VOUT=5V

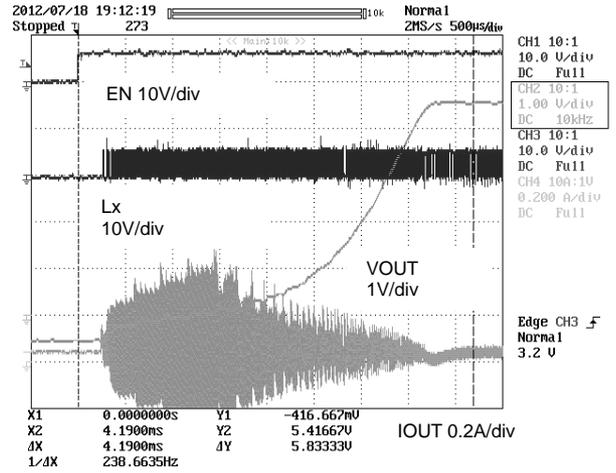


Figure 22. Start-up Characteristics
VIN=8V, IOU=500mA, VOUT=5V

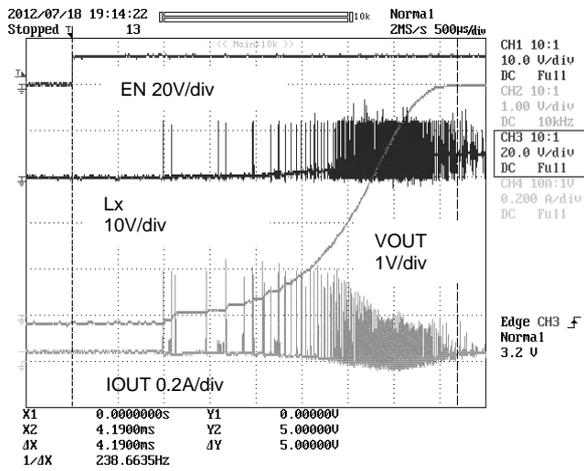


Figure 23. Start-up Characteristics
VIN=12V, IOU=0mA, VOUT=5V

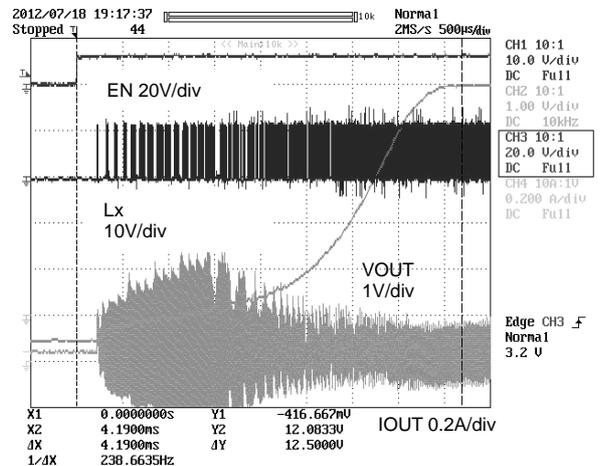


Figure 24. Start-up Characteristics
VIN=12V, IOU=500mA ,VOUT=5V

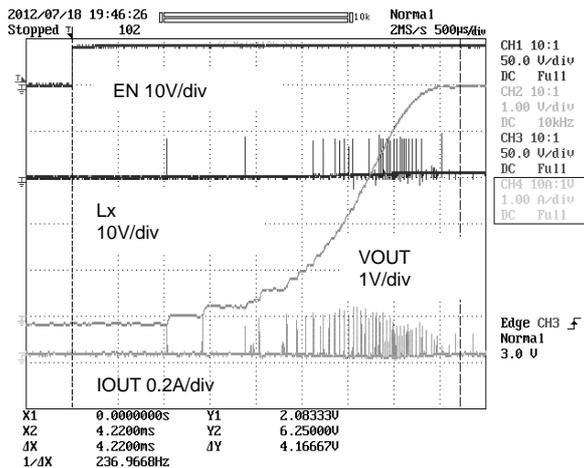


Figure 25. Start-up Characteristics
VIN=42V, IOU=0mA, VOUT=5V

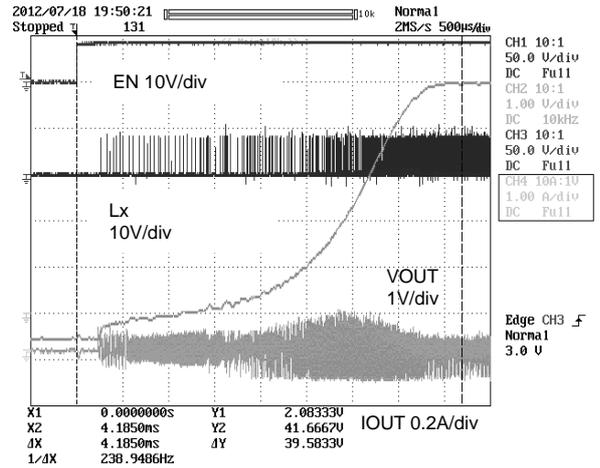


Figure 26. Start-up Characteristics
VIN=42V, IOU=500mA, VOUT=5V

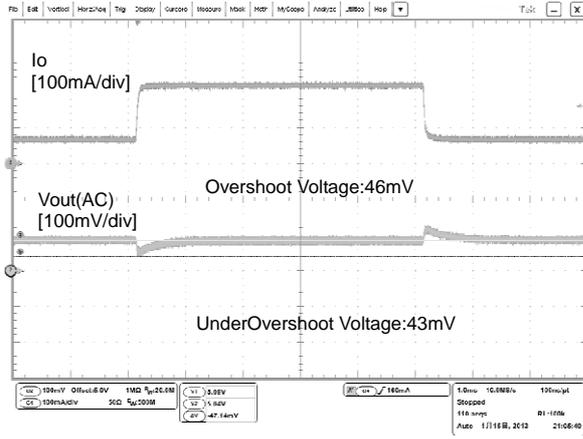


Figure 27. Load Response
Io=50mA↔200mA

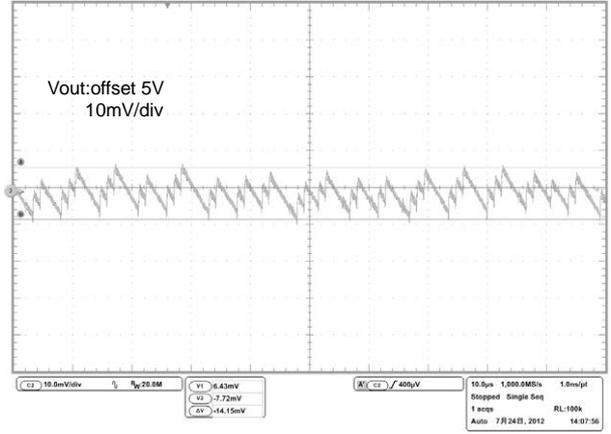


Figure 28. Lx Switching/ Vout
Ripple

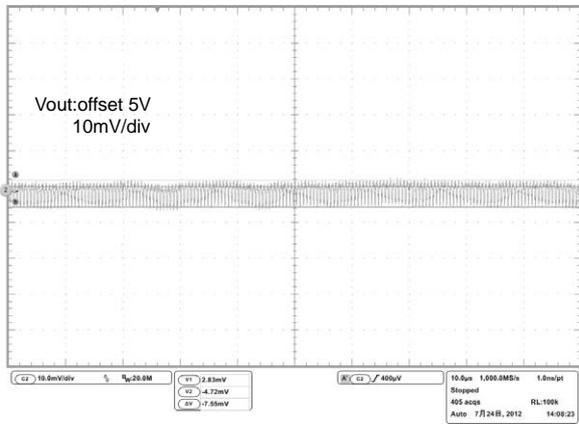


Figure 29. Lx Switching/ Vout
Ripple

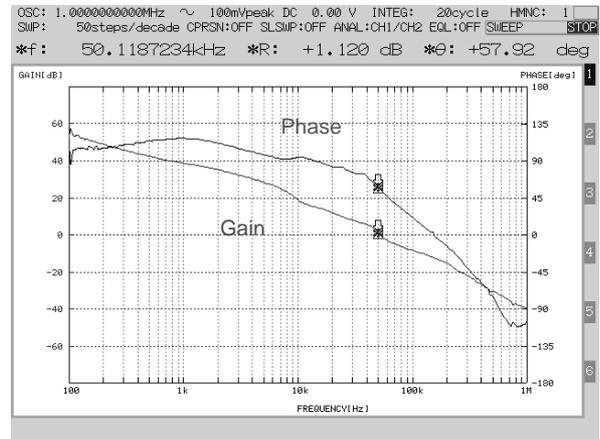


Figure 30. Frequency Response
Io=100mA, VOUT=5V

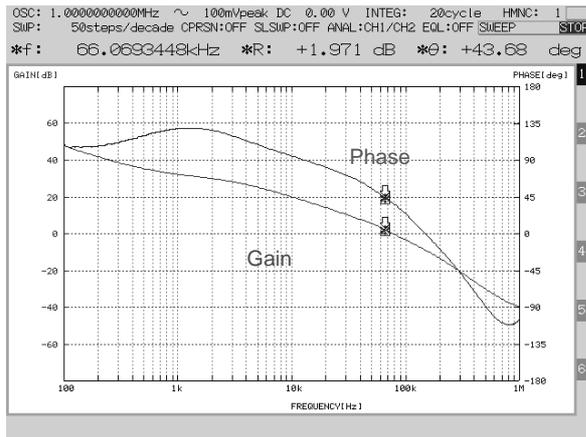


Figure 31. Frequency Response
Io=500mA, VOUT=5V

●Reference Characteristics of typical Application Circuits

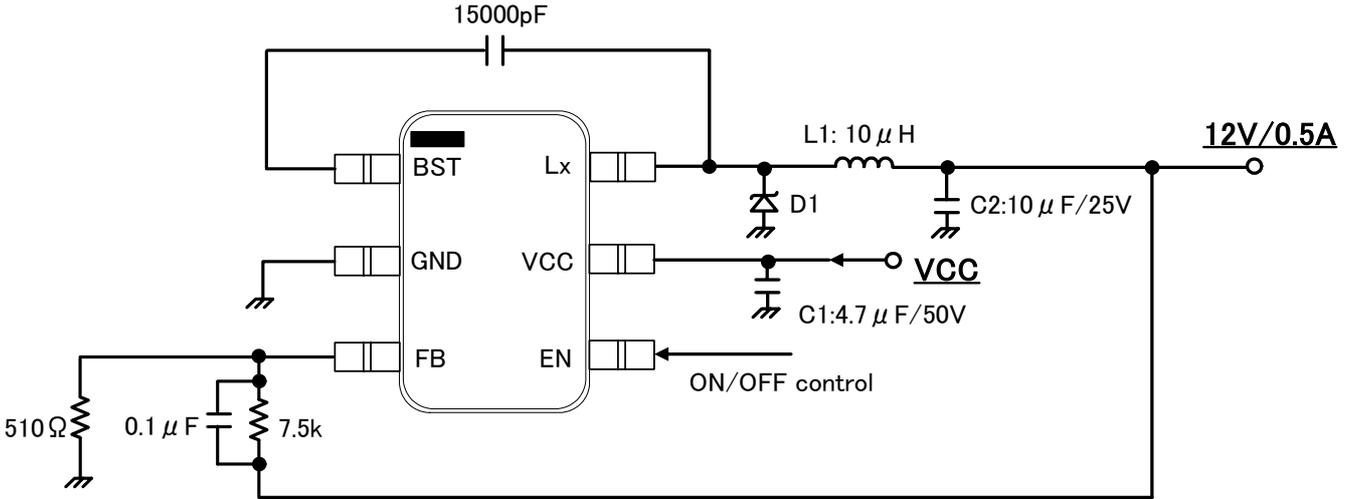
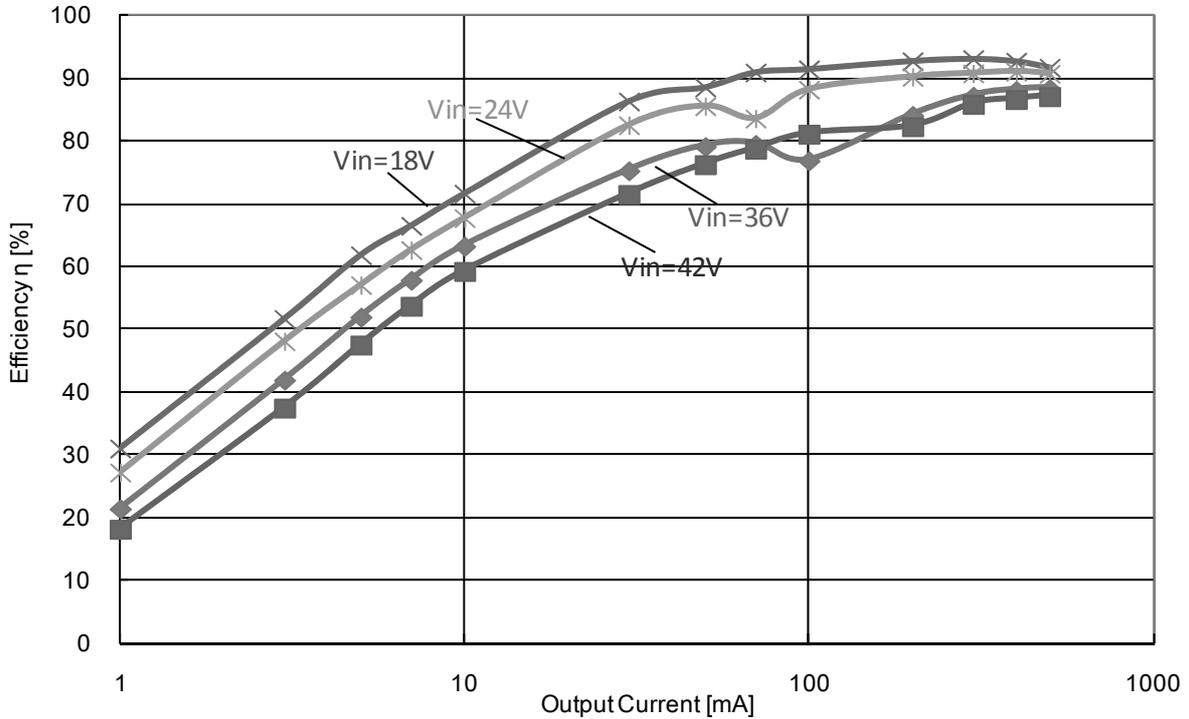


Figure 32. Typical Application Circuit (VOUT=12V)

使用部品	: L1	: TOKO TAIYO YUDEN	DEM4518C 1235AS-H-6R8M NR4018	10μH 10μH
	: C1	: Murata	GRM32EB31H475KA87	4.7μF/50V
	: C2	: Murata	GRM31CB11A106KA01	10μF/25V
	: D1	: Rohm	RB060M-60	



*The efficiency is fall when the switching waveform is turning from intermittent mode to continuous mode

Figure 33. Efficiency - Output Current VOUT=12V

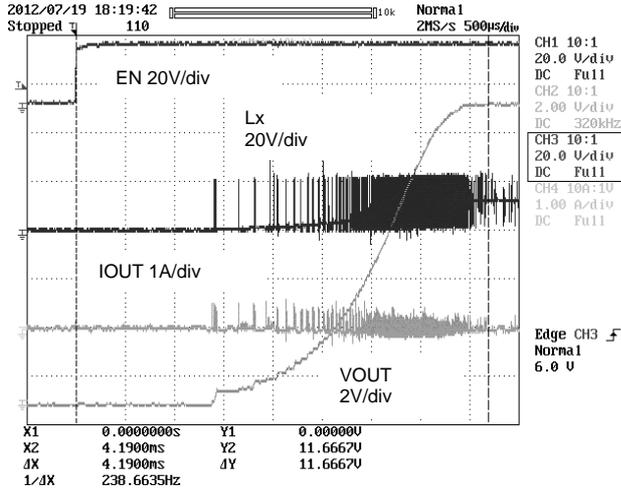


Figure 34. Start-up Characteristics
VIN=18V, IOU=0mA, VOUT=12V

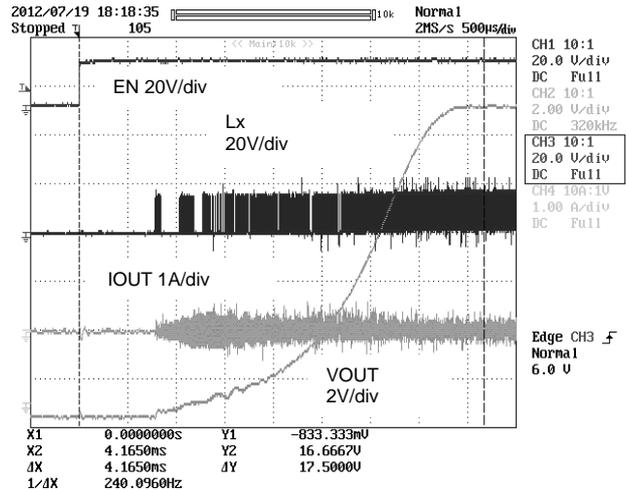


Figure 35. Start-up Characteristics
VIN=18V, IOU=500mA, VOUT=12V

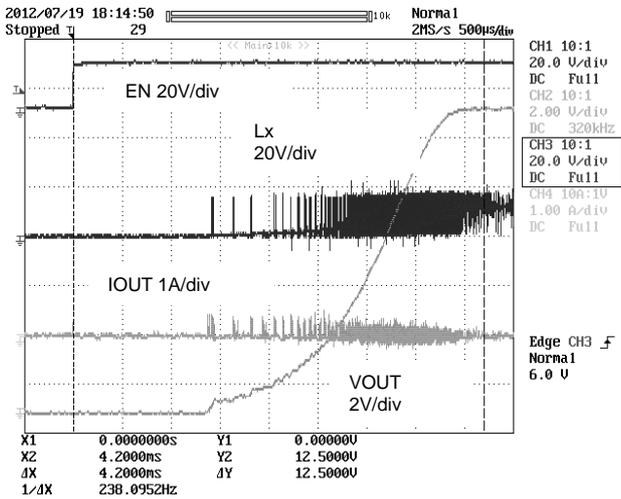


Figure 36. Start-up Characteristics
VIN=24V, IOU=0mA, VOUT=12V

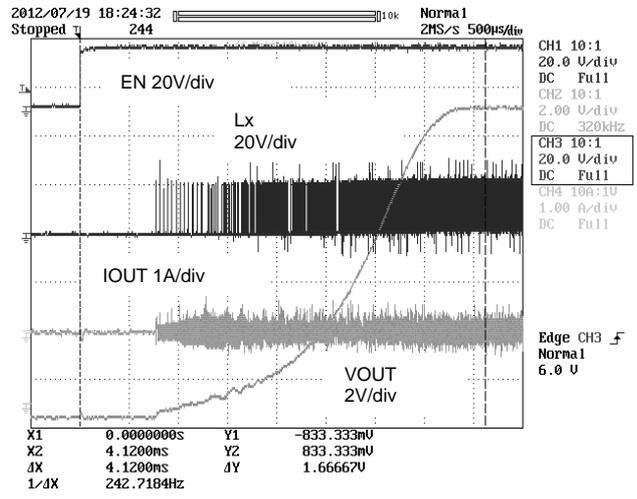


Figure 37. Start-up Characteristics
VIN=24V, IOU=500mA, VOUT=12V

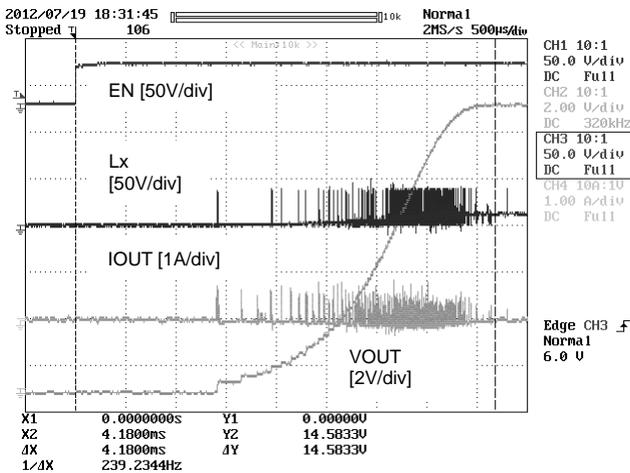


Figure 38. Start-up Characteristics
VIN=42V, IOU=0mA, VOUT=12V

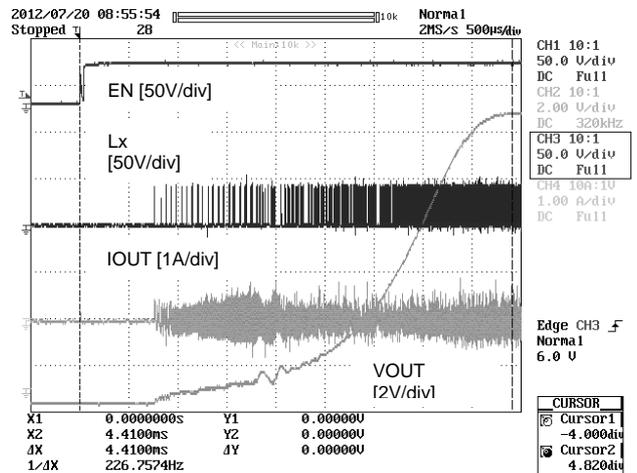


Figure 39. Start-up Characteristics
VIN=42V, IOU=500mA, VOUT=12V

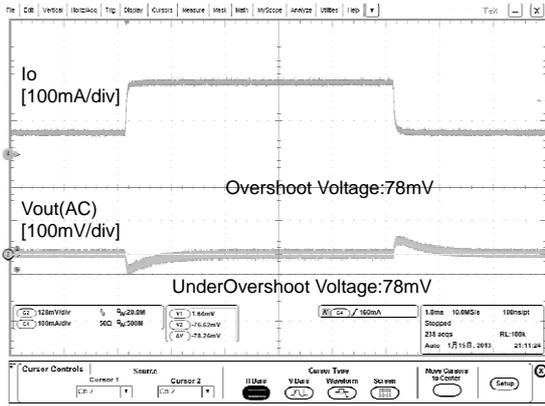


Figure 40. Load Response
 $I_o=50\text{mA} \leftrightarrow 200\text{mA}$, $V_{OUT}=12\text{V}$

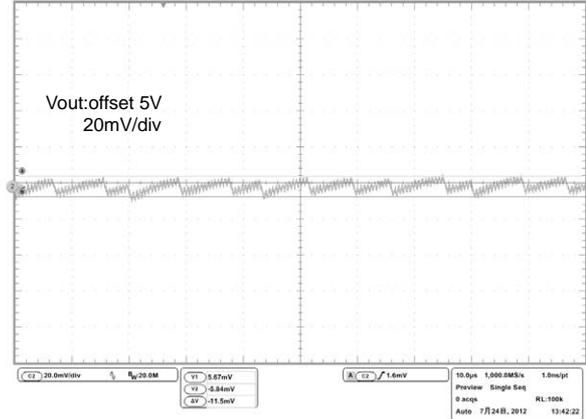


Figure 41. Lx Switching/ Vout Ripple
 $I_o = 50\text{mA}$, $V_{OUT}=12\text{V}$

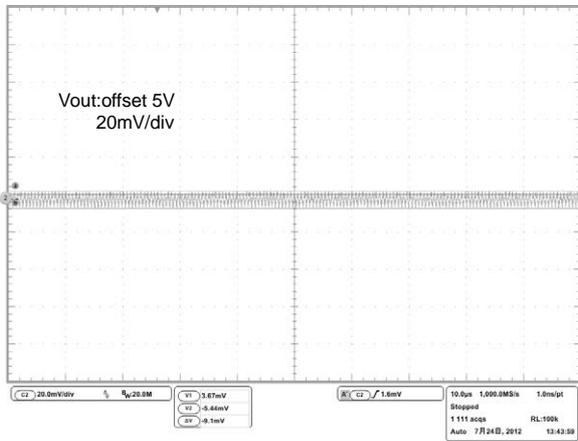


Figure 42. Lx Switching/ Vout Ripple
 $I_o = 200\text{mA}$, $V_{OUT}=12\text{V}$

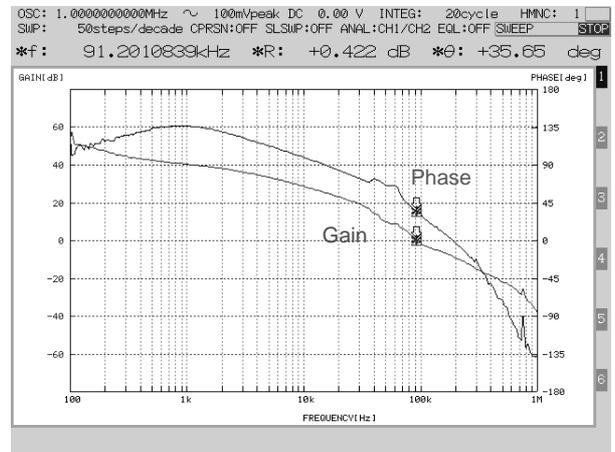


Figure 43. Frequency Response
 $I_o=100\text{mA}$, $V_{OUT}=12\text{V}$

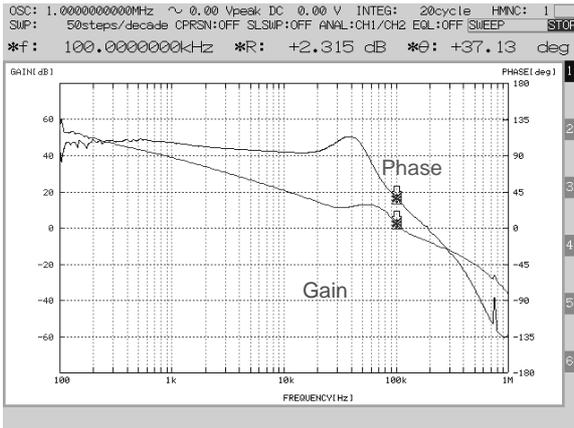


Figure 44. Frequency Response
 $I_o=500\text{mA}$, $V_{OUT}=12\text{V}$

●Application Components Selection Method

(1) Inductors

Something of the shield type that fulfills the current rating (Current value Ipeak below), with low DCR is recommended. Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple. In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

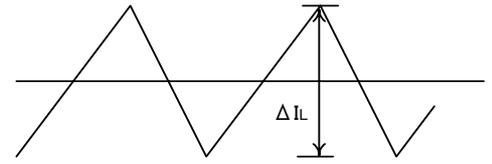


Figure 43. Inductor Current

$$I_{peak} = I_{out} + \Delta I_L / 2 \text{ [A]} \quad (4)$$

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} \times \frac{V_{out}}{V_{in}} \times \frac{1}{f} \text{ [A]} \quad (5)$$

(ΔIL: Output Ripple Current, f: Switching Frequency)

For design value of Inductor Ripple Current, please carry out design tentatively with about 20%~50% of Maximum Input Current.

In the BD9G101G, it is recommended the below series of 2.2μH~10μH inductance value.

Recommended Inductor TOKO DE4518C Series
TAIYO YUDEN NR4018 Series

(2) Input Capacitor

In order for capacitor to be used in input to reduce input ripple, mount low ceramic capacitor of ESR near the Vcc pin. In the BD9G101G, it is recommended the 4.7μF or more capacitor value. In case of using the electrolytic capacitor, mount 1μF ceramic capacitor in parallel in order to prevent oscillation

(3) Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended. Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. Output ripple voltage is looked for using the following formula.

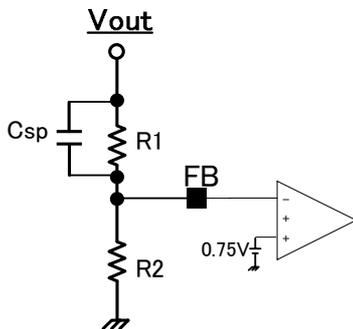
$$V_{pp} = \Delta I_L \times \frac{1}{2\pi \times f \times C_o} + \Delta I_L \times R_{ESR} \text{ [V]} \quad (6)$$

Please design in a way that it is held within Capacity Ripple Voltage.

In the BD9G101G, it is recommended a ceramic capacitor over 10μF.

(4) Output voltage setting

The internal reference voltage of ERROR AMP is 0.75V. Output voltage is determined like (7) types.



$$V_o = \frac{(R1+R2)}{R2} \times 0.75[V] \dots (7)$$

Figure 6. Output voltage setting

However, in order to avoid the BSTUVLO operation at the time of a reduced power and light load, please set up R1+R2 is satisfied the following formulas.

$$R1 + R2 \leq V_{out} \times 10^3 \dots (8)$$

The example of output resistances setting : output voltage 5V R1=3.9kΩ R2=0.68kΩ
output voltage 12V R1=7.5kΩ R2=0.51kΩ

(5) Feed-forward capacitor Csp

Please mount feed-forward capacitor in parallel to output resistance R1.

In order that a feed-forward capacitor may adjust the loop characteristic by adding the pair of a pole and zero to the loop characteristic. A phase margin is improved and transient response speed improves.

The feed-forward capacitor Csp should use the value near the following formulas.

$$C_{sp} = \frac{4.7k}{R1} \times 0.15 \quad [uF] \quad \dots (9)$$

The example of a Csp setting :
output voltage 5V R1=3.9kΩ R2=0.68kΩ Csp = 0.1uF or 0.22uF
output voltage 12V R1=7.5kΩ R2=0.51kΩ Csp = 0.1uF

By above mentioned measure, there is not BSTUVLO operation in light load and Vin-Vout<3V.

(6) Bootstrap Capacitor

Please connect from 15000pF (Laminate Ceramic Capacitor) between BST Pin and Lx Pins.

(7) Diode

Select suitable shottky diode for break down voltage and input current.

● Cautions on PC Board layout

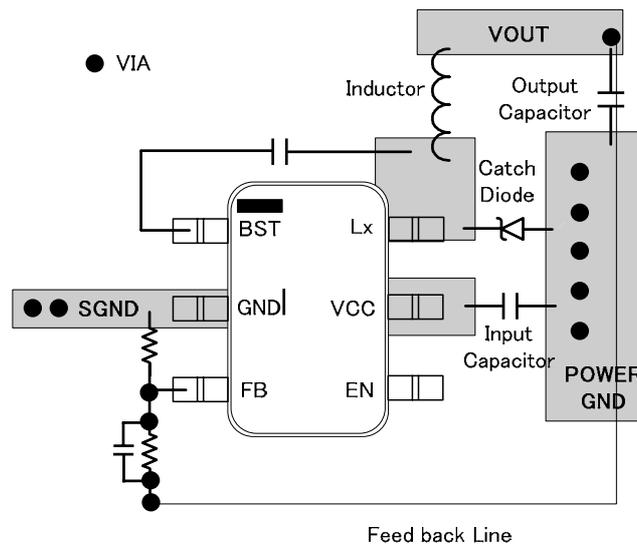


Figure 45. Reference PCB layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Figure.45 for a PCB layout example.

In the BD9G101G, since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. And GND area should not be connected directly power GND, connected avoiding the high current switch paths. The additional external components can be placed approximately as shown.

●Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 70mm × 70mm × 1.6mm^t, 1layer PCB.
Junction temperature must be designed not to exceed 150°C

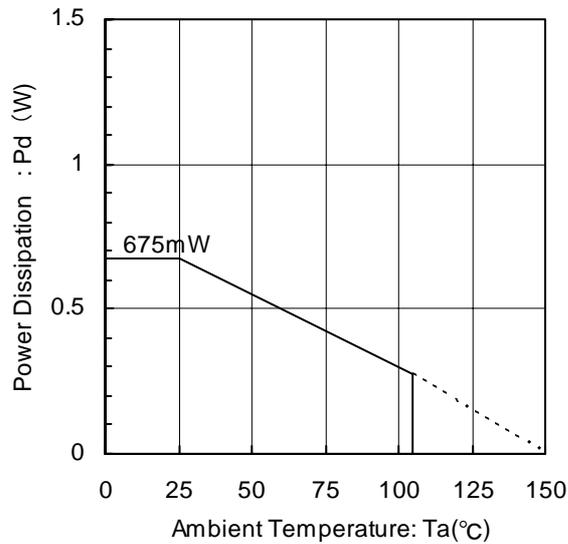


Figure 46. Power Dissipation (70mm × 70mm × 1.6mm^t 1layer PCB)

●Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.

The device power dissipation includes:

- 1) Conduction loss : $P_{con} = I_{OUT}^2 \times R_{onH} \times V_{OUT}/V_{CC}$
- 2) Switching loss: $P_{sw} = 0.41 \times 10^{-9} \times V_{CC}^2 \times I_{OUT} \times f_{sw}$
- 3) Gate charge loss : $P_{gc} = 4.88 \times 10^{-9} \times f_{sw}$
- 4) Quiescent current loss : $P_q = 0.8 \times 10^{-3} \times V_{CC}$

Where:

I_{OUT} is the output current (A) , R_{onH} is the on-resistance of the high-side MOSFET (Ω) , V_{OUT} is the output voltage (V).
 V_{CC} is the input voltage (V), f_{sw} is the switching frequency (Hz).

Therefore

Power dissipation of IC is the sum of above dissipation.

$$P_d = P_{con} + P_{sw} + P_{gc} + P_q$$

$$\text{For given } T_j, T_j = T_a + \theta_{ja} \times P_d$$

Where:

P_d is the total device power dissipation (W), T_a is the ambient temperature (°C)

T_j is the junction temperature (°C), θ_{ja} is the thermal resistance of the package (°C)

● I/O equivalent circuit

Pin. No	Pin Name	Pin Equivalent Circuit	Pin. No	Pin Name	Pin Equivalent Circuit
6 2 1 5	Lx GND BST VCC		4	EN	
3	FB				

Figure 47. I/O equivalent circuit

●Notes for use

- (1) About Absolute Maximum Rating
When the absolute maximum ratings of application voltage, operating temperature range, etc. was exceeded, there is possibility of deterioration and destruction. Also, the short Mode or open mode, etc. destruction condition cannot be assumed. When the special mode where absolute maximum rating is exceeded is assumed, please give consideration to the physical safety countermeasure for the fuse, etc.
- (2) About GND Electric Potential
In every state, please make the electric potential of GND Pin into the minimum electrical potential. Also, include the actual excessive effect, and please do it such that the pins, excluding the GND Pin do not become the voltage below GND.
- (3) About Heat Design
Consider the Power Dissipation (Pd) in actual state of use, and please make Heat Design with sufficient margin.
- (4) About short circuit between pins and erroneous mounting
When installing to set board, please be mindful of the direction of the IC, phase difference, etc. If it is not installed correctly, there is a chance that the IC will be destroyed. Also, if a foreign object enters the middle of output, the middle of output and power supply GND, etc., even for the case where it is shorted, there is a change of destruction.
- (5) About the operation inside a strong electro-magnetic field
When using inside a strong electro-magnetic field, there is a possibility of error, so please be careful.
- (6) About checking with Set boards
When doing examination with the set board, during connection of capacitor to the pin that has low impedance, there is a possibility of stress in the IC, so for every 1 process, please make sure to do electric discharge. As a countermeasure for static electricity, in the process of assembly, do grounding, and when transporting or storing please be careful. Also, when doing connection to the jig in the examination process, please make sure to turn off the power supply, then connect. After that, turn off the power supply then take it off.
- (7) About common impedance
For the power supply and the wire of GND, lower the common impedance, then, as much as possible, make the ripple smaller (as much as possible make the wire thick and short, and lower the ripple from $L \cdot C$), etc., then and please consider it sufficiently.
- (8) In the application, when the mode where the VCC and each pin electrical potential becomes reversed exists, there is a possibility that the internal circuit will become damaged. For example, during cases wherein the condition when charge was given in the external capacitor, and the VCC was shorted to GND, it is recommended to insert the bypass diode to the diode of the back current prevention in the VCC series or the middle of each Pin-VCC.
- (9) About IC Pin Input
This IC is a Monolithic IC, and between each element, it has P⁺ isolation for element separation and P board. With the N layer of each element and this, the P-N junction is formed, and the parasitic element of each type is composed.
For example, like the diagram below, when resistor and transistor is connected to Pin,
○When $GND > (PinA)$ in Resistor, when $GND > (PinA)$, when $GND > (PinB)$ in Transistor (NPN), the P-N junction will operate as a parasitic diode.
○Also, during $GND > (Pin B)$ in the Transistor (NPN), through the N layer of the other elements connected to the above-mentioned parasitic diode, the parasitic NPN Transistor will operation.
On the composition of IC, depending on the electrical potential, the parasitic element will become necessary. Through the operation of the parasitic element interference of circuit operation will arouse, and error, therefore destruction can be caused. Therefore please be careful about the applying of voltage lower than the GND (P board) in I/O Pin, and the way of using when parasitic element operating.

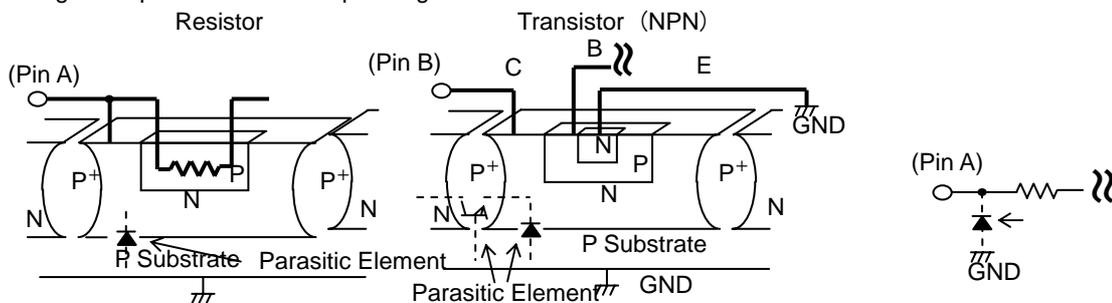


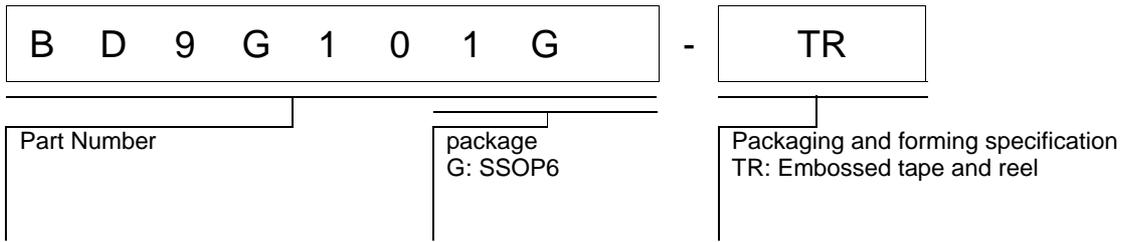
Figure 48. Example of simple structure of Bipolar IC

Status of this document

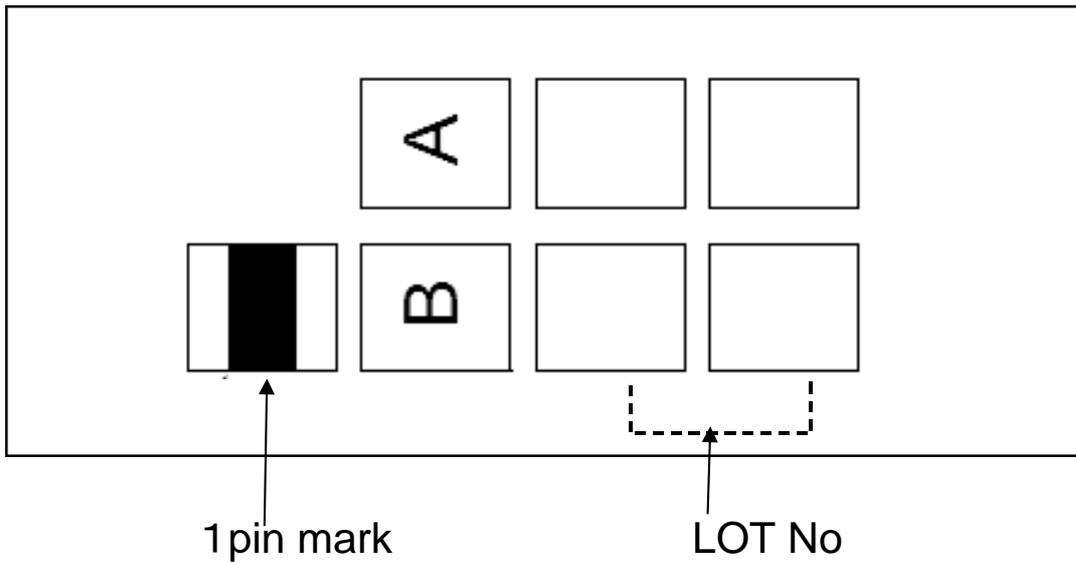
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

● Ordering part number



● External information



SSOP6

SSOP6

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

*Order quantity needs to be multiple of the minimum quantity.

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4) The Products are not subject to radiation-proof design.
- 5) Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8) Confirm that operation temperature is within the specified range described in the product specification.
- 9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

- 1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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- 1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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