General Description

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator, and the MAX13047E is a dual-channel translator. Externally applied voltages, V_{CC} and V_L, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction (V_L↔V_{CC}) on any single data line. The MAX13046E/MAX13047E accept V_L from +1.1V to the minimum of either +3.6V or (V_{CC} + 0.3V), and V_{CC} from +1.65V to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1µA thermal short-circuit protection, and \pm 15kV ESD protection on the V_{CC} side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when pushpull driving is used.

The MAX13046E is available in a 6-pin μ DFN package, and the MAX13047E is available in a 10-pin UTQFN. Both devices are specified over the extended -40°C to +85°C operating temperature range.

Applications

I²C and 1-Wire[®] Level Translation CMOS Logic-Level Translation Cell Phones Portable Devices

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Typical Application Circuits appear at end of data sheet.

_Features

- Bidirectional Level Translation
- Operation Down to +1.1V on VL
- Ultra-Low Supply Current in Shutdown Mode 1µA (max)
- ♦ Guaranteed Push-Pull Driving Data Rate 8Mbps (+1.2V ≤ V_L ≤ +3.6V, V_{CC} ≤ +5.5V) 16Mbps (+1.8V ≤ V_L ≤ V_{CC} ≤ +3.3V)
- Extended ESD Protection on the I/O V_{CC} Lines ±15kV Human Body Model ±15kV IEC61000-4-2 Air-Gap Discharge Method ±8kV IEC61000-4-2 Contact Discharge
- Low Supply Current
- Short-Circuit Protection
- ♦ Space-Saving µDFN and UTQFN Packages

Pin Configurations



Ordering Information/Selector Guide

PART	PIN-PACKAGE	NUMBER OF CHANNELS	TOP MARK
MAX13046EELT+	6 µDFN (1mm x 1.5mm)	1	OC
MAX13047EEVB+	10 UTQFN (1.4mm x 1.8mm)	2	AAC

Note: All devices are specified over the extended -40°C to +85°C operating temperature range. +Denotes a lead-free/RoHS-compliant package.

EP = Exposed pad.

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V _{CC} 0.3V to +6V	
VL0.3V to +4V	
1/O V _{CC} 0.3V to (V _{CC} + 0.3V)	
I/O VL0.3V to (VL + 0.3V)	
SHDN	
Short-Circuit Duration I/O VL, I/O VCC to GNDContinuous	
Power Dissipation ($T_A = +70^{\circ}C$)	
6-Pin µDFN (derate 2.1mW/°C above +70°C)168mW	
10-Pin UTQFN (derate 6.9mW/°C above +70°C)559mW	

Junction-to-Ambient Thermal Resistance (θ_{JA})	(Note 1)
6-Pin μDFN	477°C/W
10-Pin UTQFN	20.1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JC})	(Note 1)
6-Pin μDFN	20.1°C/W
10-Pin UTQFN	143.1°C/W
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maxim-ic.com/thermal-tutorial</u>.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +1.65V \text{ to } +5.5V, V_{L} = +1.1V \text{ to minimum of either } +3.6V \text{ or } ((V_{CC} + 0.3V)), I/O V_{L} \text{ and } I/O V_{CC} \text{ are unconnected}, T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $V_{L} = +1.8V \text{ at } T_{A} = +25^{\circ}C$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
POWER SUPPLY		·				
V. Supply Banga	\ <i>\</i> .	$V_{CC} > 3.3V$	1.1		3.6V	V
V _L Supply Range	VL	$V_{CC} \le 3.3V$	1.1	Vc	C + 0.3V	v
V _{CC} Supply Range	V _{CC}		1.65		5.5	V
Supply Current from V _{CC}	IQVCC				10	μΑ
Supply Current from V_L	IQVL				15	μA
V _{CC} Shutdown-Mode Supply Current	ISD-VCC	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.03	1	μA
V _L Shutdown-Mode Supply Current	I _{SD-VL}	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.03	1	μA
I/O V _L and I/O V _{CC} Shutdown-Mode Leakage Current	ISD-LKG	$T_A = +25^{\circ}C, \overline{SHDN} = GND$		0.02	0.5	μA
SHDN Input Leakage		$T_A = +25^{\circ}C$		0.02	0.1	μΑ
ESD PROTECTION						
		Human Body Model		±15V		
I/O V _{CC} (Note 4)		IEC 61000-4-2 Air-Gap Discharge		±15V		kV
		IEC 61000-4-2 Contact Discharge		±8V		
All Other Pins		Human Body Model		±2		kV
LOGIC-LEVEL THRESHOLDS						
I/O V _L Input-Voltage High	VIHL		V _L - 0.2			V
I/O VL Input-Voltage Low	VILL				0.15	V

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +1.65V \text{ to } +5.5V, V_L = +1.1V \text{ to minimum of either } +3.6V \text{ or } ((V_{CC} + 0.3V)), I/O V_L \text{ and } I/O V_{CC} \text{ are unconnected}, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted}. Typical values are V_{CC} = +3.3V, V_L = +1.8V \text{ at } T_A = +25^{\circ}C.)$ (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
I/O V _{CC} Input-Voltage High	VIHC		V _{CC} - 0.4			V
I/O V _{CC} Input-Voltage Low	VILC				0.15	V
I/O V _L Output-Voltage High	V _{OHL}	I/O V _L source current = 20μ A, V _{I/O VCC} > V _{CC} - 0.4V	0.67 x VL			V
I/O V _L Output-Voltage Low	Voll	$I/O V_L sink current = 1mA, V_{I/O VCC} < 0.15V$			0.4	V
I/O V _{CC} Output-Voltage High	VOHC	I/O V _{CC} source current = 20 μ A, V _{I/O VL} > V _L - 0.2V	0.67 x V _{CC}			V
I/O V _{CC} Output-Voltage Low	Volc	$I/O V_{CC}$ sink current = 1mA, $V_{I/O VL} < 0.15V$			0.4	V
	Mar .	VL > 1.2				V
SHDN Input-Voltage High	VIH-SHDN	$1.1 \le V_L < 1.2$	V _L - 0.1			v
SHDN Input-Voltage Low	VIL-SHDN				0.15	V
I/O VL-to-I/O V _{CC} Resistance				80	250	Ω
V _{CC} Shutdown Threshold Low	VTH_L_VCC	V_{CC} falling, $V_L = +3.3V$	0.5	0.8	1.1	V
V _{CC} Shutdown Threshold High	VTH_H_VCC	V_{CC} rising, $V_L = +3.3V$	0.3	0.6	0.9	V
V _L Shutdown Threshold	V _{TH_VL}		0.35	0.75	1.06	V
Pullup Resistance		$V_{CC} = V_{L} = +3.3V$	6	10	15.5	kΩ
RISE/FALL-TIME ACCELERATOR ST	AGE					
Accelerator Pulse Duration				20		ns
I/O V _L Output-Accelerator Source Impedance		$V_L = 1.7V$		13		Ω
I/O V _{CC} Output-Accelerator Source Impedance		V _{CC} = 2.2V		17		Ω
I/O V _L Output-Accelerator Source Impedance		V _L = 3.2V		6		Ω
I/O V _{CC} Output-Accelerator Source Impedance		V _{CC} = 3.6V		10		Ω

TIMING CHARACTERISTICS FOR +1.2V \leq VL \leq MINIMUM OF EITHER +3.6V OR (V_{CC} + 0.3V)

 $(V_{CC} \le \pm 5.5V, +1.2V \le V_L \le \text{minimum of either } +3.6V \text{ or } ((V_{CC} + 0.3V)), R_S = 50\Omega, R_L = 1M\Omega, C_L = 15pF, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.}$ Typical values are $V_{CC} = +3.3V, V_L = +1.8V \text{ at } T_A = +25^{\circ}C.$ (Notes 2, 3, 5)

PARAMETER	SYMBOL	CON	DITIONS	MIN	ТҮР	МАХ	UNITS
	t	Push-pull driving, Figure 1a			7	25	
I/O V _{CC} Rise Time	tRVCC	Open-drain driving, Figure 1c			170	400	ns
		Push-pull driving,	Figure 1a		6	37	
I/O V _{CC} Fall Time	tFVCC	Open-drain drivin	ig, Figure 1c		20	50	ns
		Push-pull driving,	Figure 1b		8	30	
I/O V _L Rise Time	^t RVL	Open-drain driving, Figure 1d			180	400	ns
		Push-pull driving, Figure 1			3	56	ns
I/O V _L Fall Time	tFVL	Open-drain driving, Figure 1d			30	60	
		Driving I/O VL	Push-pull driving		5	30	ns
	^t PD-VL-VCC		Open-drain driving		210	1000	
Propagation Delay		Driving I/O V _{CC}	Push-pull driving		4	30	
	^t PD-VCC-VL		Open-drain driving		190	1000	
		Each translator	Push-pull driving			20	
Channel-to-Channel Skew	tskew	equally loaded	Open-drain driving			50	ns
Mayimy m Data Data		Push-pull driving		8			Mbps
Maximum Data Rate		Open-drain drivin	g	500			kbps

TIMING CHARACTERISTICS FOR +1.1V \leq VL \leq +1.2V

 $(V_{CC} \le \pm 5.5V, +1.1V \le V_L \le +1.2V, R_S = 50\Omega, R_L = 1M\Omega, C_L = 15pF, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted. Typical values are } V_{CC} = +3.3V, V_L = +1.8V \text{ at } T_A = +25^{\circ}C.) \text{ (Notes 2, 3, 5)}$

PARAMETER	SYMBOL	CON	IDITIONS	MIN	ТҮР	МАХ	UNITS
	t	Push-pull driving, Figure 1a			7	200	
I/O V _{CC} Rise Time	trvcc	Open-drain driving, Figure 1c			170	400	ns
		Push-pull driving,	Figure 1a		6	37	
I/O V _{CC} Fall Time	tencc tenco	Open-drain drivin	g, Figure 1c		20	50	ns
		Push-pull driving,	Figure 1b		8	30	
I/O V _L Rise Time	^t RVL	Open-drain driving, Figure 1d			180	400	ns
		Push-pull driving,	Figure 1		3	30	
I/O V _L Fall Time	tFVL	Open-drain driving, Figure 1d			30	60	ns
	tpd-vl-vcc	: Driving I/O V _L	Push-pull driving		5	200	
Draw and the Dalay			Open-drain driving		210	1000	ns
Propagation Delay		Driving I/O V _{CC}	Push-pull driving		4	200	
	^t PD-VCC-VL		Open-drain driving		190	1000	
		Each translator	Push-pull driving			20	
Channel-to-Channel Skew	^t SKEW	equally loaded	Open-drain driving			50	ns
Maximum Data Data		Push-pull driving		1.2			Mbps
Maximum Data Rate		Open-drain drivin	g	500			kbps

TIMING CHARACTERISTICS FOR +1.8V \leq VL \leq VCC \leq +3.3V

 $(+1.8V \le V_L \le V_{CC} \le +3.3V, R_S = 50\Omega, R_L = 1M\Omega, C_L = 15pF, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $V_L = +1.8V$ at $T_A = +25^{\circ}C$.) (Notes 2, 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
I/O V _{CC} Rise Time	t RVCC	Push-pull driving, Figure 1a			15	ns
I/O V _{CC} Fall Time	t FVCC	Push-pull driving, Figure 1a			15	ns
I/O V _L Rise Time	t _{RVL}	Push-pull driving, Figure 1b			15	ns
I/O V _L Fall Time	tFVL	Push-pull driving, Figure 1b			15	ns
Propagation Dalay	tpd-vl-vcc	Push-pull driving, driving I/O V_L			15	20
Propagation Delay	tpd-vcc-vl	Push-pull driving, driving I/O V _{CC}			15	ns
Channel-to-Channel Skew	^t SKEW	Push-pull driving, each translator equally loaded			10	ns
Maximum Data Rate		Push-pull driving	16			Mbps

Note 2: All units are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ does not damage the device.

Note 4: ESD protection is guaranteed by design. To ensure maximum ESD protection, place a 1µF ceramic capacitor between V_{CC} and GND. See *Typical Application Circuits*.

Note 5: Timing is measured using 10% of input to 90% of output.



MAX13046E/MAX13047E

Typical Operating Characteristics (continued)

 $(V_{CC} = +3.3V, V_L = +1.8V, R_L = 1M\Omega, C_L = 15pF$, push-pull driving data rate = 8Mbps, $T_A = +25^{\circ}C$, unless otherwise noted.)



MAX13046E Pin Description

MAX13046E		FUNCTION
μDFN	NAME	
1	VL	V_L Input Supply Voltage. Bypass V_L with a 0.1 μ F ceramic capacitor located as close as possible to the input.
2	GND	Ground
3	I/O V _L	Input/Output. Referenced to VL.
4	I/O V _{CC}	Input/Output. Referenced to V _{CC} .
5	SHDN	Shutdown Input. Drive SHDN high to enable the device. Drive SHDN low to put the device in shutdown mode.
6	Vcc	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.

MAX13047E Pin Description

MAX13047E		FUNCTION
UTQFN	NAME	
1	I/O V _{L2}	Input/Output 2. Referenced to VL.
2	VL	V_L Input Supply Voltage. Bypass V_L with a 0.1 μF ceramic capacitor located as close as possible to the input.
3, 7	N.C.	Not Connected. Internally not connected.
4	SHDN	Enable Input. Drive SHDN high to enable the device. Drive SHDN low to put the device in shutdown mode.
5	I/O V _{CC2}	Input/Output 2. Referenced to V _{CC} .
6	V _{CC}	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.
8	I/O VCC1	Input/Output 1. Referenced to V _{CC} .
9	GND	Ground
10	I/O VL1	Input/Output 1. Referenced to VL.
	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator and the MAX13047E is a dual-channel translator. Externally applied voltages, V_{CC} and V_L, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction (V_L \leftrightarrow V_{CC}) on any single data line. The MAX13046E/MAX13047E accept V_L from +1.1V to the minimum of either +3.6V or (V_{CC} + 0.3V) and V_{CC} from

+1.65V to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1µA thermal short-circuit protection, and \pm 15kV ESD protection on the V_{CC} side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when pushpull driving is used. See the *Functional Diagram*.

_Functional Diagram



Level Translation

For proper operation, ensure that +1.65V \leq V_{CC} \leq +5.5V and +1.1V \leq V_L \leq the minimum of either +3.6V or (V_{CC} + 0.3V). During power-up sequencing, V_L \geq (V_{CC} + 0.3V) does not damage the device. The speed of the rise time accelerator circuitry limits the maximum data rate for the MAX13046E/MAX13047E to 16Mbps.

Rise-Time Accelerators

The MAX13046E/MAX13047E have an internal rise-time accelerator, allowing operation up to 16Mbps. The risetime accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To guarantee operation of the rise time accelerators the maximum parasitic capacitance should be less than 200pF on the I/O lines.

Shutdown Mode

Drive SHDN low to place the MAX13046E/MAX13047E in shutdown mode and drive SHDN high for normal operation. Activating the shutdown mode disconnects the internal $10k\Omega$ pullup resistors on the I/O V_{CC} and I/O V_L lines. This forces the I/O lines to a high-impedance

state, and decreases the supply current to less than 1µA. The high-impedance I/O lines in shutdown mode allow for use in a multidrop network. The MAX13046E/ MAX13047E have a diode from each I/O to the corresponding supply rail and GND. Therefore, when in shutdown mode, do not allow the voltage at I/O V_L to exceed (V_L + 0.3V), or the voltage at I/O V_{CC} to exceed (V_{CC} + 0.3V).

Operation with One Supply Disconnected Certain applications require sections of circuitry to be disconnected to save power. When V_L is connected and V_{CC} is disconnected or connected to ground, the device enters shutdown mode. In this mode, I/O V_L can still be driven without damage to the device; however, data does not translate from I/O V_L to I/O V_{CC}. If V_{CC} falls more than V_{TH_L_VCC} below V_L, the device disconnects the pullup resistors at I/O V_L and I/O V_{CC}. To achieve the lowest possible supply current from V_L when V_{CC} is disconnected, it is recommended that the voltage at the V_{CC} supply input be approximately equal to GND.

When V_{CC} is connected and V_L is less than V_{TH_VL}, the device enters shutdown mode. In this mode, I/O V_{CC} can still be driven without damage to the device; however, data does not translate from I/O V_{CC} to I/O V_L.



Figure 1a. Rail-to-Rail Driving I/O VL

When V_{CC} is disconnected or connected to ground, I/O V_{CC} must not be driven more than V_{CC} + 0.3V. When V_L is disconnected or connected to ground, I/O V_L must not be driven more than V_L + 0.3V.

Short-Circuit Protection

Thermal-overload detection protects the MAX13046E/ MAX13047E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature (T_J) exceeds $+150^{\circ}$ C, the device enters shutdown mode. When the device has cooled to below $+140^{\circ}$ C, normal operation resumes.

±15kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The ESD structures withstand electrostatic discharge in all states: normal



Figure 1b. Rail-to-Rail Driving I/O V_{CC}

operation, shutdown mode, and powered down. The I/O V_{CC} lines of the MAX13046E/MAX13047E are characterized for protection to the following limit:

• ±15kV using the Human Body Model

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a $1.5k\Omega$ resistor.





Figure 1c. Open-Drain Driving I/O V_L

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX13046E/MAX13047E help to design equipment that meets Level 4 of IEC 61000-4-2 without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 can be lower than that measured using the Human Body Model. Figure 3a shows the IEC 61000-4-2 model, and Figure 3b shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD contact-discharge test. The Air-Gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.



Figure 1d. Open-Drain Driving I/O V_{CC}

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1μ F ceramic capacitor. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF ceramic capacitor. Place all capacitors as close as possible to the power-supply inputs.

I²C Level Translation

The MAX13046E/MAX13047E level shifts the data present on the I/O lines between +1.1V and +5.5V, making them ideal for level translation between a low-voltage ASIC and an I²C device. A typical application involves interfacing a low-voltage microprocessor to a +3V or +5V D/A converter, such as the MAX517.

1-Wire Interface Translation

The MAX13046E/MAX13047E are ideal for level translation between a low-voltage ASIC and 1-Wire device. A



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MAX13046E/MAX13047E



Figure 2a. Human Body ESD Test Model



Figure 2b. Human Body Current Waveform

typical application involves interfacing a low-voltage microprocessor to an external memory, such as the DS2502. The maximum data rate depends on the 1-Wire device. For the DS2502, the maximum data rate is 16.3kbps. A $5k\Omega$ pullup resistor is recommended when interfacing with the DS2502.

Push-Pull vs. Open-Drain Driving

The MAX13046E/MAX13047E can be driven in a pushpull or open-drain configurations. For open-drain configuration, internal 10k Ω resistors pull up I/O V_L and I/O V_{CC} to their respective power supplies. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers.



Figure 3a. IEC 61000-4-2 ESD Test Model



Figure 3b. IEC 61000-4-2 ESD Generator Current Waveform

PCB Layout

The MAX13046E/MAX13047E require good PCB layout for proper operation and optimal rise/fall time performance. Ensure proper high-frequency PCB layout even when operating at low data rates.

Driving High-Capacitive Load

Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13046E/MAX13047E when driving the signal lines. The actual rise time is a function of the load capacitance, parasitic capacitance, the supply voltage, and the drive impedance of the MAX13046E/ MAX13047E.

Operating the MAX13046E/MAX13047E at a low data rate does **NOT** increase capacitive load driving capability.

Typical Application Circuits





Chip Information

Package Information

PROCESS: BiCMOS

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 µDFN	L611-1	<u>21-0147</u>
10 UTQFN	V101A1CN-1	<u>21-0028</u>

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	8/08	Removing future product asterisks from MAX13047, changing <i>Electrical Characteristics</i> Table, packaging changes, changing ESD information	1–4, 6, 10

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