

# DATA SHEET



## SAA7324

Digital servo processor and  
Compact Disc decoder with  
integrated DAC (CD10 II)

Product specification  
Supersedes data of 1999 May 17  
File under Integrated Circuits, IC01

2000 Jun 26



# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 1 FEATURES

- Integrated bitstream DAC with differential outputs, operating at  $96f_s$  with 3rd-order noise shaper; typical performance of  $-90$  dB signal-to-noise ratio
- Separate serial input and output interfaces allow data 'loopback' mode for use of onboard DAC with external Electronic Shock Absorption (ESA) systems
- Up to 4 times speed mode
- Low voltage operation at up to 2 times speed
- Lock-to-disc mode
- Full error correction strategy,  $t = 2$  and  $e = 4$
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- Two and four times oversampling integrated digital filter, including  $f_s$  mode
- Audio data peak level detection
- Kill interface for external DAC deactivation during digital silence
- All SAA737x (CD7) digital servo and high-level functions
- Low focus noise
- Same playability performance as SAA737x (CD7)
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support

## 3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |   |          |
|-------------|---------|---|----------|
|             | NAME    | DESCRIPTION   | VERSION  |
| SAA7324H    | QFP64   | plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm | SOT393-1 |



- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I<sup>2</sup>C-bus
- On-chip clock multiplier allows the use of 8.4672, 16.9344 or 33.8688 MHz crystals or ceramic resonators.

## 2 GENERAL DESCRIPTION

The SAA7324 (CD10 II) is a single chip combining the functions of a CD decoder, digital servo and bitstream DAC. The decoder/servo part is based on the SAA737x (CD7) and is software compatible with this design. Extra functions are controlled by use of 'shadow' registers (see Section 7.15.3).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 4 QUICK REFERENCE DATA

| SYMBOL             | PARAMETER                         | CONDITIONS                                  | MIN. | TYP.   | MAX. | UNIT |
|--------------------|-----------------------------------|---|------|--------|------|------|
| V <sub>DD</sub>    | supply voltage                    | n = 4 mode; note 1                          | 3.0  | 3.3    | 3.6  | V    |
|                    |                                   | n = 1 or 2 mode; note 1                     | 2.4  | –      | 3.6  | V    |
| I <sub>DD</sub>    | supply current                    | V <sub>DD</sub> = 3.3 V                     | –    | 20     | –    | mA   |
|                    |                                   | V <sub>DD</sub> = 2.4 V                     | –    | 14     | –    | mA   |
| f <sub>xtal</sub>  | crystal frequency                 |   | 4    | 8.4672 | 35   | MHz  |
| T <sub>amb</sub>   | ambient temperature               |   | –10  | –      | +70  | °C   |
| T <sub>stg</sub>   | storage temperature               |   | –55  | –      | +125 | °C   |
| S/N <sub>DAC</sub> | onboard DAC signal-to-noise ratio | 1 kHz; 1f <sub>s</sub> ; see Figs 38 and 39 | –85  | –90    | –    | dB   |

### Note

1. n = overspeed factor.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 5 BLOCK DIAGRAM

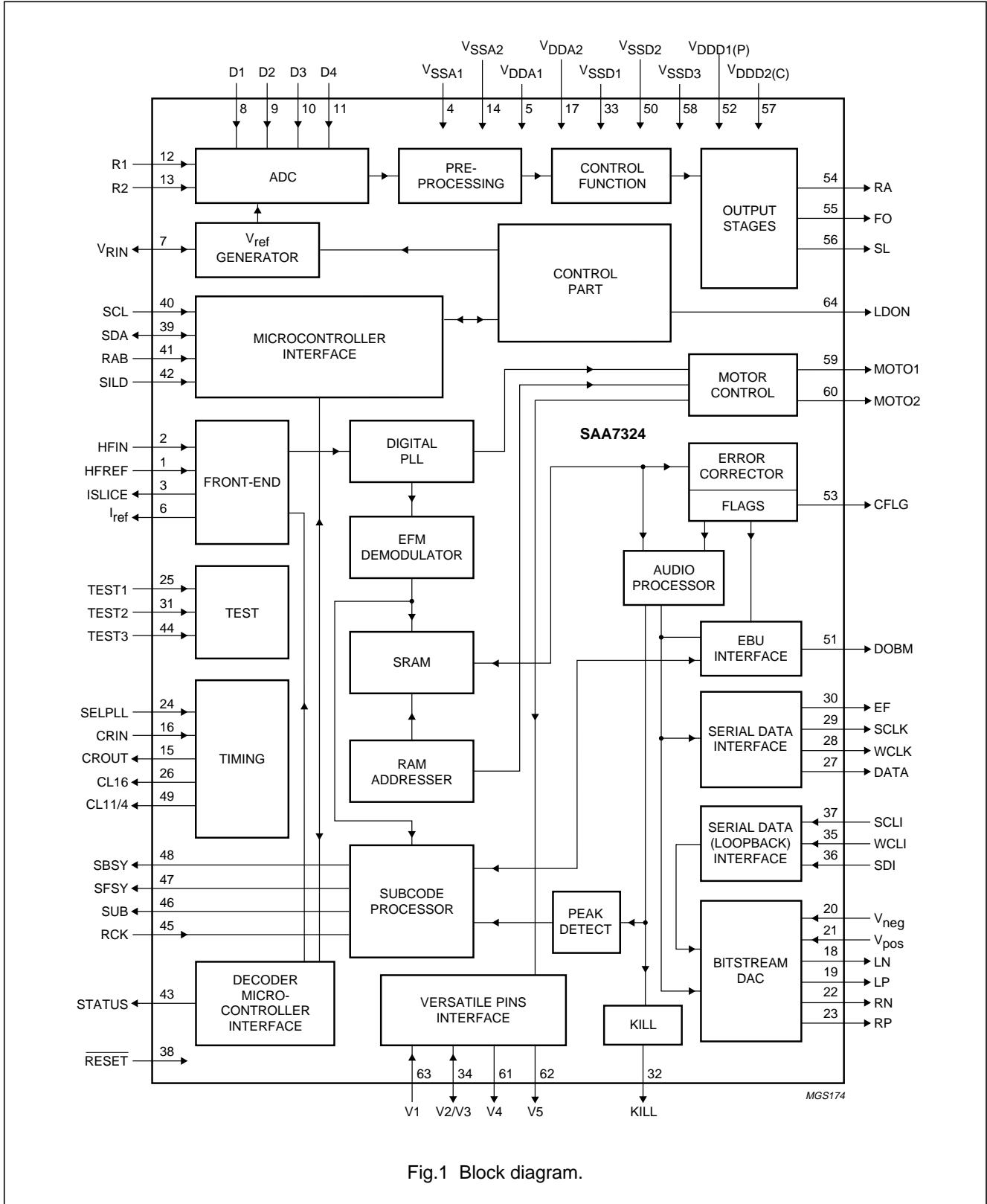


Fig.1 Block diagram.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 6 PINNING

| SYMBOL            | PIN               | DESCRIPTION   |
|-------------------|-------------------|---|
| HFREF             | 1                 | comparator common mode input  |
| HFIN              | 2                 | comparator signal input   |
| ISLICE            | 3                 | current feedback output from data slicer  |
| V <sub>SSA1</sub> | 4 <sup>(1)</sup>  | analog ground 1   |
| V <sub>DDA1</sub> | 5 <sup>(1)</sup>  | analog supply voltage 1   |
| I <sub>ref</sub>  | 6                 | reference current output  |
| V <sub>RIN</sub>  | 7                 | reference voltage for servo ADCs  |
| D1                | 8                 | unipolar current input 1 (central diode signal input)                             |
| D2                | 9                 | unipolar current input 2 (central diode signal input)                             |
| D3                | 10                | unipolar current input 3 (central diode signal input)                             |
| D4                | 11                | unipolar current input 4 (central diode signal input)                             |
| R1                | 12                | unipolar current input 1 (satellite diode signal input)                           |
| R2                | 13                | unipolar current input 2 (satellite diode signal input)                           |
| V <sub>SSA2</sub> | 14 <sup>(1)</sup> | analog ground 2   |
| CROUT             | 15                | crystal/resonator output  |
| CRIN              | 16                | crystal/resonator input   |
| V <sub>DDA2</sub> | 17 <sup>(1)</sup> | analog supply voltage 2   |
| LN                | 18                | DAC left channel differential negative output                                     |
| LP                | 19                | DAC left channel differential positive output                                     |
| V <sub>neg</sub>  | 20                | DAC negative reference input  |
| V <sub>pos</sub>  | 21                | DAC positive reference input  |
| RN                | 22                | DAC right channel differential negative output                                    |
| RP                | 23                | DAC right channel differential positive output                                    |
| SELPLL            | 24                | selects whether internal clock multiplier PLL is used                             |
| TEST1             | 25                | test control input 1 (this pin should be tied LOW)                                |
| CL16              | 26                | 16.9344 MHz system clock output   |
| DATA              | 27                | serial d4(1) data output (3-state)  |
| WCLK              | 28                | word clock output (3-state)   |
| SCLK              | 29                | serial bit clock output (3-state)   |
| EF                | 30                | C2 error flag output (3-state)  |
| TEST2             | 31                | test control input 2 (this pin should be tied LOW)                                |
| KILL              | 32                | kill output (programmable; open-drain)  |
| V <sub>SSD1</sub> | 33 <sup>(1)</sup> | digital ground 1  |
| V2/V3             | 34                | versatile I/O: versatile input 2 or versatile output 3 (open-drain)               |
| WCLI              | 35                | word clock input (for data loopback to DAC)                                       |
| SDI               | 36                | serial data input (for data loopback to DAC)                                      |
| SCLI              | 37                | serial bit clock input (for data loopback to DAC)                                 |
| RESET             | 38                | power-on reset input (active LOW)   |
| SDA               | 39                | microcontroller interface data I/O line (I <sup>2</sup> C-bus; open-drain output) |
| SCL               | 40                | microcontroller interface clock line input (I <sup>2</sup> C-bus)                 |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL               | PIN               | DESCRIPTION   |
|----------------------|-------------------|---|
| RAB                  | 41                | microcontroller interface R/W and load control line input (4-wire bus mode)               |
| SILD                 | 42                | microcontroller interface $\bar{R}/\bar{W}$ and load control line input (4-wire bus mode) |
| STATUS               | 43                | servo interrupt request line/decoder status register output (open-drain)                  |
| TEST3                | 44                | test control input 3 (this pin should be tied LOW)  |
| RCK                  | 45                | subcode clock input   |
| SUB                  | 46                | P-to-W subcode bit 3-states output (3-state)  |
| SFSY                 | 47                | subcode frame sync output (3-state)   |
| SBSY                 | 48                | subcode block sync output (3-state)   |
| CL11/4               | 49                | 11.2896 or 4.2336 MHz (for microcontroller) clock output                                  |
| V <sub>SSD2</sub>    | 50 <sup>(1)</sup> | digital ground 2  |
| DOBM                 | 51                | bi-phase mark output (externally buffered; 3-state)                                       |
| V <sub>DDD1(P)</sub> | 52 <sup>(1)</sup> | digital supply voltage 1 for periphery  |
| CFLG                 | 53                | correction flag output (open-drain)   |
| RA                   | 54                | radial actuator output  |
| FO                   | 55                | focus actuator output   |
| SL                   | 56                | sledge control output   |
| V <sub>DDD2(C)</sub> | 57 <sup>(1)</sup> | digital supply voltage 2 for core   |
| V <sub>SSD3</sub>    | 58 <sup>(1)</sup> | digital ground 3  |
| MOTO1                | 59                | motor output 1; versatile (3-state)   |
| MOTO2                | 60                | motor output 2; versatile (3-state)   |
| V4                   | 61                | versatile output 4  |
| V5                   | 62                | versatile output 5  |
| V1                   | 63                | versatile input 1   |
| LDON                 | 64                | laser drive on output (open-drain)  |

**Note**

1. All supply pins must be connected to the same external power supply voltage.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

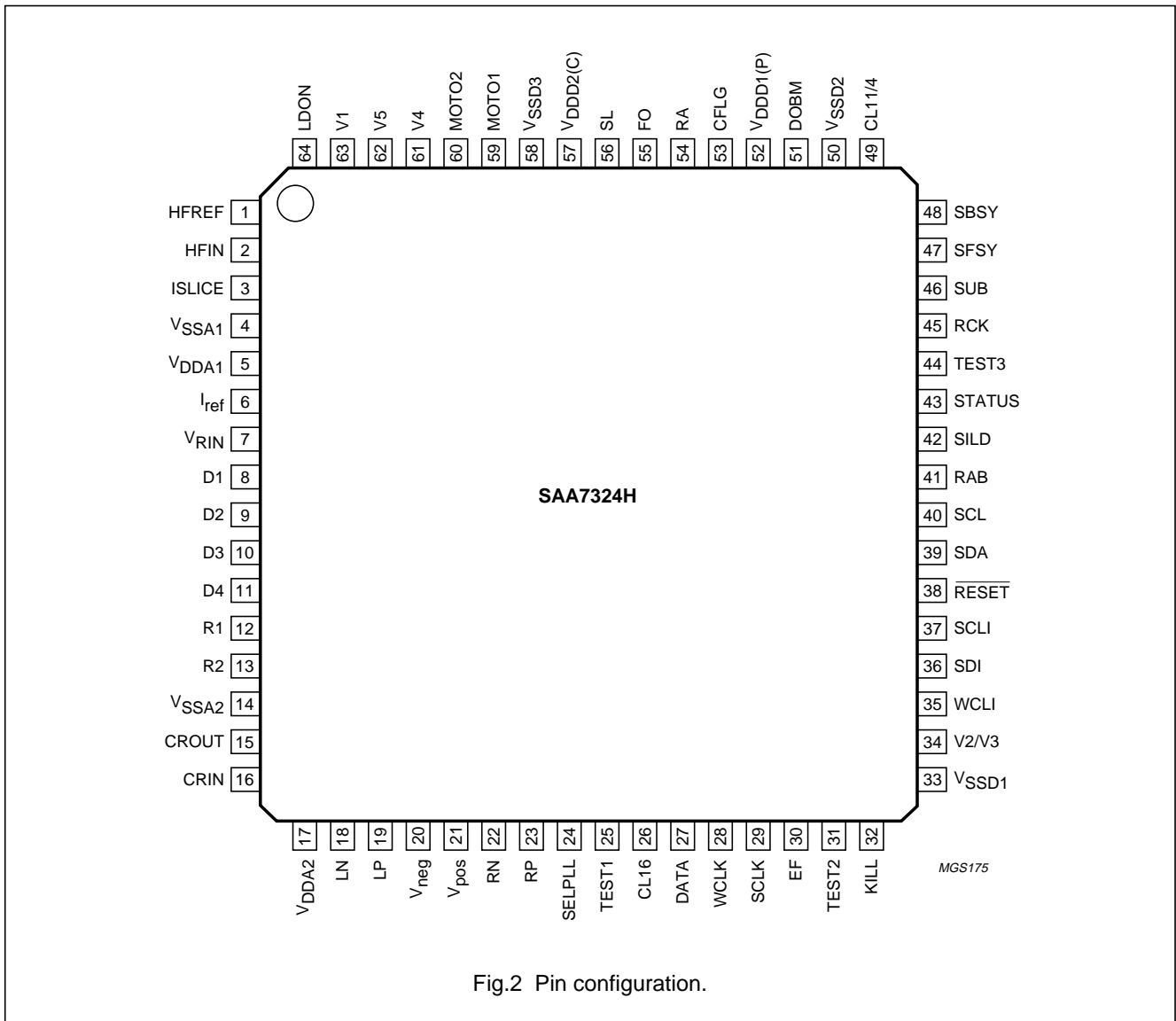


Fig.2 Pin configuration.

**7 FUNCTIONAL DESCRIPTION**

**7.1 Decoder part**

**7.1.1 PRINCIPAL OPERATING MODES OF THE DECODER**

The decoding part supports a full audio specification and can operate at two different disc speeds, from single-speed ( $n = 1$ ) to 4 times speed ( $n = 4$ ). The factor 'n' is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.7.

**7.1.2 DECODING SPEED AND CRYSTAL FREQUENCY**

The SAA7324 is a two speed decoding device, with an internal Phase-Locked Loop (PLL) clock multiplier. Depending on the crystal frequency used and the internal clock settings (selectable via decoder register B), the playback speeds shown in Table 1 are possible, where 'n' is the overspeed factor (1, 2 or 4).

An internal clock multiplier is present, controlled by SELPLL, and should only be used if a 8.4672 or 16.9344 MHz crystal, ceramic resonator or external clock is present.



## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.1.3 LOCK-TO-DISC MODE

For electronic shock absorption applications, the SAA7324 can be put into lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside-to-outside of the disc.

In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the I<sup>2</sup>S-bus (WCLK and SCLK) clocks are dependent on the disc speed. In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7324 will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled/disabled by decoder register E.

### 7.1.4 STANDBY MODES

The SAA7324 may be placed in two standby modes selected by decoder register B (it should be noted that the device core is still active):

- Standby 1: CD-STOP mode; most I/O functions are switched off

- Standby 2: CD-PAUSE mode; audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active; this is also called a 'Hot Pause'.

In the standby modes the various pins will have the following values:

- MOTO1 and MOTO2: put in high-impedance, PWM mode (standby 1 and reset: operating in standby 2); put in high-impedance, PDM mode (standby 1 and reset: operating in standby 2)
- SCL and SDA: no interaction; normal operation continues
- SCLK, WCLK, DATA, EF and DOBM: 3-state in both standby modes; normal operation continues after reset
- CRIN, CROUT, CL16 and CL11/4: no interaction; normal operation continues
- V1, V2/V3, V4, V5 and CFLG: no interaction; normal operation continues.

**Table 1** Playback speeds

| REGISTER B | REGISTER E | SELPLL | CRYSTAL FREQUENCY (MHz) |                      |        | CL11 FREQUENCY (MHz) <sup>(1)</sup> |
|------------|------------|--------|-------------------------|----------------------|--------|-------------------------------------|
|            |            |        | 33.8688                 | 16.9344              | 8.4672 |                                     |
| 00XX       | 0XXX       | 0      | n = 1                   | –                    | –      | 11.2896                             |
| 00XX       | 0XXX       | 1      | –                       | –                    | n = 1  | 11.2896                             |
| 01XX       | 0XXX       | 0      | –                       | n = 1                | –      | 5.6448                              |
| 01XX       | 0XXX       | 1      | –                       | n = 1                | –      | 11.2896                             |
| 10XX       | 0XXX       | 0      | n = 2                   | –                    | –      | 11.2896                             |
| 10XX       | 0XXX       | 1      | –                       | –                    | n = 2  | 11.2896                             |
| 11XX       | 0XXX       | 0      | –                       | n = 2 <sup>(2)</sup> | –      | 5.6448                              |
| 11XX       | 0XXX       | 1      | –                       | n = 2                | –      | 11.2896                             |
| 00XX       | 1XXX       | 0      | n = 4 <sup>(2)</sup>    | –                    | –      | 11.2896                             |
| 00XX       | 1XXX       | 1      | –                       | –                    | n = 4  | 11.2896                             |
| 01XX       | 1XXX       | 0      | –                       | n = 4 <sup>(2)</sup> | –      | 5.6448                              |
| 01XX       | 1XXX       | 1      | –                       | n = 4                | –      | 11.2896                             |

#### Notes

1. The CL11 output is always a 5.6448 MHz clock if a 16.9344 MHz external clock is used and SELPLL = 0. CL11 is available on the CL11/4 output, enabled by programming shadow register 3 (see Section 7.15.3).
2. Data capture performance is not optimized for this option.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

## SAA7324

### 7.2 Crystal oscillator

The crystal oscillator is a conventional 2-pin design operating between 8 and 35 MHz. This oscillator is capable of operating with ceramic resonators and with both fundamental and third overtone crystals. External components should be used to suppress the fundamental output of the third overtone crystals as shown in Figs 3 and 4. Typical oscillation frequencies required are 8.4672, 16.9344 or 33.8688 MHz depending on the internal clock settings used and whether or not the clock multiplier is enabled.

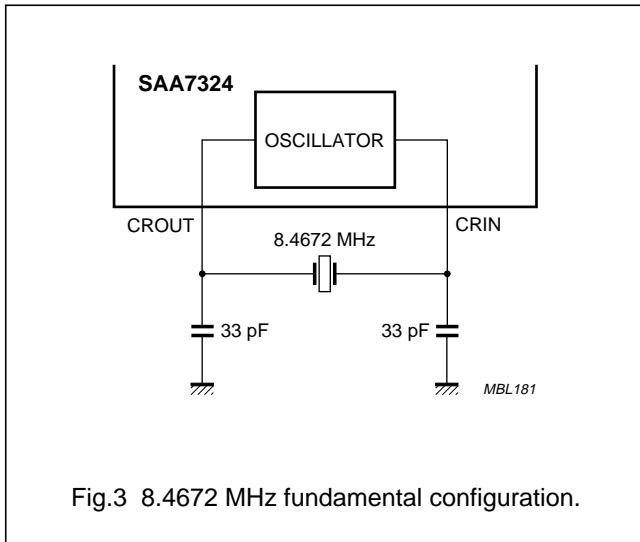


Fig.3 8.4672 MHz fundamental configuration.

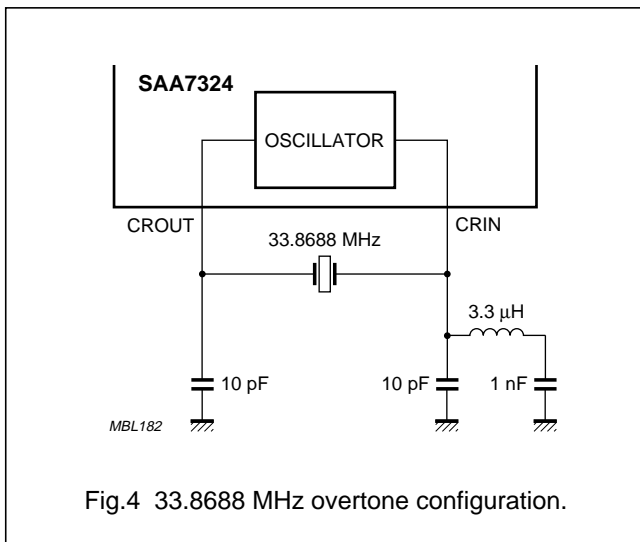


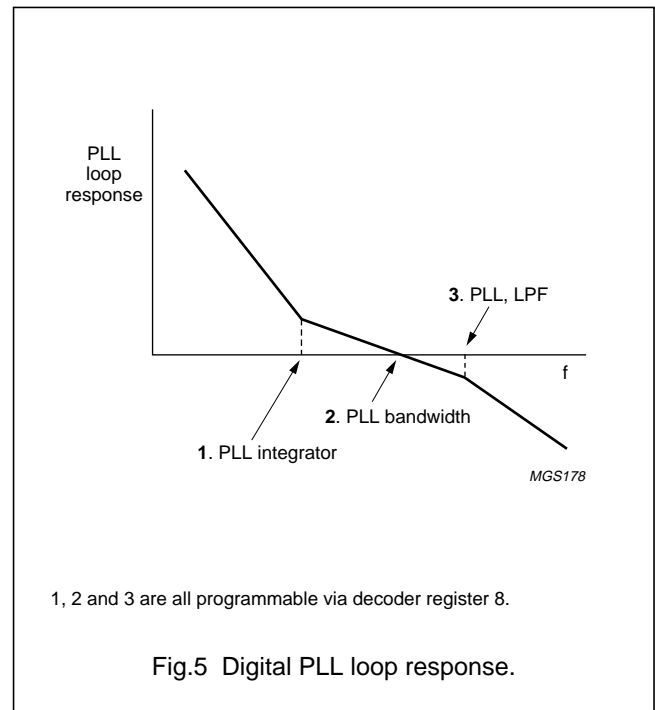
Fig.4 33.8688 MHz overtone configuration.

### 7.3 Data slicer and clock regenerator

The SAA7324 has an integrated slice level comparator which can be clocked by the crystal frequency clock, or 4 times the crystal frequency clock (if SELPLL is set HIGH while using a 16.9344 MHz crystal and register 4 is set to 0XXX), or 8 times the crystal frequency clock (if SELPLL is set HIGH while using an 8.4672 MHz crystal, and register 4 is set to 0XXX). The slice level is controlled by an internal current source applied to an external capacitor under the control of the Digital Phase-Locked Loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization. The PLL response is shown in Fig.5.

For certain applications an off-track input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc\_parm1 parameter), but may be input via the V1 pin if selected by register C. If this flag is HIGH, the SAA7324 will assume that its servo part is following on the wrong track, and will flag all incoming HF data as incorrect.

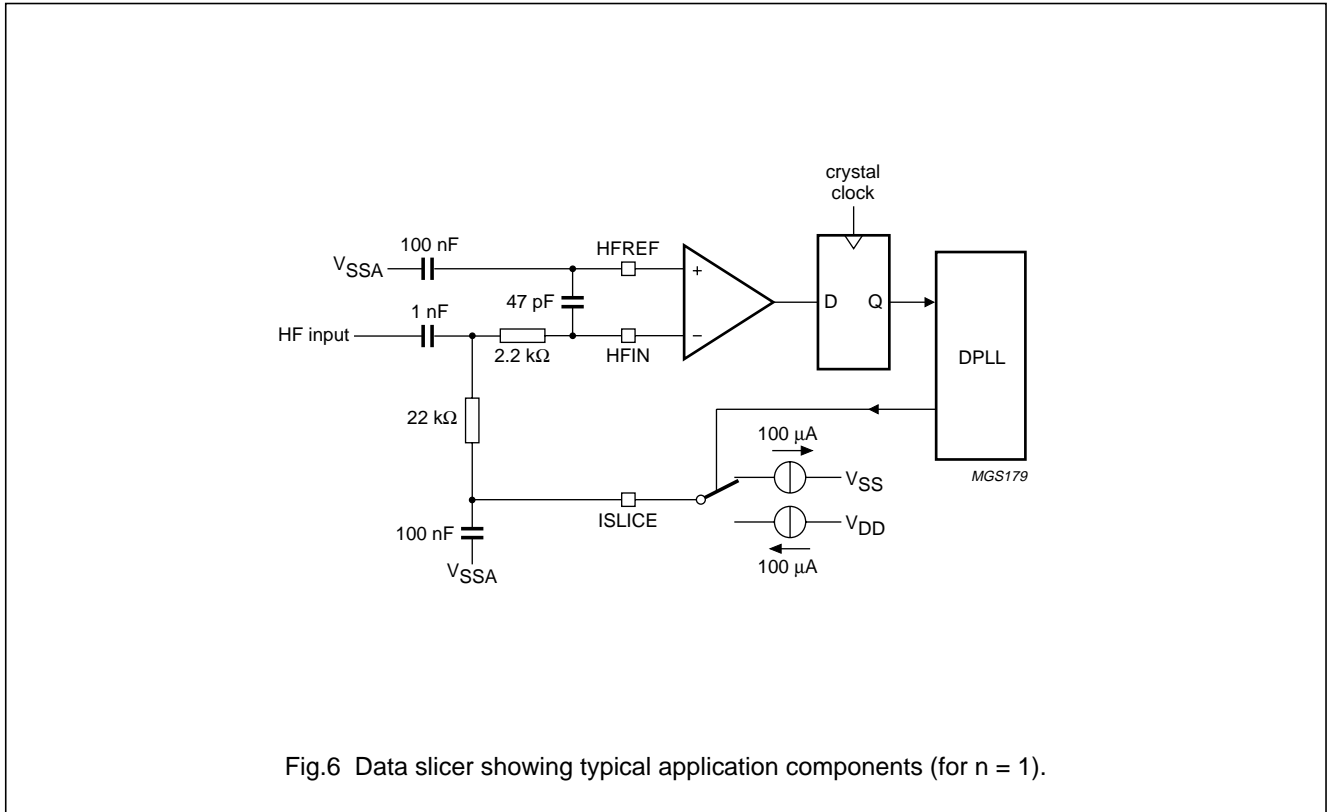


1, 2 and 3 are all programmable via decoder register 8.

Fig.5 Digital PLL loop response.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324



7.4 Demodulator

7.4.1 FRAME SYNC PROTECTION

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data.

The master counter is only reset if:

- A sync coincidence is detected; sync pattern occurs  $588 \pm 1$  EFM clocks after the previous sync pattern
- A new sync pattern is detected within  $\pm 6$  EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence is found, and reset LOW if during 61 consecutive frames no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by decoder registers 2 and 7.

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

7.4.2 EFM DEMODULATION

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

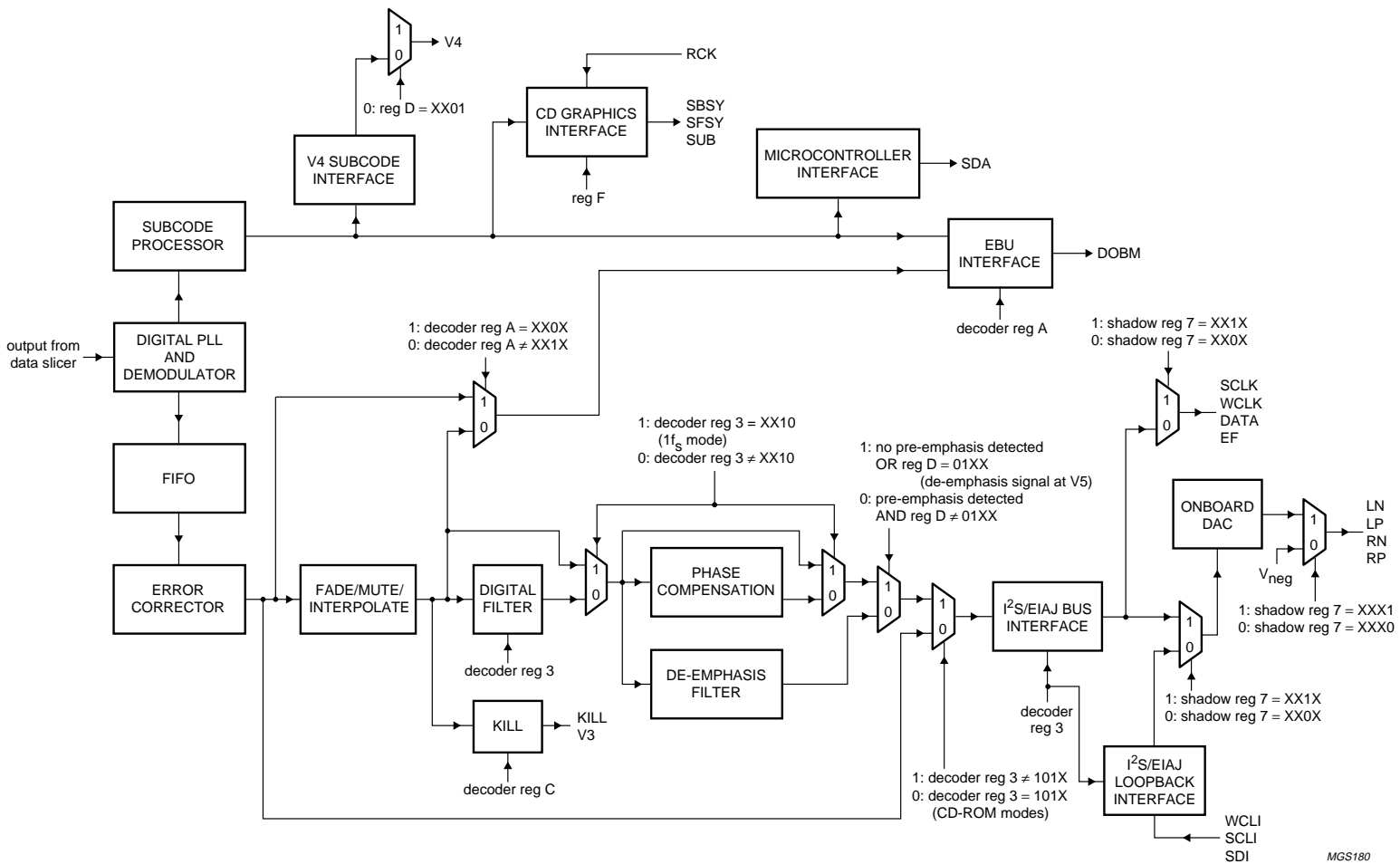


Fig.7 Simplified data flow of decoder functions.

MGS180

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

## SAA7324

### 7.5 Subcode data processing

#### 7.5.1 Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBREADY-I signal will go LOW. SUBREADY-I can be read via the SDA or STATUS pins, selected via decoder register 2. Good Q-channel data may be read from SDA.

#### 7.5.2 EIAJ 3 AND 4-WIRE SUBCODE (CD GRAPHICS) INTERFACES

Data from all the subcode channels (P-to-W) may be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3 or 4-wire interface via decoder register F.

The subcode interface output formats are illustrated in Fig.8, where the RCK signal is supplied by another device such as a CD graphics decoder.

#### 7.5.3 V4 SUBCODE INTERFACE

Data of subcode channels, Q-to-W, may be read via pin V4 if selected via decoder register D. The format is similar to RS232 and is illustrated in Fig.9. The subcode sync word is formed by a pause of  $(200/n)$   $\mu$ s minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between  $(11.3/n)$   $\mu$ s and  $(90/n)$   $\mu$ s.

The subcode data is also available in the EBU output (DOBM) in a similar format.

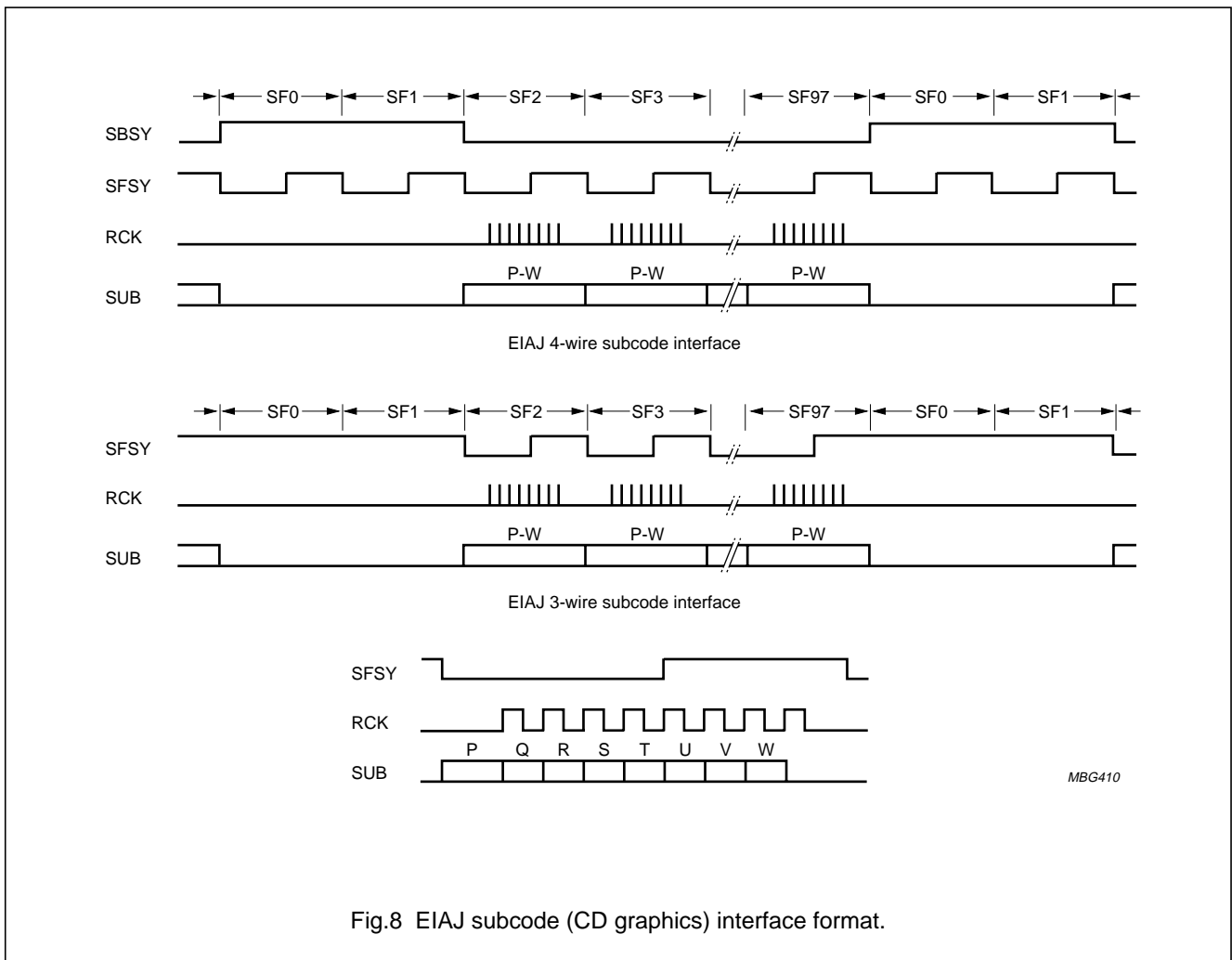
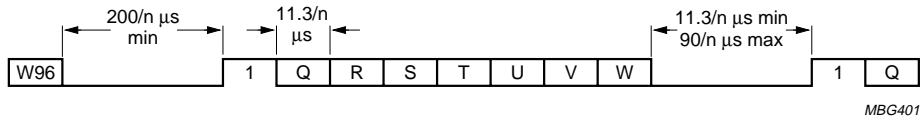


Fig.8 EIAJ subcode (CD graphics) interface format.

MBG410

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324



n = disc speed.

Fig.9 Subcode format and timing on pin V4.

7.6 FIFO and error corrector

The SAA7324 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

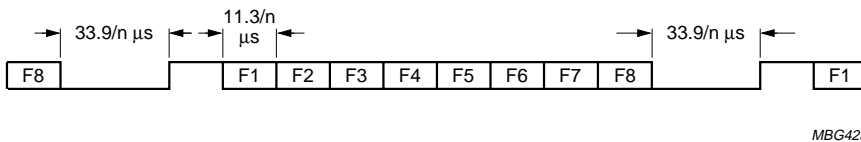
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after (de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM). The EF output will flag bytes in error in both audio and CD-ROM modes.

7.6.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG shows the status of the error corrector and interpolator and is updated every frame (7.35 × n kHz). In the SAA7324 chip a 1-bit flag is present on the CFLG pin as illustrated in Fig.10. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by decoder register A.



n = disc speed.

Fig.10 Flag output timing diagram.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

**Table 2** Output flags

| F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | DESCRIPTION                                      |
|----|----|----|----|----|----|----|----|--|
| 0  | X  | X  | X  | X  | X  | X  | X  | no absolute time sync                            |
| 1  | X  | X  | X  | X  | X  | X  | X  | absolute time sync                               |
| X  | 0  | 0  | X  | X  | X  | X  | X  | C1 frame contained no errors                     |
| X  | 0  | 1  | X  | X  | X  | X  | X  | C1 frame contained 1 error                       |
| X  | 1  | 0  | X  | X  | X  | X  | X  | C1 frame contained 2 errors                      |
| X  | 1  | 1  | X  | X  | X  | X  | X  | C1 frame uncorrectable                           |
| X  | X  | X  | 0  | 0  | X  | X  | 0  | C2 frame contained no errors                     |
| X  | X  | X  | 0  | 0  | X  | X  | 1  | C2 frame contained 1 error                       |
| X  | X  | X  | 0  | 1  | X  | X  | 0  | C2 frame contained 2 errors                      |
| X  | X  | X  | 0  | 1  | X  | X  | 1  | C2 frame contained 3 errors                      |
| X  | X  | X  | 1  | 0  | X  | X  | 0  | C2 frame contained 4 errors                      |
| X  | X  | X  | 1  | 1  | X  | X  | 1  | C2 frame uncorrectable                           |
| X  | X  | X  | X  | X  | 0  | 0  | X  | no interpolations                                |
| X  | X  | X  | X  | X  | 0  | 1  | X  | at least one 1-sample interpolation              |
| X  | X  | X  | X  | X  | 1  | 0  | X  | at least one hold and no interpolations          |
| X  | X  | X  | X  | X  | 1  | 1  | X  | at least one hold and one 1-sample interpolation |

## 7.7 Audio functions

### 7.7.1 DE-EMPHASIS AND PHASE LINEARITY

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to  $\leq \pm 1^\circ$  within the band 0 to 16 kHz. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at V5, selected via decoder register D, then the de-emphasis filter is bypassed.

### 7.7.2 DIGITAL OVERSAMPLING FILTER

For optimizing performance with an external DAC, the SAA7324 contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 3.

These attenuations do not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled  $-0.5$  dB down to avoid overflow on full-scale sine wave inputs (0 to 20 kHz).

**Table 3** Filter specification

| PASS BAND    | STOP BAND    | ATTENUATION     |
|--------------|--------------|-----------------|
| 0 to 9 kHz   | –            | $\leq 0.001$ dB |
| 19 to 20 kHz | –            | $\leq 0.03$ dB  |
| –            | 24 kHz       | $\geq 25$ dB    |
| –            | 24 to 27 kHz | $\geq 38$ dB    |
| –            | 27 to 35 kHz | $\geq 40$ dB    |
| –            | 35 to 64 kHz | $\geq 50$ dB    |
| –            | 64 to 68 kHz | $\geq 31$ dB    |
| –            | 68 kHz       | $\geq 35$ dB    |
| –            | 69 to 88 kHz | $\geq 40$ dB    |

### 7.7.3 CONCEALMENT

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.11).

In CD-ROM modes (i.e. the external DAC interface is selected to be in a CD-ROM format) concealment is not executed.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.7.4 MUTE, FULL-SCALE, ATTENUATION AND FADE

A digital level controller is present on the SAA7324 which performs the functions of soft mute, full-scale, attenuation and fade; these are selected via decoder register 0:

- Mute: signal reduced to 0 in a maximum of 128 steps; (3/n) ms
- Attenuation: signal scaled by -12 dB
- Full-scale: ramp signal back to 0 dB level; from mute takes (3/n) ms
- Fade: activates a 128 stage counter which allows the signal to be scaled up/down by 0.07 dB steps
  - 128 = full-scale
  - 120 = -0.5 dB (i.e. full-scale if oversampling filter used)
  - 32 = -12 dB
  - 0 = mute.

### 7.7.5 PEAK DETECTOR

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via pin SDA.

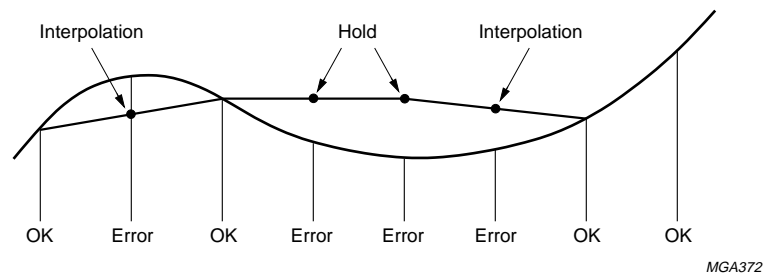


Fig.11 Concealment mechanism.



## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.8 DAC interface

#### 7.8.1 INTERNAL BITSTREAM DIGITAL-TO-ANALOG CONVERTER (DAC)

The onboard bitstream DAC operates at a clock frequency of  $96f_s$  and is designed for operation with an audio input at  $1f_s$ . Optimum performance is dependent on the application circuit used and careful consideration should be given to the recommended application circuits shown in Figs 38 and 39. The onboard DAC is controlled from shadow register 7 (see Section 7.15.3 for definition of shadow registers). This shadow register controls routing of data into the onboard DAC and also controls the DAC output pins, which can be held at zero when the onboard DAC is not required; see Table 4:

Audio data from the decoder part of the SAA7324 can be routed as described in Sections 7.8.1.1 and 7.8.1.2.

**Table 4** Shadow register

| SHADEN | SHADOW ADDRESS | REGISTER               | DATA | FUNCTION  | RESET |
|--------|----------------|------------------------|------|---|-------|
| 1      | 0111 (7H)      | control of onboard DAC | XXX0 | hold onboard DAC outputs at zero                                      | reset |
|        |                |                        | XXX1 | enable onboard DAC outputs  | –     |
|        |                |                        | XX0X | use external DAC or route audio data into onboard DAC (loopback mode) | reset |
|        |                |                        | XX1X | route audio data into onboard DAC (non-loopback mode)                 | –     |

##### 7.8.1.1 Use onboard DAC

Setting shadow register 7 to XX11 will route audio data from the CD10 decoder into the internal DAC, and enables the DAC output pins (LN, LP, RN and RP). To enable the on-board DAC, the DAC interface format (set by register 3) must be set to 16-bit  $1f_s$  mode, either I<sup>2</sup>S or EIAJ format. CD-ROM mode can also be used if interpolation is not required. The serial data output pins for interfacing with an external DAC (SCLK, WCLK, DATA and EF) are set to high-impedance.

##### 7.8.1.2 Loopback external data into onboard DAC

The onboard DAC can also be set to accept serial data inputs from an external source, e.g. an Electronic Shock Absorption (ESA) IC. This is known as loopback mode and is enabled by setting shadow register 7 to XX01.

This enables the serial data output pins (SCLK, WCLK, DATA and EF) so that data can be routed from the SAA7324 to an external ESA system (or external DAC).

The serial data from an external ESA IC can then also be input to the onboard DAC on the SAA7324 by utilising the serial data input interface (SCLI, SDI and WCLI).

In this mode, a wide range of data formats to the external ESA IC can be programmed as shown in Table 5. However, the serial input on the SAA7324 will always expect the input data from the ESA IC to be 16-bit  $1f_s$  and the same data format, either I<sup>2</sup>S-bus or EIAJ, as the serial output format (set by decoder register 3).

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.8.2 EXTERNAL DAC INTERFACE

Audio data from the SAA7324 can be sent to an external DAC, identical to the SAA737x series. This is similar to the 'loopback' mode, but in this case the internal DAC outputs can be held at zero. i.e. shadow register 7 is set to XX00. The SAA7324 is compatible with a wide range of external DACs. Eleven formats are supported and are given in Table 5. Figures 12 and 13 show the Philips I<sup>2</sup>S-bus and the EIAJ data formats respectively. When the decoder is operated in lock-to-disc mode, the SCLK frequency is dependent on the disc speed factor 'd'.

All formats are MSB first and  $f_s$  is  $(44.1 \times n)$  kHz.

The polarity of the WCLK and the data can be inverted; selectable by decoder register 7. It should be noted that EF is only a defined output in CD-ROM and  $1f_s$  modes.

When using an external DAC (or when using the onboard DAC in non-loopback mode), the serial data inputs to the onboard DAC (SCLI, SDI and WCLI) should be left unconnected.

**Table 5** DAC interface formats

| REGISTER 3 | SAMPLE FREQUENCY | NUMBER OF BITS       | SCLK (MHz)        | FORMAT   | INTERPOLATION |
|------------|------------------|----------------------|-------------------|--|---------------|
| 1010       | $f_s$            | 16                   | $2.1168 \times n$ | CD-ROM (I <sup>2</sup> S-bus)                          | no            |
| 1011       | $f_s$            | 16                   | $2.1168 \times n$ | CD-ROM (EIAJ)  | no            |
| 1110       | $f_s$            | 16/18 <sup>(1)</sup> | $2.1168 \times n$ | Philips I <sup>2</sup> S-bus 16/18 bits <sup>(1)</sup> | yes           |
| 0010       | $f_s$            | 16                   | $2.1168 \times n$ | EIAJ 16 bits   | yes           |
| 0110       | $f_s$            | 18                   | $2.1168 \times n$ | EIAJ 18 bits   | yes           |
| 0000       | $4f_s$           | 16                   | $8.4672 \times n$ | EIAJ 16 bits   | yes           |
| 0100       | $4f_s$           | 18                   | $8.4672 \times n$ | EIAJ 18 bits   | yes           |
| 1100       | $4f_s$           | 18                   | $8.4672 \times n$ | Philips I <sup>2</sup> S-bus 18 bits                   | yes           |
| 0011       | $2f_s$           | 16                   | $4.2336 \times n$ | EIAJ 16 bits   | yes           |
| 0111       | $2f_s$           | 18                   | $4.2336 \times n$ | EIAJ 18 bits   | yes           |
| 1111       | $2f_s$           | 18                   | $4.2336 \times n$ | Philips I <sup>2</sup> S-bus 18 bits                   | yes           |

#### Note

1. In this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAAT7324

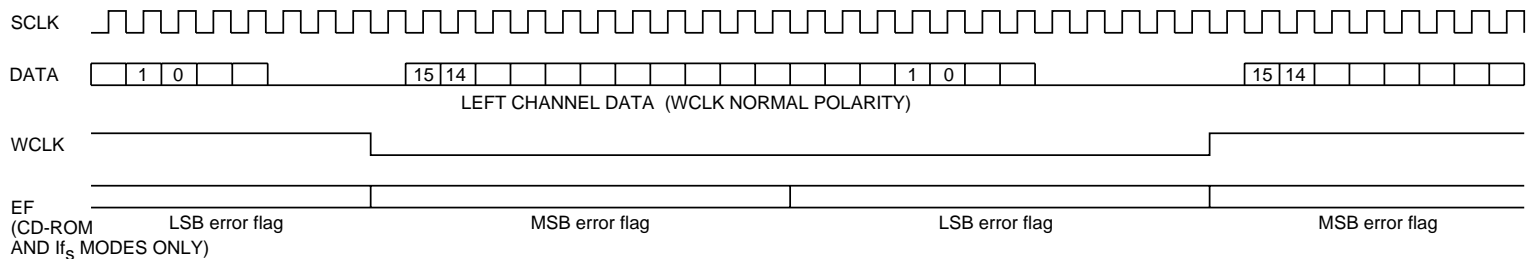


Fig.12 Philips I<sup>2</sup>S-bus data format (16-bit word length shown).

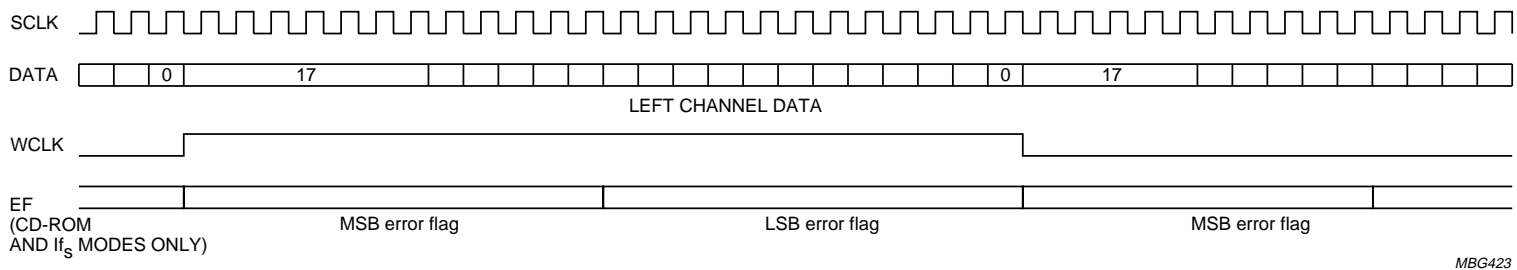


Fig.13 EIAJ data format (18-bit word length shown).

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.9 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC 958 specification. Three different modes can be selected via decoder register A:

- DOBM pin held LOW
- Data taken before concealment, mute and fade (must always be used for CD-ROM modes)
- Data taken after concealment, mute and fade.

### 7.9.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. The formats are given in Table 6.

**Table 6** Format

| FUNCTION       | BITS    | DESCRIPTION   |
|----------------|---------|---|
| Sync           | 0 to 3  | –   |
| Auxiliary      | 4 to 7  | not used; normally zero   |
| Error flags    | 4       | CFLG error and interpolation flags when selected by register A                  |
| Audio sample   | 8 to 27 | first 4 bits not used (always zero); 2's complement; LSB = bit 12, MSB = bit 27 |
| Validity flag  | 28      | valid = logic 0   |
| User data      | 29      | used for subcode data (Q-to-W)  |
| Channel status | 30      | control bits and category code  |
| Parity bit     | 31      | even parity for bits 4 to 30  |

**Table 7** Description of Table 6

| FUNCTION       | DESCRIPTION  |
|----------------|--|
| Sync           | The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B: start of a block (384 words), word contains left sample; sync M: word contains left sample (no block start) and sync W: word contains right sample. |
| Audio sample   | Left and right samples are transmitted alternately.  |
| Validity flag  | Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment.  |
| User data      | Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.   |
| Channel status | The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 8.  |

**Table 8** Bit assignment

| FUNCTION       | BITS                  | DESCRIPTION   |
|----------------|-----------------------|---|
| Control        | 0 to 3                | copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis |
| Reserved mode  | 4 to 7                | always zero   |
| Category code  | 8 to 15               | CD: bit 8 = logic 1, all other bits = logic 0   |
| Clock accuracy | 28 to 29              | set by register A; 10 = level I; 00 = level II; 01 = level III  |
| Remaining      | 6 to 27 and 30 to 191 | always zero   |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.10 KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel prior to the digital filter. The output is switched to active LOW when silence has been detected for at least 270 ms, or if mute is active, or in CD-ROM modes. Two modes are available which can be selected by decoder register C:

1. Pin KILL: KILL active LOW indicates silence detected on both left and right channels
2. Pin KILL: KILL active LOW indicates silence detected on left channel. V3 active LOW indicates silence detected on right channel.

It should be noted that when mute is active or in CD-ROM modes the output(s) are switched LOW.

### 7.11 Audio features off

The audio features can be turned off (selected by decoder register E) which affects the following functions:

- Digital filter, fade, peak detector, KILL circuit (but outputs KILL, V3 still active) are disabled
- V5 (if selected to be the de-emphasis flag output) and the EBU outputs become undefined.

It should be noted that the EBU output should be set LOW prior to switching the audio features off and after switching the audio features back on, a full-scale command should be given.

### 7.12 The versatile pins interface

The SAA7324 has four pins that can be reconfigured for different applications. One of these pins, V2/V3, can be programmed as an input (V2) or as an output (V3). Control of the V2/V3 pin is via shadow register 3; see Table 9.

Selection of the V2/V3 pin does not affect the function programmed by decoder register C i.e. the V2 or V3 pin can be changed from V2/V3 function either before or after setting the desired function via decoder register 1100. Selection of, for instance, a V3 function while the V2/V3 pin is set to V2 will not affect the V2 functionality.

The functions of these versatile pins is identical to the SAA737x series. The functions of these versatile pins is programmed by decoder registers C and D, as shown in Table 10.

**Table 9** V2 or V3 configuration

| SHADEN | ADDRESS   | REGISTER                | DATA | FUNCTION                                       | RESET |
|--------|-----------|-------------------------|------|--|-------|
| 1      | 0011 (3H) | control of V2 or V3 pin | 0XXX | V2/V3 pin configured as V2 input               | reset |
|        |           |                         | 1XXX | V2/V3 pin configured as V3 output (open-drain) |       |

**Table 10** Pin applications

| PIN NAME | PIN NUMBER | TYPE   | REGISTER ADDRESS | REGISTER DATA | FUNCTION   |
|----------|------------|--------|------------------|---------------|--|
| V1       | 63         | input  | 1100             | XXX1          | external off-track signal input  |
|          |            |        | –                | XXX0          | internal off-track signal used input may be read via decoder status bit; selected via register 2 |
| V2       | 36         | input  | –                | –             | input may be read via decoder status bit; selected via register 2                                |
| V3       | 36         | output | 1100             | XX0X          | KILL output for right channel  |
|          |            |        | –                | X01X          | output = 0   |
|          |            |        | –                | X11X          | output = 1   |
| V4       | 61         | output | 1101             | 0000          | 4-line motor drive (using V4 and V5)   |
|          |            |        | –                | XX01          | Q-to-W subcode output  |
|          |            |        | –                | XX10          | output = 0   |
|          |            |        | –                | XX11          | output = 1   |
| V5       | 62         | output | 1101             | 01XX          | de-emphasis output (active HIGH)   |
|          |            |        | –                | 10XX          | output = 0   |
|          |            |        | –                | 11XX          | output = 1   |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 7.13 Spindle motor control

### 7.13.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal  $\pm 8$  frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by decoder register 6, are supported:

- Pulse density, 2-line (true complement output),  $(1 \times n)$  MHz sample frequency
- PWM output, 2-line,  $(22.05 \times n)$  kHz modulation frequency
- PWM output, 4-line,  $(22.05 \times n)$  kHz modulation frequency
- CDV motor mode.

#### 7.13.1.1 Pulse density output mode

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal. A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower mean braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a  $(1 \times n)$  MHz internal clock signal. Possible application diagrams are illustrated in Fig.14.

#### 7.13.1.2 PWM output mode (2-line)

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig.15. A typical application diagram is illustrated in Fig.16.

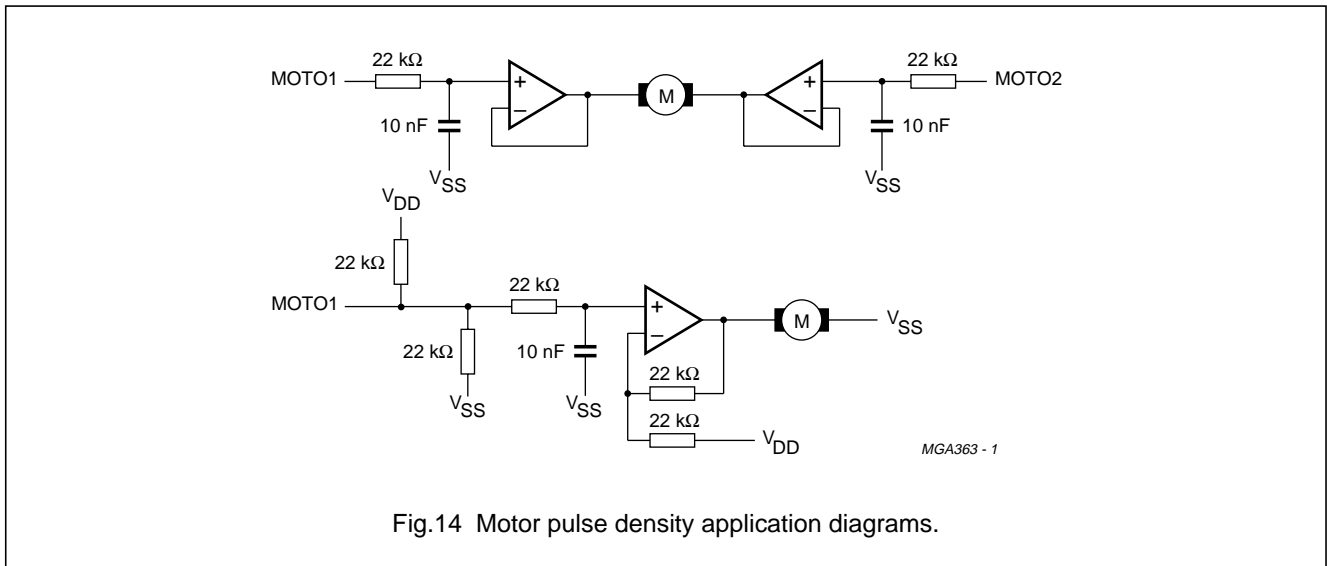


Fig.14 Motor pulse density application diagrams.

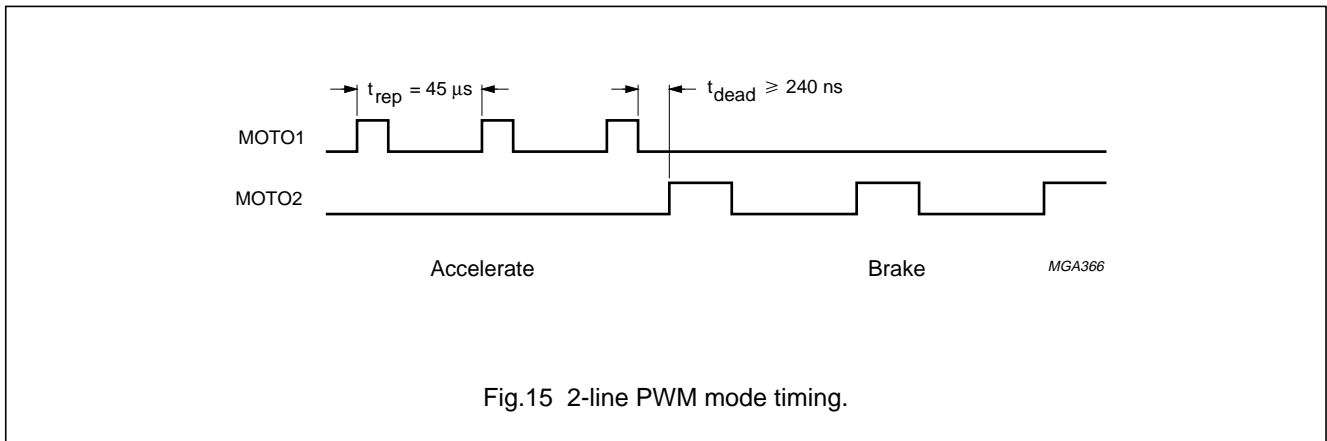


Fig.15 2-line PWM mode timing.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

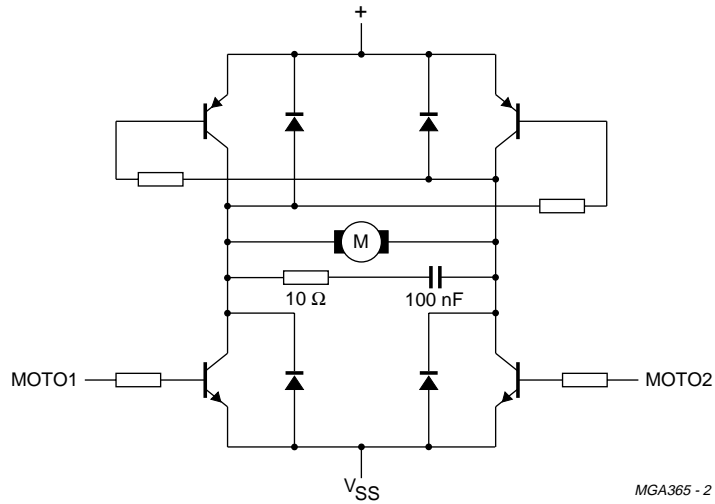


Fig.16 Motor 2-line PWM mode application diagram.

### 7.13.1.3 PWM output mode (4-line)

Using two extra outputs from the versatile pins interface, it is possible to use the SAA7324 with a 4-input motor bridge. The timing is illustrated in Fig.17. A typical application diagram is illustrated in Fig.18.

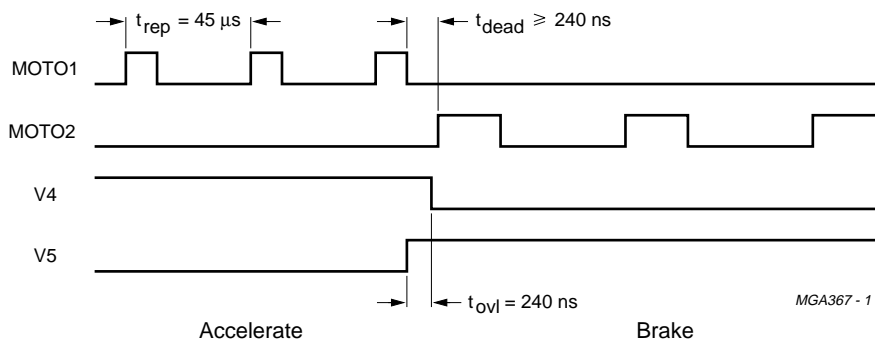


Fig.17 4-line PWM mode timing.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

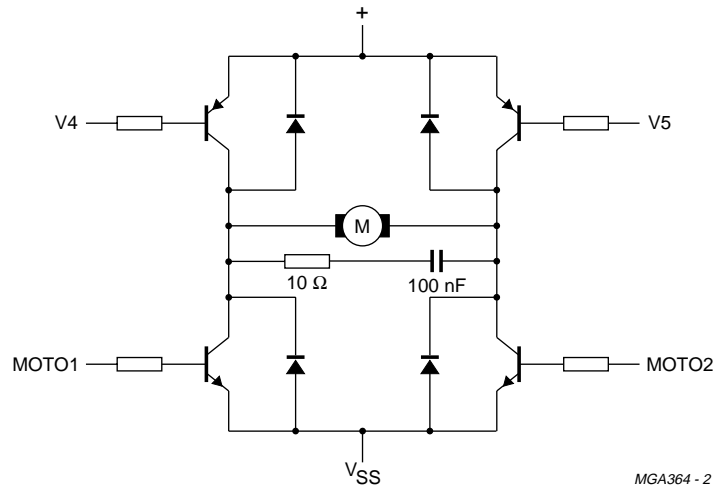


Fig.18 Motor 4-line PWM mode application diagram.

### 7.13.1.4 CDV/CAV output mode

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin [carrier frequency  $(300 \times d)$  Hz], where 'd' is the disc speed factor. The PLL frequency signal will be put in pulse-density modulated form (carrier frequency  $4.23 \times n$  MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

In the lock-to-disc (CAV) mode the CDV motor mode is the only mode that can be used to control the motor.

### 7.13.2 SPINDLE MOTOR OPERATING MODES

The operating modes of the motor servo is controlled by decoder register 1 (see Table 11).

In the SAA7324 decoder there is an anti-windup mode for the motor servo, selected via decoder register 1. When the anti-windup mode is activated the motor servo integrator will hold if the motor output saturates.

### 7.13.2.1 Power limit

In start mode 1, start mode 2, stop mode 1 and stop mode 2, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop.

The following power limits are possible:

- 100% (no power limit), 75%, 50%, or 37% of maximum.

### 7.13.3 LOOP CHARACTERISTICS

The gain and crossover frequencies of the motor control loop can be programmed via decoder registers 4 and 5. The following parameter values are possible:

- Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6 and 32
- Crossover frequency  $f_4$ :  $0.5 \times n$  Hz,  $0.7 \times n$  Hz,  $1.4 \times n$  Hz and  $2.8 \times n$  Hz
- Crossover frequency  $f_3$ :  $0.85 \times n$  Hz,  $1.71 \times n$  Hz and  $3.42 \times n$  Hz.

It should be noted that the crossover frequencies  $f_3$  and  $f_4$  are scaled with the overspeed factor 'n' whereas the gains are not.



# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 7.13.4 FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g.: as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator tries to conceal as much as possible to minimize the effect of data loss.

**Table 11** Operating modes

| MODE         | DESCRIPTION  |
|--------------|--|
| Start mode 1 | The disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller.   |
| Start mode 2 | The disc is accelerated as in start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to jump mode. The motor status signals selectable via register 2 are valid.  |
| Jump mode    | Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode. It should be noted that in the CD-ROM modes the data, on EBU and the I <sup>2</sup> S-bus is not muted.   |
| Jump mode 1  | Similar to jump mode but motor integrator is kept at zero. Used for long jumps where there is a large change in disc speed.  |
| Play mode    | FIFO released after resetting to 50%. Audio mute released.   |
| Stop mode 1  | Disc is braked by applying a negative voltage to the motor. No decisions are involved.   |
| Stop mode 2  | The disc is braked as in stop mode 1 but the PLL will monitor the disc speed. As soon as the disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to Off mode. |
| Off mode     | Motor not steered.   |

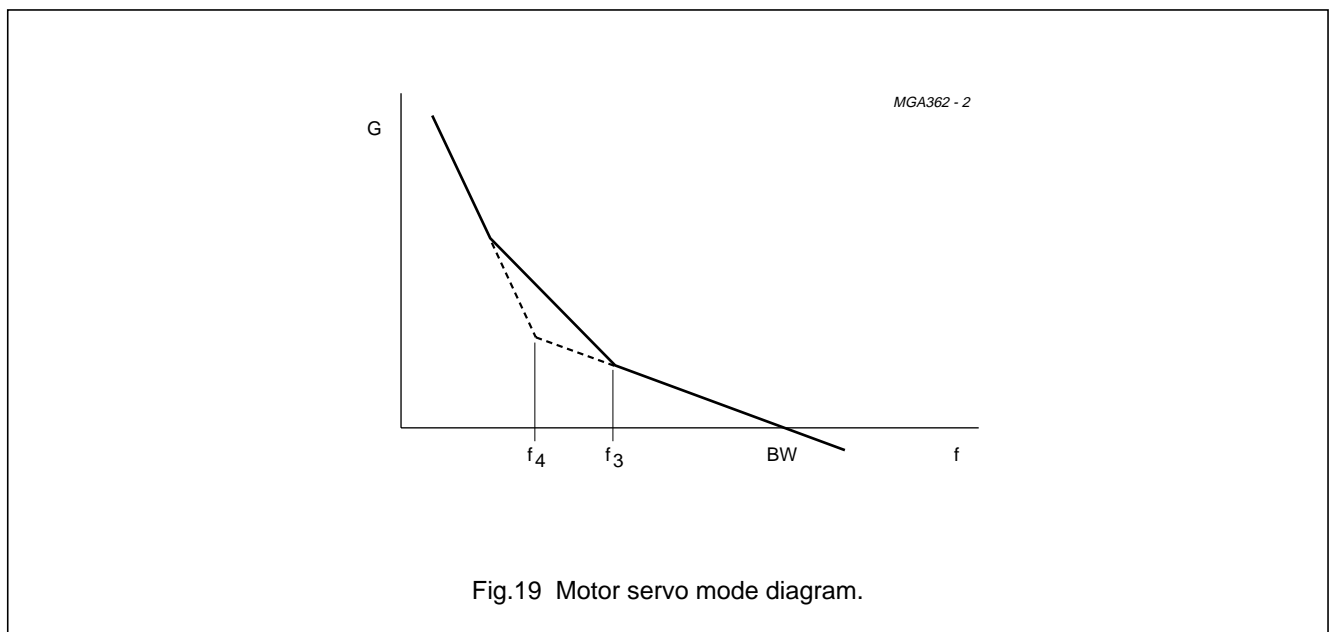


Fig.19 Motor servo mode diagram.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.14 Servo part

#### 7.14.1 DIODE SIGNAL PROCESSING

The photo detector in conventional two-stage three-beam Compact Disc systems normally contains six discrete diodes. Four of these diodes (three for single focault systems) carry the Central Aperture signal (CA) while the other two diodes (satellite diodes) carry the radial tracking information. The CA signal is processed into an HF signal (for the decoder function) and LF signal (information for the focus servo loop) before it is supplied to the SAA7324.

The analog signals from the central and satellite diodes are converted into a digital representation using Analog-to-Digital Converters (ADCs).

The ADCs are designed to convert unipolar currents into a digital code. The dynamic range of the input currents is adjustable within a given range, which is dependent on the value of the external reference current ( $I_{ref}$ ) resistor and the values programmed in shadow registers A and C.

The magnitude of the signal currents for the central aperture diodes D1 to D4 and the radial diodes R1 and R2 are programmed separately to sixteen separate current ranges.

The maximum input currents with an external 30 k $\Omega$  reference current resistor are given in Table 12.

**Table 12** Shadow register settings to control diode input current ranges

| SHADEN BIT | SHADOW REGISTER   | ADDRESS | DATA | FUNCTION  | INITIAL |
|------------|---|---------|------|---|---------|
| 1          | A<br>signal<br>magnitude<br>control for<br>diodes<br>D1 to D4 | 1010    | 0000 | (0.042). $I_{ref} = 1.006 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0001 | (0.083). $I_{ref} = 2.013 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0010 | (0.125). $I_{ref} = 3.019 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0011 | (0.167). $I_{ref} = 4.025 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0100 | (0.208). $I_{ref} = 5.031 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0101 | (0.25). $I_{ref} = 6.034 \mu\text{A}$ (nominal)   | –       |
|            |   |         | 0110 | (0.292). $I_{ref} = 7.044 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 0111 | (0.333). $I_{ref} = 8.05 \mu\text{A}$ (nominal)   | –       |
|            |   |         | 1000 | (0.375). $I_{ref} = 9.056 \mu\text{A}$ (nominal)  | –       |
|            |   |         | 1001 | (0.417). $I_{ref} = 10.063 \mu\text{A}$ (nominal) | –       |
|            |   |         | 1010 | (0.458). $I_{ref} = 11.069 \mu\text{A}$ (nominal) | –       |
|            |   |         | 1011 | (0.5). $I_{ref} = 12.075 \mu\text{A}$ (nominal)   | –       |
|            |   |         | 1100 | (0.542). $I_{ref} = 13.081 \mu\text{A}$ (nominal) | –       |
|            |   |         | 1101 | (0.583). $I_{ref} = 14.088 \mu\text{A}$ (nominal) | –       |
|            |   |         | 1110 | (0.625). $I_{ref} = 15.094 \mu\text{A}$ (nominal) | –       |
|            |   |         | 1111 | (0.667). $I_{ref} = 16.1 \mu\text{A}$ (nominal)   | reset   |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SHADEN BIT | SHADOW REGISTER  | ADDRESS | DATA | FUNCTION                                       | INITIAL |
|------------|--|---------|------|--|---------|
| 1          | C<br>signal<br>magnitude<br>control for<br>diodes<br>R1 and R2 | 1100    | 0000 | (0.042).I <sub>ref</sub> = 1.006 μA (nominal)  | –       |
|            |  |         | 0001 | (0.083).I <sub>ref</sub> = 2.013 μA (nominal)  | –       |
|            |  |         | 0010 | (0.125).I <sub>ref</sub> = 3.019 μA (nominal)  | –       |
|            |  |         | 0011 | (0.167).I <sub>ref</sub> = 4.025 μA (nominal)  | –       |
|            |  |         | 0100 | (0.208).I <sub>ref</sub> = 5.031 μA (nominal)  | –       |
|            |  |         | 0101 | (0.25).I <sub>ref</sub> = 6.034 μA (nominal)   | –       |
|            |  |         | 0110 | (0.292).I <sub>ref</sub> = 7.044 μA (nominal)  | –       |
|            |  |         | 0111 | (0.333).I <sub>ref</sub> = 8.05 μA (nominal)   | –       |
|            |  |         | 1000 | (0.375).I <sub>ref</sub> = 9.056 μA (nominal)  | –       |
|            |  |         | 1001 | (0.417).I <sub>ref</sub> = 10.063 μA (nominal) | –       |
|            |  |         | 1010 | (0.458).I <sub>ref</sub> = 11.069 μA (nominal) | –       |
|            |  |         | 1011 | (0.5).I <sub>ref</sub> = 12.075 μA (nominal)   | –       |
|            |  |         | 1100 | (0.542).I <sub>ref</sub> = 13.081 μA (nominal) | –       |
|            |  |         | 1101 | (0.583).I <sub>ref</sub> = 14.088 μA (nominal) | –       |
|            |  |         | 1110 | (0.625).I <sub>ref</sub> = 15.094 μA (nominal) | –       |
|            |  |         | 1111 | (0.667).I <sub>ref</sub> = 16.1 μA (nominal)   | reset   |

### 7.14.2 SIGNAL CONDITIONING

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal.

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set-up is assumed to be as shown in Fig.20.

In the event of single Foucault focusing method, the signal conditioning can be switched under software control such that the signal processing is as follows:

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The error signal, FE<sub>n</sub>, is further processed by a Proportional Integral and Differential (PID) filter section.

A Focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the Track-Loss (TL) generation, the focus start-up procedure and the dropout detection.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows:

$$RE_s = (R1 - R2) \times re\_gain + (R1 + R2) \times re\_offset$$

where the index 's' indicates the automatic scaling operation which is performed on the radial error signal. This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and reduces the radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start-up of the disc.

The four signals from the central aperture detectors, together with the satellite detector signals generate a Track Position Signal (TPI) which can be formulated as follows:

$$TPI = \text{sign} [(D1 + D2 + D3 + D4) - (R1 + R2) \times \text{sum\_gain}]$$

where the weighting factor sum\_gain is generated internally by the SAA7324 during initialization.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

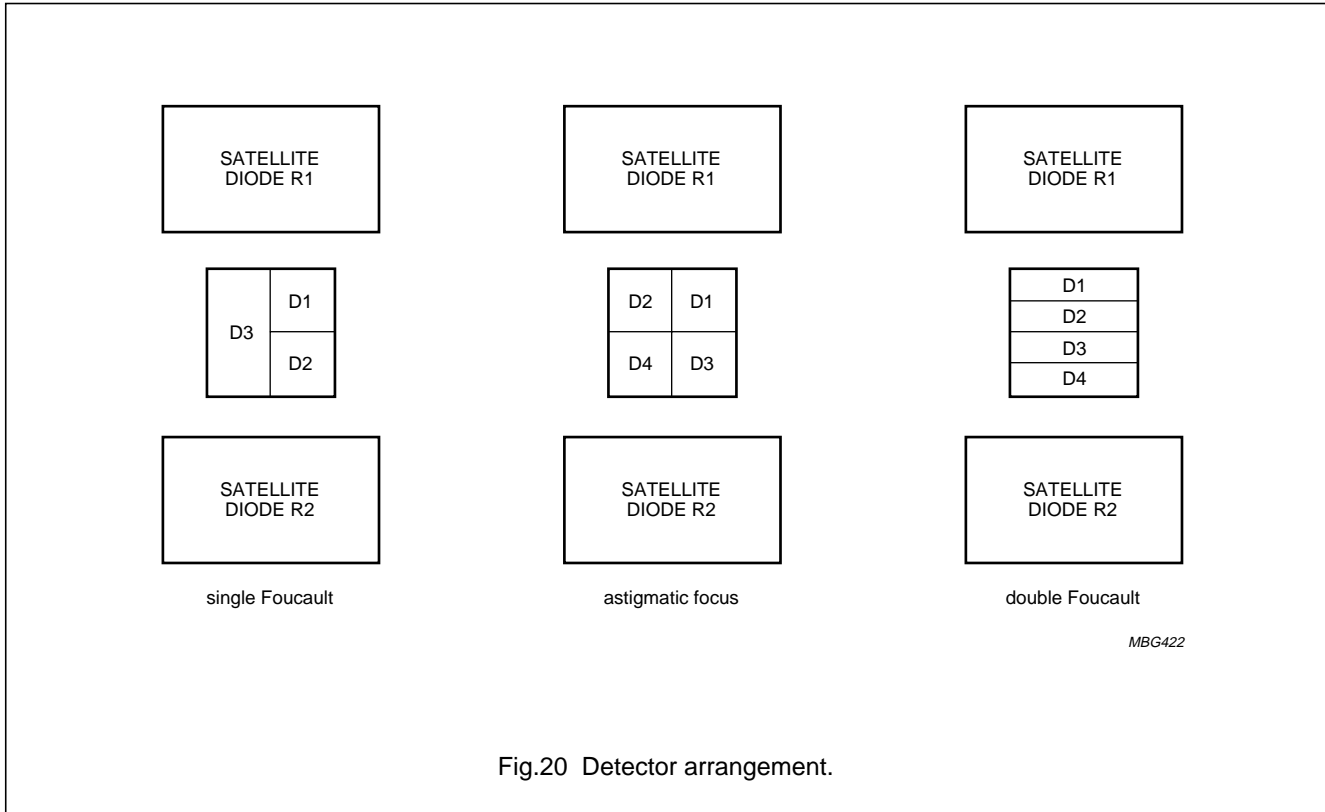


Fig.20 Detector arrangement.

7.14.3 FOCUS SERVO SYSTEM

7.14.3.1 Focus start-up

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangular voltage can be influenced by 3 parameters; for height (ramp\_height) and DC offset (ramp\_offset) of the triangle and its steepness (ramp\_incr).

For protection against false focus point detections two parameters are available which are an absolute level on the CA signal (CA\_start) and a level on the FE<sub>n</sub> signal (FE\_start). When this CA level is reached the FOK signal becomes true.

If the FOK signal is true and the level on the FE<sub>n</sub> signal is reached, the focus PID is enabled to switch-on when the next zero crossing is detected in the FE<sub>n</sub> signal.

7.14.3.2 Focus position control loop

The focus control loop contains a digital PID controller which has 5 parameters that are available to the user. These coefficients influence the integrating (foc\_int), proportional (foc\_lead\_length, part of foc\_parm3) and differentiating (foc\_pole\_lead, part of foc\_parm1) action of the PID and a digital low-pass filter (foc\_pole\_noise, part of foc\_parm2) following the PID. The fifth coefficient foc\_gain influences the loop gain.

7.14.3.3 Dropout detection

This detector can be influenced by one parameter (CA\_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.14.3.4 Focus loss detection and fast restart

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the programmed coefficients of the microcontroller.

### 7.14.3.5 Focus loop gain switching

The gain of the focus control loop (*foc\_gain*) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (*foc\_pole\_lead*) action of the PID can be switched at the same time as the gain switching is performed.

### 7.14.3.6 Focus automatic gain control loop

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

## 7.14.4 RADIAL SERVO SYSTEM

### 7.14.4.1 Level initialization

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (*re\_gain*), offset (*re\_offset*) and satellite sum gain (*sum\_gain*) for TPI level generation. The initialization procedure runs in a radial open loop situation and is  $\leq 300$  ms. This start-up time period may coincide with the last part of the motor start-up time period:

- Automatic gain adjustment: as a result of this initialization the amplitude of the RE signal is adjusted to within  $\pm 10\%$  around the nominal RE amplitude
- Offset adjustment: the additional offset in RE due to the limited accuracy of the start-up procedure is less than  $\pm 50$  nm
- TPI level generation: the accuracy of the initialization procedure is such that the duty factor range of TPI becomes  $0.4 < \text{duty factor} < 0.6$  (default duty factor = TPI HIGH/TPI period).

### 7.14.4.2 Sledge control

The microcontroller can move the sledge in both directions via the steer sledge command.

### 7.14.4.3 Tracking control

The actuator is controlled using a PID loop filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over 0.75 of the track. On request from the microcontroller, S-curve extension over 2.25 tracks is used, automatically changing to access control when exceeding those 2.25 tracks.

Both modes of S-curve extension make use of a track-count mechanism. In this mode, track counting results in an 'automatic return-to-zero track', to avoid major music rhythm disturbances in the audio output for improved shock resistance. The sledge is continuously controlled, or provided with step pulses to reduce power consumption using the filtered value of the radial PID output. Alternatively, the microcontroller can read the average voltage on the radial actuator and provide the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

### 7.14.4.4 Access

The access procedure is divided into two different modes (see Table 13), depending on the requested jump size.

**Table 13** Access modes

| ACCESS TYPE   | JUMP SIZE <sup>(1)</sup>      | ACCESS SPEED                           |
|---------------|-------------------------------|--|
| Actuator jump | 1 - <i>brake_distance</i>     | decreasing velocity                    |
| Sledge jump   | <i>brake_distance</i> - 32768 | maximum power to sledge <sup>(1)</sup> |

**Note**

1. Microcontroller presettable.

The access procedure makes use of a track counting mechanism, a velocity signal based on a fixed number of tracks passed within a fixed time interval, a velocity set point calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks remaining is greater than the *brake\_distance* then the sledge jump mode should be activated or, the actuator jump should be performed. The requested jump size together with the required sledge breaking distance at maximum access speed defines the *brake\_distance* value.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

## SAA7324

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the radial PID output. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction while the actuator becomes idle (the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated). The actuator can be electronically damped during sledge jump. The gain of the damping loop is controlled via the hold\_mult parameter.

The fast track jumping circuitry can be enabled/disabled via the xtra\_preset parameter.

### 7.14.4.5 Radial automatic gain control loop

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

This gain control differs from the level initialization. The level initialization should be performed first. The disadvantage of using the level initialization without the gain control is that only tolerances from the front-end are reduced.

### 7.14.5 OFF-TRACK COUNTING

The Track Position Signal (TPI) is a flag which is used to indicate whether the radial spot is positioned on the track, with a margin of  $\pm 1/4$  of the track-pitch. In combination with the Radial Polarity flag (RP) the relative spot position over the tracks can be determined.

These signals are, however, afflicted with some uncertainties caused by:

- Disc defects such as scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a Track Loss signal (TL) and an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the following three counting states is selected:

1. Protected state: used in normal play situations. A good protection against false detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations. In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of  $1/2\pi$  radians is affected too much, the direction cannot then be determined accurately).
3. Fast counting state: used in high velocity track jump situations. Highest obtainable velocity is the most important feature in this state.

### 7.14.6 DEFECT DETECTION

A defect detection circuit is incorporated into the SAA7324. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability. The defect detector can be switched off, applied only to focus control or applied to both focus and radial controls under software control (part of foc\_parm1).

The defect detector (see Fig.21) has programmable set points selectable by the parameter defect\_parm.

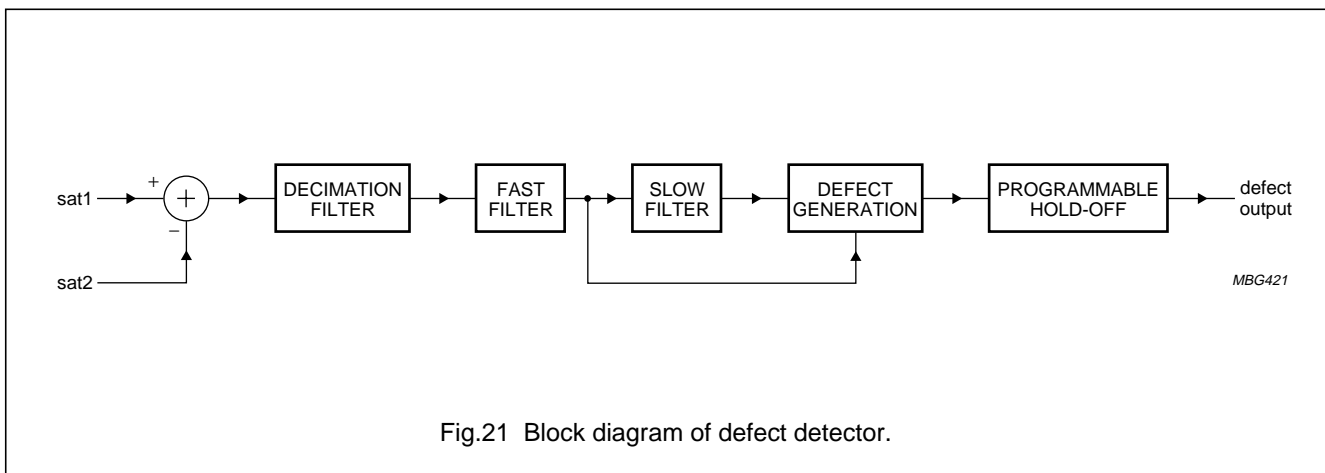


Fig.21 Block diagram of defect detector.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.14.7 OFF-TRACK DETECTION

During active radial tracking, off-track detection has been realised by continuously monitoring the off-track counter value. The off-track flag becomes valid whenever the off-track counter value is not equal to zero. Depending on the type of extended S-curve, the off-track counter is reset after 0.75 extend or at the original track in the 2.25 track extend mode.

### 7.14.8 HIGH-LEVEL FEATURES

#### 7.14.8.1 Interrupt mechanism and STATUS pin

The STATUS pin is an output which is active LOW, its output is selected by decoder register 7 to be either the decoder status bit (active LOW) selected by decoder register 2 (only available in 4-wire bus mode) or the interrupt signal generated by the servo part.

Eight signals from the interrupt status register are selectable from the servo part via the `interrupt_mask` parameter. The interrupt is reset by sending the read high-level status command. The 8 signals are as follows:

- Focus lost: dropout of longer than 3 ms
- Subcode ready
- Subcode absolute seconds changed
- Subcode discontinuity detected: new subcode time before previous subcode time, or more than 10 frames later than previous subcode time
- Radial error: during radial on-track, no new subcode frame occurs within time defined by the 'playwatchtime' parameter; during radial jump, less than 4 tracks have been crossed during time defined by the 'jumpwatchtime' parameter
- Autosequencer state change
- Autosequencer error
- Subcode interface blocked: the internal decoder interface is being used.

It should be noted that if the STATUS pin output is selected via decoder register 2 and either the microcontroller writes a different value to decoder register 2 or the decoder interface is enabled then the STATUS output will change.

#### 7.14.8.2 Decoder interface

The decoder interface allows decoder registers 0 to F to be programmed and subcode Q-channel data to be read via servo commands. The interface is enabled/disabled by the preset latch command (and the `xtra_preset` parameter).

#### 7.14.8.3 Automatic error handling

Three Watchdogs are present:

- Focus: detects focus dropout of longer than 3 ms, sets focus lost interrupt, switches off radial and sledge servos, disables drive to disc motor
- Radial play: started when radial servo is in on-track mode and a first subcode frame is found; detects when maximum time between two subcode frames exceeds the time set by `playwatchtime` parameter; then sets radial error interrupt, switches radial and sledge servos off, puts disc motor in jump mode
- Radial jump: active when radial servo is in long jump or short jump modes; detects when the off-track counter value decreases by less than 4 tracks between two readings (time interval set by `jumpwatchtime` parameter); then sets radial jump error, switches radial and sledge servos off to cancel jump.

The focus Watchdog is always active, the radial Watchdogs are selectable via the `radcontrol` parameter.

#### 7.14.8.4 Automatic sequencers and timer interrupts

Two automatic sequencers are implemented (and must be initialized after power-on):

- Autostart sequencer: controls the start-up of focus, radial and motor
- Autostop sequencer: brakes the disc and shuts down servos.

When the automatic sequencers are not used it is possible to generate timer interrupts, defined by the `time_parameter` coefficient.

#### 7.14.8.5 High-level status

The read high-level status command can be used to obtain the interrupt, decoder, autosequencer status registers and the motor start time. Use of the read high-level status command clears the interrupt status register, and re-enables the subcode read via a servo command.

### 7.14.9 DRIVER INTERFACE

The control signals (pins RA, FO and SL) for the mechanism actuators are pulse density modulated. The modulating frequency can be set to either 1.0584 (DSD mode) or 2.1168 MHz; controlled via the `xtra_preset` parameter. An analog representation of the output signals can be achieved by connecting a 1st-order low-pass filter to the outputs.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

During reset (i.e. RESET pin is held LOW) the RA, FO and SL pins are high-impedance.

### 7.14.10 LASER INTERFACE

The LDON pin (open-drain output) is used to switch the laser off and on. When the laser is on, the output is high-impedance. The action of the LDON pin is controlled by the xtra\_preset parameter; the pin is automatically driven if the focus control loop is active.

### 7.14.11 RADIAL SHOCK DETECTOR

The shock detector (see Fig.22) can be switched on during normal track following, and detects within an adjustable frequency whether disturbances in the radial spot position relative to the track exceed an adjustable level (controlled by shock\_level).

Every time the radial tracking error exceeds this level the radial control bandwidth is switched to twice its original bandwidth and the loop gain is increased by a factor of 4.

The shock detection level is adjustable in 16 steps from 0% to 100% of the traverse radial amplitude which is sent to an amplitude detection unit via an adjustable band-pass filter (controlled by sledge\_parm1); lower corner frequency can be set at either 0 or 20 Hz, and upper corner frequency at 750 or 1850 Hz. The shock detector is switched off automatically during jump mode.

### 7.15 Microcontroller interface

Communication on the microcontroller interface can be set-up in two different modes:

- 4-wire bus mode: protocol compatible with SAA7345 (CD6) and TDA1301 (DSIC2) where:
  - SCL = serial clock
  - SDA = serial data
  - RAB =  $R/\bar{W}$  control and data strobe (active HIGH) for writing to decoder registers 0 to F, reading status bit selected via decoder register 2 and reading Q-channel subcode
  - SILD =  $\bar{R}/W$  control and data strobe (active LOW) for servo commands.
- I<sup>2</sup>C-bus mode: I<sup>2</sup>C-bus protocol where the SAA7324 behaves as slave device, activated by setting RAB = HIGH and SILD = LOW where:
  - I<sup>2</sup>C-bus slave address (write mode) = 30H
  - I<sup>2</sup>C-bus slave address (read mode) = 31H
  - Maximum data transfer rate = 400 kbits/s.

It should be noted that only servo commands can be used therefore, writing to decoder registers 0 to F, reading decoder status and reading Q-channel subcode data must be performed by servo commands.

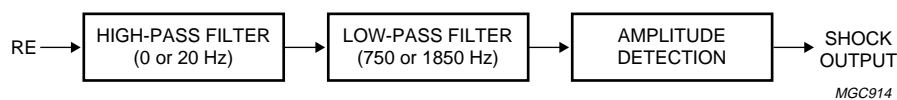


Fig.22 Block diagram of radial shock detector.



## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.15.1 MICROCONTROLLER INTERFACE (4-WIRE BUS MODE)

#### 7.15.1.1 Writing data to registers 0 to F

The sixteen 4-bit programmable configuration registers, 0 to F (see Table 14), can be written to via the microcontroller interface using the protocol shown in Fig.23.

It should be noted that SILD must be held HIGH; A3 to A0 identifies the register number and D3 to D0 is the data. The data is latched into the register on the LOW-to-HIGH transition of RAB.

#### 7.15.1.2 Writing repeated data to registers 0 to F

The same data can be repeated several times (e.g. for a fade function) by applying extra RAB pulses as shown in Fig.24. It should be noted that SCL must stay HIGH between RAB pulses.

#### 7.15.1.3 Reading decoder status information on SDA

There are several internal status signals, selected via register 2, which can be made available on the SDA line:

SUBQREADY-I: LOW if new subcode word is ready in Q-channel register

MOTSTART1: HIGH if motor is turning at 75% or more of nominal speed

MOTSTART2: HIGH if motor is turning at 50% or more of nominal speed

MOTSTOP: HIGH if motor is turning at 12% or less of nominal speed; can be set to indicate 6% or less (instead of 12% or less) via register E

PLL lock: HIGH if sync coincidence signals are found

V1: follows input on pin V1

V2: follows input on pin V2

MOTOR-OV: HIGH if the motor servo output stage saturates

FIFO-OV: HIGH if FIFO overflows

SHOCK:  $\overline{\text{MOTSTART2}} + \overline{\text{PLL Lock}} + \overline{\text{MOTOR-OV}} + \overline{\text{FIFO-OV}} + \text{servo interrupt signal} + \text{OTD}$  (HIGH if shock detected)

LA-SHOCK: latched SHOCK signal.

The status read protocol is shown in Fig.25. It should be noted that SILD must be held HIGH.

#### 7.15.1.4 Reading Q-channel subcode

To read the Q-channel subcode direct in the 4-wire bus mode, the SUBQREADY-I signal should be selected as status signal. The subcode read protocol is illustrated in Fig.26.

It should be noted that SILD must be held HIGH; after subcode read starts, the microcontroller may take as long as it wants to terminate the read operation. When enough subcode has been read (1 to 96 bits), terminate reading by pulling RAB LOW.

Alternatively, the Q-channel subcode can be read using a servo command as follows:

- Use the read high-level status command to monitor the subcode ready signal
- Send the read subcode command and read the required number of bytes (up to 12)
- Send the read high-level status command; to re-enable the decoder interface.

#### 7.15.1.5 Behaviour of the SUBQREADY-I signal

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I status signal will react as shown in Fig.27. When the CRC is good and the subcode is being read, the timing in Fig.28 applies.

If  $t_1$  (SUBQREADY-I status LOW to end of subcode read) is below  $2.6/n$  ms, then  $t_2 = 13.1/n$  ms (i.e. the microcontroller can read all subcode frames if it completes the read operation within  $2.6/n$  ms after the subcode is ready). If these criteria are not met, it is only possible to guarantee that  $t_3$  will be below  $26.2/n$  ms (approximately).

If subcode frames with failed CRCs are present, the  $t_2$  and  $t_3$  times will be increased by  $13.1/n$  ms for each defective subcode frame.

It should be noted that in the lock-to-disc mode 'n' is replaced by 'd', which is the disc speed factor.

#### 7.15.1.6 Write servo commands

A write data command is used to transfer data (a number of bytes) from the microcontroller, using the protocol shown in Fig.29. The first of these bytes is the command byte and the following are data bytes; the number (between 1 and 7) depends on the command byte.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

## SAA7324

It should be noted that RAB must be held LOW; the command or data is interpreted by the SAA7324 after the HIGH-to-LOW transition of SILD; there must be a minimum time of 70  $\mu$ s between SILD pulses.

### 7.15.1.7 Writing repeated data in servo commands

The same data byte can be repeated by applying extra SILD pulses as illustrated in Fig.30. SCL must be HIGH between the SILD pulses.

### 7.15.1.8 Read servo commands

A read data command is used to transfer data (status information) to the microcontroller, using the protocol shown in Fig.31. The first byte written determines the type of command. After this byte a variable number of bytes can be read. It should be noted that RAB must be held LOW; after the end of the command byte (LOW-to-HIGH transition on SILD) there must be a delay of 70  $\mu$ s before reading data is started (i.e. the next HIGH-to-LOW transition on SILD); there must be a minimum time of 70  $\mu$ s between SILD pulses.

### 7.15.2 MICROCONTROLLER INTERFACE (I<sup>2</sup>C-BUS MODE)

Bytes are transferred over the interface in groups (i.e. servo commands) of which there are two types: write data commands and read data commands.

The sequence for a write data command (that requires 3 data bytes) is as follows:

1. Send START condition
2. Send address 30H (write)
3. Write command byte
4. Write data byte 1
5. Write data byte 2
6. Write data byte 3
7. Send STOP condition.

It should be noted that more than one command can be sent in one write sequence.

The sequence for a read data command (that reads 2 data bytes) is as follows:

1. Send START condition
2. Send address 30H (write)
3. Write command byte
4. Send STOP condition
5. Send START condition
6. Send address 31H (read)
7. Read data byte 1
8. Read data byte 2
9. Send STOP condition.

It should be noted that the timing constraints specified for the read and write servo commands must still be adhered to.

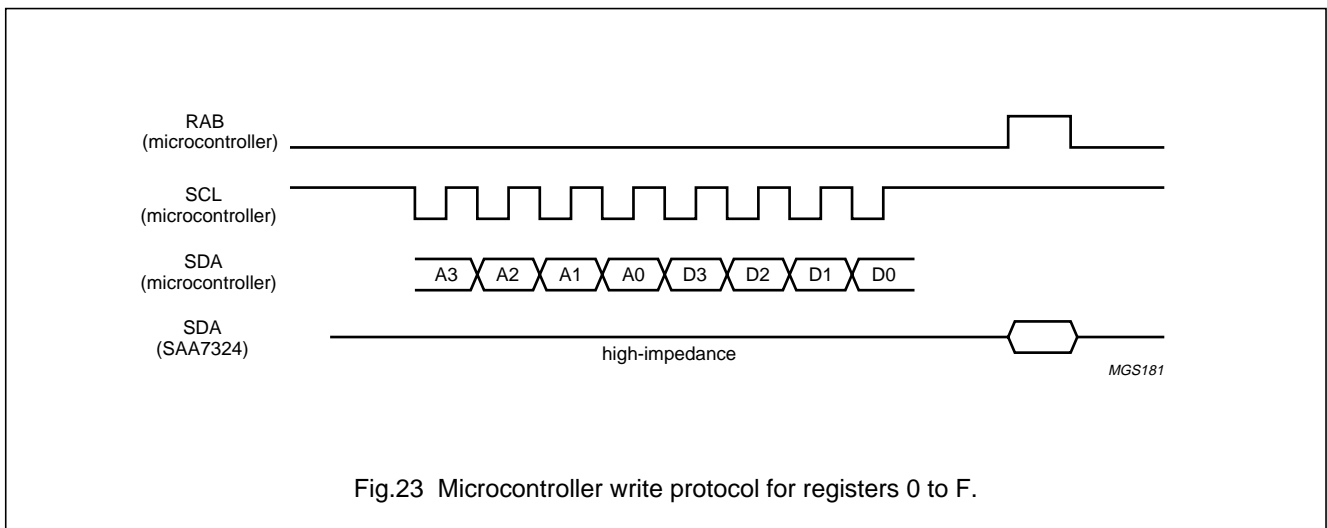


Fig.23 Microcontroller write protocol for registers 0 to F.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

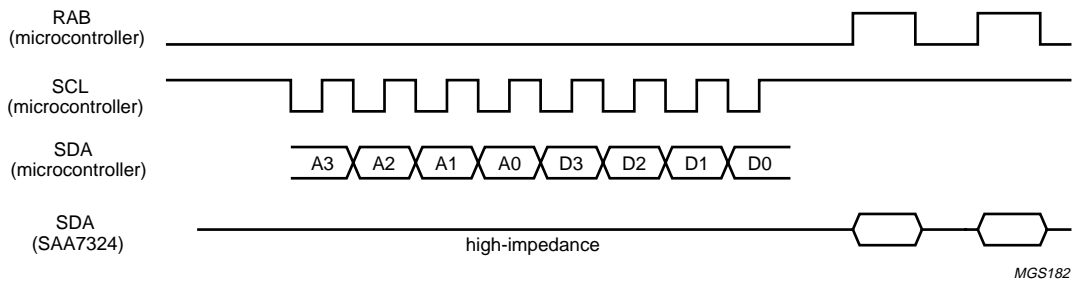


Fig.24 Microcontroller write protocol for registers 0 to F (repeat mode).

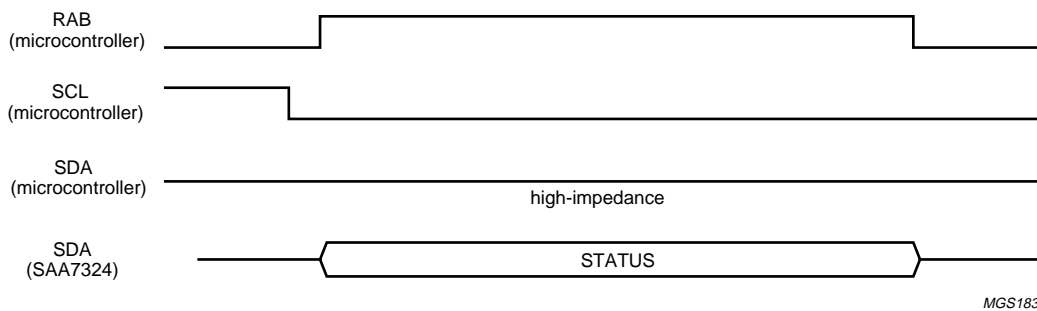


Fig.25 Microcontroller read protocol for decoder status on SDA.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

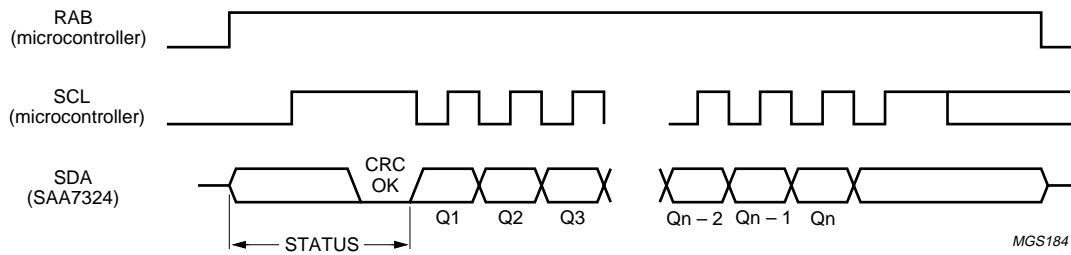


Fig.26 Microcontroller protocol for reading Q-channel subcode.

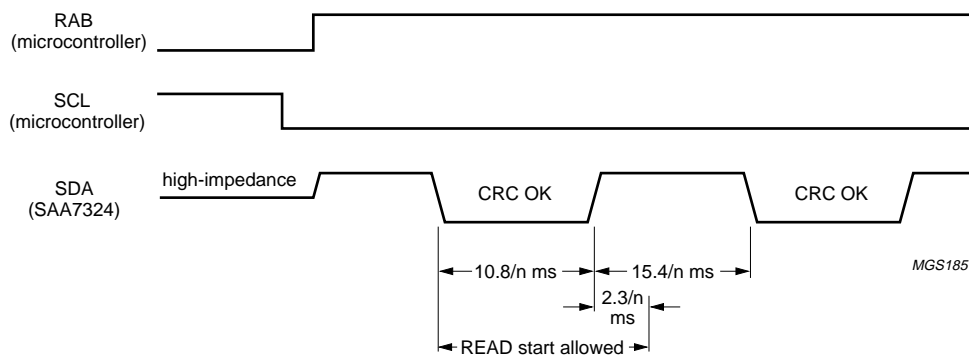


Fig.27 SUBQREADY-I status timing when no subcode is read.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

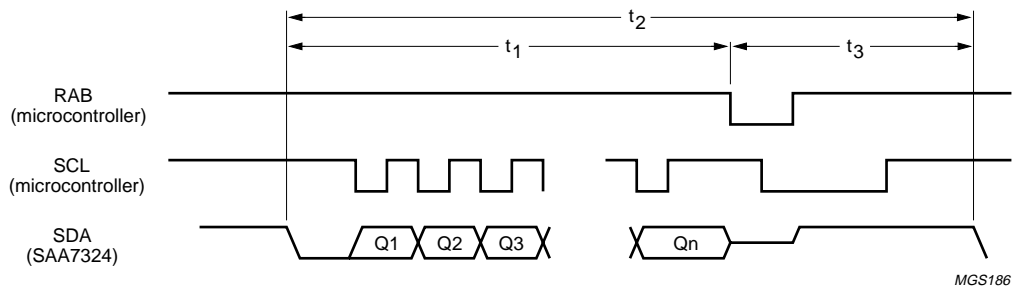


Fig.28 SUBQREADY-I status timing when subcode is read.

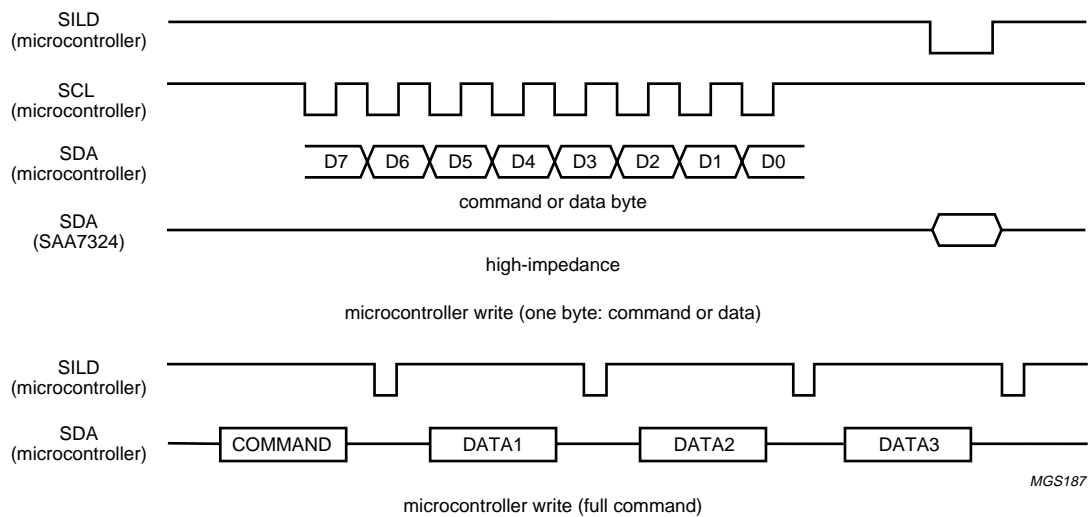


Fig.29 Microcontroller protocol for write servo commands.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

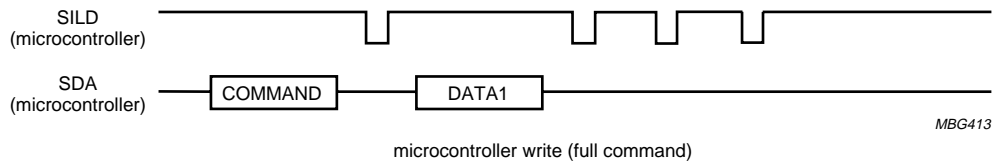


Fig.30 Microcontroller protocol for repeated data in write servo commands.

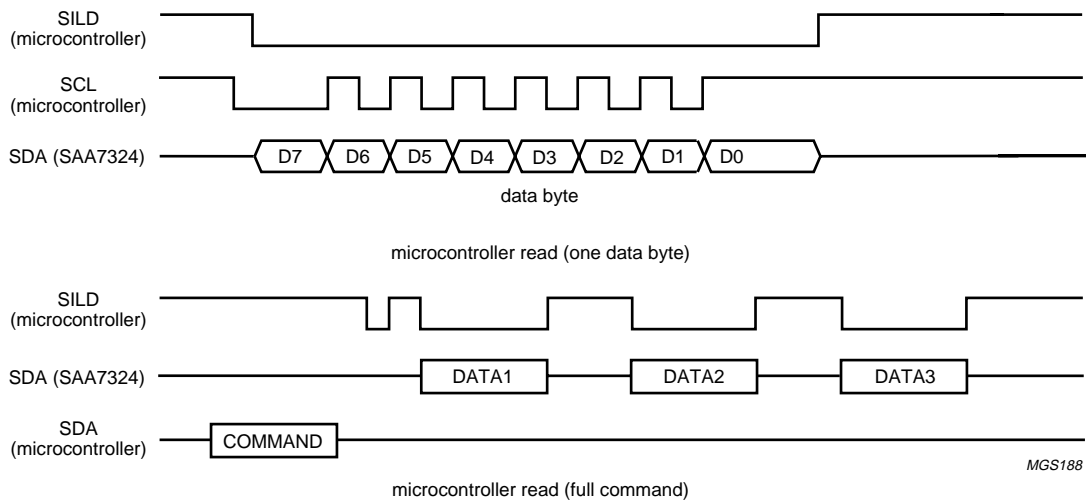


Fig.31 Microcontroller protocol for read servo commands.

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.15.3 DECODER REGISTERS AND SHADOW REGISTERS

To maintain compatibility with the SAA737x series, decoder registers 0 to F are identical to the SAA7370. However, to control the extra functionality of SAA7324, a new set of registers called shadow registers have been implemented.

These are accessed by using the LSB of decoder register F. This bit is called SHADEN (shadow registers enable) on SAA7324. When this bit is set to logic 1 (i.e. decoder register F set to XXX1), any subsequent addresses will be decoded by the shadow registers. In fact, only four addresses are implemented as shadow registers; 3, 7, A and C. Any other addresses sent while SHADEN = 1 are invalid and have no effect.

When SHADEN is set to logic 0 (decoder register F set to XXX0) all subsequent addresses are decoded by the main decoder registers again.

Access to decoder register F is always enabled so that SHADEN can be set or reset as required.

The SHADEN bit and subsequent shadow registers are programmed identically to the main decoder registers, i.e. they can be directly programmed when using the SAA7324 in 4-wire mode or programmed via the servo interface when using 3-wire or I<sup>2</sup>C-bus modes.

The main decoder registers are given in Table 14. The functions implemented using shadow registers are given in Table 16.

### 7.15.4 SUMMARY OF FUNCTIONS CONTROLLED BY DECODER REGISTERS 0 TO F

**Table 14** Registers 0 to F

| REGISTER                    | ADDRESS | DATA  | FUNCTION           | INITIAL <sup>(1)</sup> |
|-----------------------------|---------|-------|--------------------|------------------------|
| 0<br>(fade and attenuation) | 0000    | 0000  | mute               | reset                  |
|                             |         | 0010  | attenuate          | –                      |
|                             |         | 0001  | full-scale         | –                      |
|                             |         | 0100  | step down          | –                      |
|                             |         | 0101  | step up            | –                      |
| 1<br>(motor mode)           | 0001    | X000  | motor off mode     | reset                  |
|                             |         | X 001 | motor stop mode 1  | –                      |
|                             |         | X010  | motor stop mode 2  | –                      |
|                             |         | X011  | motor start mode 1 | –                      |
|                             |         | X100  | motor start mode 2 | –                      |
|                             |         | X101  | motor jump mode    | –                      |
|                             |         | X111  | motor play mode    | –                      |
|                             |         | X110  | motor jump mode 1  | –                      |
|                             |         | 1XXX  | anti-windup active | –                      |
|                             |         | 0XXX  | anti-windup off    | reset                  |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| REGISTER   | ADDRESS | DATA | FUNCTION   | INITIAL <sup>(1)</sup> |
|--|---------|------|--|------------------------|
| 2<br>(status control to servo part - not the STATUS pin) | 0010    | 0000 | status = SUBQREADY-I                                     | reset                  |
|  |         | 0001 | status = MOTSTART1                                       | –                      |
|  |         | 0010 | status = MOTSTART2                                       | –                      |
|  |         | 0011 | status = MOTSTOP   | –                      |
|  |         | 0100 | status = PLL lock  | –                      |
|  |         | 0101 | status = V1  | –                      |
|  |         | 0110 | status = V2  | –                      |
|  |         | 0111 | status = MOTOR-OV  | –                      |
|  |         | 1000 | status = FIFO overflow                                   | –                      |
|  |         | 1001 | status = shock detect                                    | –                      |
|  |         | 1010 | status = latched shock detect                            | –                      |
|  |         | 1011 | status = latched shock detect reset                      | –                      |
| 3<br>(DAC output)  | 0011    | 1010 | I <sup>2</sup> S-bus; CD-ROM mode                        | –                      |
|  |         | 1011 | EIAJ; CD-ROM mode  | –                      |
|  |         | 1100 | I <sup>2</sup> S-bus; 18-bit; 4f <sub>s</sub> mode       | reset                  |
|  |         | 1111 | I <sup>2</sup> S-bus; 18-bit; 2f <sub>s</sub> mode       | –                      |
|  |         | 1110 | I <sup>2</sup> S-bus; 16-bit; f <sub>s</sub> mode        | –                      |
|  |         | 0000 | EIAJ; 16-bit; 4f <sub>s</sub>                            | –                      |
|  |         | 0011 | EIAJ; 16-bit; 2f <sub>s</sub>                            | –                      |
|  |         | 0010 | EIAJ; 16-bit; f <sub>s</sub>                             | –                      |
|  |         | 0100 | EIAJ; 18-bit; 4f <sub>s</sub>                            | –                      |
|  |         | 0111 | EIAJ; 18-bit; 2f <sub>s</sub>                            | –                      |
|  |         | 0110 | EIAJ; 18-bit; f <sub>s</sub>                             | –                      |
| 4<br>(motor gain)  | 0100    | X000 | motor gain G = 3.2                                       | reset                  |
|  |         | X001 | motor gain G = 4.0                                       | –                      |
|  |         | X010 | motor gain G = 6.4                                       | –                      |
|  |         | X011 | motor gain G = 8.0                                       | –                      |
|  |         | X100 | motor gain G = 12.8                                      | –                      |
|  |         | X101 | motor gain G = 16.0                                      | –                      |
|  |         | X110 | motor gain G = 25.6                                      | –                      |
|  |         | X111 | motor gain G = 32.0                                      | –                      |
|  |         | 0XXX | disable comparator clock divider                         | reset                  |
|  |         | 1XXX | enable comparator clock divider; only if SELPLL set HIGH | –                      |
| 5<br>(motor bandwidth)                                   | 0101    | XX00 | motor f <sub>4</sub> = 0.5 × n Hz                        | reset                  |
|  |         | XX01 | motor f <sub>4</sub> = 0.7 × n Hz                        | –                      |
|  |         | XX10 | motor f <sub>4</sub> = 1.4 × n Hz                        | –                      |
|  |         | XX11 | motor f <sub>4</sub> = 2.8 × n Hz                        | –                      |
|  |         | 00XX | motor f <sub>3</sub> = 0.85 × n Hz                       | reset                  |
|  |         | 01XX | motor f <sub>3</sub> = 1.71 × n Hz                       | –                      |
|  |         | 10XX | motor f <sub>3</sub> = 3.42 × n Hz                       | –                      |



# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| REGISTER                             | ADDRESS | DATA | FUNCTION   | INITIAL <sup>(1)</sup> |
|--------------------------------------|---------|------|--|------------------------|
| 6<br>(motor output configuration)    | 0110    | XX00 | motor power maximum 37%  | reset                  |
|                                      |         | XX01 | motor power maximum 50%  | –                      |
|                                      |         | XX10 | motor power maximum 75%  | –                      |
|                                      |         | XX11 | motor power maximum 100%   | –                      |
|                                      |         | 00XX | MOTO1, MOTO2 pins 3-state  | reset                  |
|                                      |         | 01XX | motor PWM mode   | –                      |
|                                      |         | 10XX | motor PDM mode   | –                      |
|                                      |         | 11XX | motor CDV mode   | –                      |
| 7<br>(DAC output and status control) | 0111    | XX00 | interrupt signal from servo at STATUS pin  | reset                  |
|                                      |         | XX10 | status bit from decoder status register at STATUS pin                                    | –                      |
|                                      |         | X0XX | DAC data normal value  | reset                  |
|                                      |         | X1XX | DAC data inverted value  | –                      |
|                                      |         | 0XXX | left channel first at DAC (WCLK normal)  | reset                  |
|                                      |         | 1XXX | right channel first at DAC (WCLK inverted)   | –                      |
| 8<br>(PLL loop filter bandwidth)     |         |      | see Table 15   | –                      |
| 9<br>(PLL equalization)              | 1001    | 0011 | PLL loop filter equalization   | reset                  |
|                                      |         | 0001 | PLL 30 ns over-equalization  | –                      |
|                                      |         | 0010 | PLL 15 ns over-equalization  | –                      |
|                                      |         | 0100 | PLL 15 ns under-equalization   | –                      |
|                                      |         | 0101 | PLL 30 ns under-equalization   | –                      |
| A<br>(EBU output)                    | 1010    | XX0X | EBU data before concealment  | –                      |
|                                      |         | XX1X | EBU data after concealment and fade  | reset                  |
|                                      |         | X0X0 | level II clock accuracy (<1000 ppm)  | reset                  |
|                                      |         | X0X1 | level I clock accuracy (<50 ppm)   | –                      |
|                                      |         | X1X0 | level III clock accuracy (>1000 ppm)   | –                      |
|                                      |         | X1X1 | EBU off - output low   | –                      |
|                                      |         | 0XXX | flags in EBU off   | reset                  |
|                                      |         | 1XXX | flags in EBU on  | –                      |
| B<br>(speed control)                 | 1011    | X0XX | 33.8688 MHz crystal present, or 8.4672 MHz (or 16.9344 MHz) crystal with SELPLL set HIGH | reset                  |
|                                      |         | X1XX | 16.9344 MHz crystal present  | –                      |
|                                      |         | 0XXX | single-speed mode  | reset                  |
|                                      |         | 1XXX | double-speed mode  | –                      |
|                                      |         | XX00 | standby 1: 'CD-STOP' mode  | reset                  |
|                                      |         | XX10 | standby 2: 'CD-PAUSE' mode   | –                      |
|                                      |         | XX11 | operating mode   | –                      |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| REGISTER  | ADDRESS | DATA | FUNCTION  | INITIAL <sup>(1)</sup> |
|---|---------|------|---|------------------------|
| C<br>(versatile pins interface)                     | 1100    | XXX1 | external off-track signal input at V1   | –                      |
|   |         | XXX0 | internal off-track signal used (V1 may be read via status)  | reset                  |
|   |         | XX0X | kill-L at KILL output, kill-R at V3 output  | –                      |
|   |         | 001X | V3 = 0; single KILL output  | reset                  |
|   |         | 011X | V3 = 1; single KILL output  | –                      |
| D<br>(versatile pins interface)                     | 1101    | 0000 | 4-line motor (using V4 and V5)  | –                      |
|   |         | XX01 | Q-to-W subcode at V4  | –                      |
|   |         | XX10 | V4 = 0  | –                      |
|   |         | XX11 | V4 = 1  | reset                  |
|   |         | 01XX | de-emphasis signal at V5, no internal de-emphasis filter  | –                      |
|   |         | 10XX | V5 = 0  | –                      |
|   |         | 11XX | V5 = 1  | reset                  |
| E   | 1110    | 00XX | audio features disabled   | –                      |
|   |         | 01XX | audio features enabled  | reset                  |
|   |         | XX0X | lock-to-disc mode disabled  | reset                  |
|   |         | XX1X | lock-to-disc mode enabled   | –                      |
|   |         | XXX0 | motor brakes to 12%   | reset                  |
|   |         | XXX1 | motor brakes to 6%  | –                      |
| F<br>(subcode interface and shadow register enable) | 1111    | X0XX | subcode interface off   | reset                  |
|   |         | X1XX | subcode interface on  | –                      |
|   |         | 0XXX | 4-wire subcode  | reset                  |
|   |         | 1XXX | 3-wire subcode  | –                      |
|   |         | XXX0 | SHADEN = 0; shadow registers not enabled; addresses will be decoded by main decoder registers                             | reset                  |
|   |         | XXX1 | SHADEN = 1; shadow registers enabled; all subsequent addresses will be decoded by shadow registers, not decoder registers | –                      |

**Note**

1. The initial column shows the Power-on reset state.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

Table 15 Loop filter bandwidth

| REGISTER                         | ADDRESS | DATA | FUNCTION            |                         |                         | INITIAL <sup>(1)</sup> |
|----------------------------------|---------|------|---------------------|-------------------------|-------------------------|------------------------|
|                                  |         |      | LOOP BANDWIDTH (HZ) | INTERNAL BANDWIDTH (HZ) | LOW-PASS BANDWIDTH (HZ) |                        |
| 8<br>(PLL loop filter bandwidth) | 1000    | 0000 | 1640 × n            | 525 × n                 | 8400 × n                | –                      |
|                                  |         | 0001 | 3279 × n            | 263 × n                 | 16800 × n               | –                      |
|                                  |         | 0010 | 6560 × n            | 131 × n                 | 33600 × n               | –                      |
|                                  |         | 0100 | 1640 × n            | 1050 × n                | 8400 × n                | –                      |
|                                  |         | 0101 | 3279 × n            | 525 × n                 | 16800 × n               | –                      |
|                                  |         | 0110 | 6560 × n            | 263 × n                 | 33600 × n               | –                      |
|                                  |         | 1000 | 1640 × n            | 2101 × n                | 8400 × n                | –                      |
|                                  |         | 1001 | 3279 × n            | 1050 × n                | 16800 × n               | reset                  |
|                                  |         | 1010 | 6560 × n            | 525 × n                 | 33600 × n               | –                      |
|                                  |         | 1100 | 1640 × n            | 4200 × n                | 8400 × n                | –                      |
|                                  |         | 1101 | 3279 × n            | 2101 × n                | 16800 × n               | –                      |
|                                  |         | 1110 | 6560 × n            | 1050 × n                | 33600 × n               | –                      |

Note

1. The initial column shows the Power-on reset state.

7.15.5 SUMMARY OF FUNCTIONS CONTROLLED BY SHADOW REGISTERS

Table 16 Shadow register settings

| SHADEN BIT | SHADOW REGISTER                          | ADDRESS | DATA | FUNCTION                                       | INITIAL |
|------------|--|---------|------|--|---------|
| 1          | 3<br>control of versatile and clock pins | 0011    | XXX0 | select CL4 on CL11/4 output                    | reset   |
|            |  |         | XXX1 | select CL11 on CL11/4 output                   | –       |
|            |  |         | XX0X | enable CL11/4 output pin                       | reset   |
|            |  |         | XX1X | set CL11/4 output pin to high-impedance        | –       |
|            |  |         | X0XX | enable CL16 output pin                         | reset   |
|            |  |         | X1XX | set CL16 output pin to high-impedance          | –       |
|            |  |         | 0XXX | V2/V3 pin configured as V2 input               | reset   |
|            |  |         | 1XXX | V2/V3 pin configured as V3 output (open-drain) | –       |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SHADEN BIT | SHADOW REGISTER   | ADDRESS                                       | DATA | FUNCTION  | INITIAL                                     |   |
|------------|---|---|------|---|---|---|
| 1          | 7<br>control of<br>onboard DAC                                | 0111  | XXX0 | hold onboard DAC outputs at zero                                      | reset                                       |   |
|            |   |   | XXX1 | enable onboard DAC outputs  | –   |   |
|            |   |   | XX0X | use external DAC or route audio data into onboard DAC (loopback mode) | reset                                       |   |
|            |   |   | XX1X | route audio data into onboard DAC (non-loopback mode)                 | –   |   |
|            |   |   | X1XX | use internal reference for servo reference voltage                    | reset                                       |   |
|            |   |   | X0XX | use external reference for servo reference voltage                    | –   |   |
|            | A<br>signal<br>magnitude<br>control for<br>diodes<br>D1 to D4 | 7<br>servo<br>reference<br>pin = 7, $V_{RIN}$ | 1010 | 0000  | (0.042). $I_{ref} = 1.006 \mu A$ (nominal)  | – |
|            |   |   |      | 0001  | (0.083). $I_{ref} = 2.013 \mu A$ (nominal)  | – |
|            |   |   |      | 0010  | (0.125). $I_{ref} = 3.019 \mu A$ (nominal)  | – |
|            |   |   |      | 0011  | (0.167). $I_{ref} = 4.025 \mu A$ (nominal)  | – |
|            |   |   |      | 0100  | (0.208). $I_{ref} = 5.031 \mu A$ (nominal)  | – |
|            |   |   |      | 0101  | (0.25). $I_{ref} = 6.034 \mu A$ (nominal)   | – |
|            |   |   |      | 0110  | (0.292). $I_{ref} = 7.044 \mu A$ (nominal)  | – |
|            |   |   |      | 0111  | (0.333). $I_{ref} = 8.05 \mu A$ (nominal)   | – |
|            |   |   |      | 1000  | (0.375). $I_{ref} = 9.056 \mu A$ (nominal)  | – |
|            |   |   |      | 1001  | (0.417). $I_{ref} = 10.063 \mu A$ (nominal) | – |
|            |   |   |      | 1010  | (0.458). $I_{ref} = 11.069 \mu A$ (nominal) | – |
|            |   |   |      | 1011  | (0.5). $I_{ref} = 12.075 \mu A$ (nominal)   | – |
|            |   |   |      | 1100  | (0.542). $I_{ref} = 13.081 \mu A$ (nominal) | – |
| 1101       | (0.583). $I_{ref} = 14.088 \mu A$ (nominal)                   | –   |      |   |   |   |
| 1110       | (0.625). $I_{ref} = 15.094 \mu A$ (nominal)                   | –   |      |   |   |   |
| 1111       | (0.667). $I_{ref} = 16.1 \mu A$ (nominal)                     | reset   |      |   |   |   |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SHADEN BIT | SHADOW REGISTER  | ADDRESS | DATA | FUNCTION                                       | INITIAL |
|------------|--|---------|------|--|---------|
| 1          | C<br>signal<br>magnitude<br>control for<br>diodes<br>R1 and R2 | 1100    | 0000 | (0.042).I <sub>ref</sub> = 1.006 μA (nominal)  | –       |
|            |  |         | 0001 | (0.083).I <sub>ref</sub> = 2.013 μA (nominal)  | –       |
|            |  |         | 0010 | (0.125).I <sub>ref</sub> = 3.019 μA (nominal)  | –       |
|            |  |         | 0011 | (0.167).I <sub>ref</sub> = 4.025 μA (nominal)  | –       |
|            |  |         | 0100 | (0.208).I <sub>ref</sub> = 5.031 μA (nominal)  | –       |
|            |  |         | 0101 | (0.25).I <sub>ref</sub> = 6.034 μA (nominal)   | –       |
|            |  |         | 0110 | (0.292).I <sub>ref</sub> = 7.044 μA (nominal)  | –       |
|            |  |         | 0111 | (0.333).I <sub>ref</sub> = 8.05 μA (nominal)   | –       |
|            |  |         | 1000 | (0.375).I <sub>ref</sub> = 9.056 μA (nominal)  | –       |
|            |  |         | 1001 | (0.417).I <sub>ref</sub> = 10.063 μA (nominal) | –       |
|            |  |         | 1010 | (0.458).I <sub>ref</sub> = 11.069 μA (nominal) | –       |
|            |  |         | 1011 | (0.5).I <sub>ref</sub> = 12.075 μA (nominal)   | –       |
|            |  |         | 1100 | (0.542).I <sub>ref</sub> = 13.081 μA (nominal) | –       |
|            |  |         | 1101 | (0.583).I <sub>ref</sub> = 14.088 μA (nominal) | –       |
| 1110       | (0.625).I <sub>ref</sub> = 15.094 μA (nominal)                 | –       |      |  |         |
| 1111       | (0.667).I <sub>ref</sub> = 16.1 μA (nominal)                   | reset   |      |  |         |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 7.15.6 SUMMARY OF SERVO COMMANDS

A list of the servo commands are given in Table 17. These are fully compatible with the SAA7370.

**Table 17** SAA7324 servo commands

| COMMANDS                           | CODE | BYTES    | PARAMETERS   |
|------------------------------------|------|----------|--|
| <b>Write commands</b>              |      |          |  |
| Write_focus_coefs1                 | 17H  | 7        | <foc_parm3> <foc_int> <ramp_incr> <ramp_height><br><ramp_offset> <FE_start> <foc_gain>                       |
| Write_focus_coefs2                 | 27H  | 7        | <defect_parm> <rad_parm_jump> <vel_parm2><br><vel_parm1> <foc_parm1> <foc_parm2> <CA_drop>                   |
| Write_focus_command                | 33H  | 3        | <foc_mask> <foc_stat> <shock_level>  |
| Focus_gain_up                      | 42H  | 2        | <foc_gain> <foc_parm1>   |
| Focus_gain_down                    | 62H  | 2        | <foc_gain> <foc_parm1>   |
| Write_radial_coefs                 | 57H  | 7        | <rad_length_lead> <rad_int> <rad_parm_play><br><rad_pole_noise> <rad_gain> <sledge_parm2><br><sledge_parm_1> |
| Preset_Latch                       | 81H  | 1        | <chip_init>  |
| Radial_off                         | C1H  | 1        | '1CH'  |
| Radial_init                        | C1H  | 1        | '3CH'  |
| Short_jump                         | C3H  | 3        | <tracks_hi> <tracks_lo> <rad_stat>   |
| Long_jump                          | C5H  | 5        | <brake_dist> <sledge_U_max> <tracks_hi> <tracks_lo><br><rad_stat>  |
| Steer_sledge                       | B1H  | 1        | <sledge_level>   |
| Preset_init                        | 93H  | 3        | <re_offset> <re_gain> <sum_gain>   |
| Write_decoder_reg <sup>(1)</sup>   | D1H  | 1        | <decoder_reg_data>   |
| Write_parameter                    | A2H  | 2        | <param_ram_addr> <param_data>  |
| <b>Read commands</b>               |      |          |  |
| Read_Q_subcode <sup>(1)(2)</sup>   | 0H   | up to 12 | <Q_sub1 to 10> <peak_l> <peak_r>   |
| Read_status                        | 70H  | up to 5  | <foc_stat> <rad_stat> <rad_int_lpf> <tracks_hi><br><tracks_lo>   |
| Read_hilevel_status <sup>(3)</sup> | E0H  | up to 4  | <intreq> <dec_stat> <seq_stat> <motor_start_time>  |
| Read_aux_status                    | F0H  | up to 3  | <re_offset> <re_gain> <sum_gain>   |

#### Notes

1. These commands only available when internal decoder interface is enabled.
2. <peak\_l> and <peak\_r> bytes are clocked out LSB first.
3. Decoder status flag information in <dec\_stat> is only valid when the internal decoder interface is enabled.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 7.15.7 SUMMARY OF SERVO COMMAND PARAMETERS

**Table 18** Servo command parameters

| PARAMETER         | RAM ADDRESS | AFFECTS         | POR VALUE | DETERMINES  |
|-------------------|-------------|-----------------|-----------|---|
| foc_parm_1        | –           | focus PID       | –         | end of focus lead<br>defect detector enabling                       |
| foc_parm_2        | –           | focus PID       | –         | focus low-pass<br>focus error normalising                           |
| foc_parm_3        | –           | focus PID       | –         | focus lead length<br>minimum light level                            |
| foc_int           | 14H         | focus PID       | –         | focus integrator crossover frequency                                |
| foc_gain          | 15H         | focus PID       | 70H       | focus PID loop gain   |
| CA_drop           | 12H         | focus PID       | –         | sensitivity of dropout detector                                     |
| ramp_offset       | 16H         | focus ramp      | –         | asymmetry of focus ramp   |
| ramp_height       | 18H         | focus ramp      | –         | peak-to-peak value of ramp voltage                                  |
| ramp_incr         | –           | focus ramp      | –         | slope of ramp voltage   |
| FE_start          | 19H         | focus ramp      | –         | minimum value of focus error  |
| rad_parm_play     | 28H         | radial PID      | –         | end of radial lead  |
| rad_pole_noise    | 29H         | radial PID      | –         | radial low-pass   |
| rad_length_lead   | 1CH         | radial PID      | –         | length of radial lead   |
| rad_int           | 1EH         | radial PID      | –         | radial integrator crossover frequency                               |
| rad_gain          | 2AH         | radial PID      | 70H       | radial loop gain  |
| rad_parm_jump     | 27H         | radial jump     | –         | filter during jump  |
| vel_parm1         | 1FH         | radial jump     | –         | PI controller crossover frequencies                                 |
| vel_parm2         | 32H         | radial jump     | –         | jump pre-defined profile  |
| speed_threshold   | 48H         | radial jump     | –         | maximum speed in fastrad mode                                       |
| hold_mult         | 49H         | radial jump     | 00H       | electronic damping<br>sledge bandwidth during jump                  |
| brake_dist_max    | 21H         | radial jump     | –         | maximum sledge distance allowed in fast actuator steered mode       |
| sledge_long_brake | 58H         | radial jump     | FFH       | brake distance of sledge  |
| sledge_Umax       | –           | sledge          | –         | voltage on sledge during long jump                                  |
| sledge_level      | –           | sledge          | –         | voltage on sledge when steered                                      |
| sledge_parm_1     | 36H         | sledge          | –         | sledge integrator crossover frequency                               |
| sledge_parm_2     | 17H         | sledge          | –         | sledge low-pass frequencies<br>sledge gain<br>sledge operation mode |
| sledge_pulse1     | 46H         | pulsed sledge   | –         | pulse width   |
| sledge_pulse2     | 64H         | pulsed sledge   | –         | pulse height  |
| defect_parm       | –           | defect detector | –         | defect detector setting   |
| shock_level       | –           | shock detector  | –         | shock detector operation  |
| playwatchtime     | 54H         | Watchdog        | –         | radial on-track Watchdog time                                       |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| PARAMETER         | RAM ADDRESS | AFFECTS           | POR VALUE | DETERMINES                                  |
|-------------------|-------------|-------------------|-----------|---|
| jumpwatchtime     | 57H         | Watchdog          | –         | radial jump Watchdog time-out               |
| radcontrol        | 59H         | Watchdog          | –         | enable/disable automatic radial off feature |
| chip_init         | –           | set-up            | –         | enable/disable decoder interface            |
| xtra_preset       | 4AH         | set-up            | 38H       | laser on/off                                |
|                   |             |                   |           | RA, FO and SL PDM modulating frequency      |
|                   |             |                   |           | fast jumping circuit on/off                 |
| cd6cmd            | 4DH         | decoder interface | –         | decoder part commands                       |
| interrupt_mask    | 53H         | STATUS pin        | –         | enabled interrupts                          |
| seq_control       | 42H         | autosequencer     | –         | autosequencer control                       |
| focus_start_time  | 5EH         | autosequencer     | –         | focus start time                            |
| motor_start_time1 | 5FH         | autosequencer     | –         | motor start 1 time                          |
| motor_start_time2 | 60H         | autosequencer     | –         | motor start 2 time                          |
| radial_init_time  | 61H         | autosequencer     | –         | radial initialization time                  |
| brake_time        | 62H         | autosequencer     | –         | brake time                                  |
| RadCmdByte        | 63H         | autosequencer     | –         | radial command byte                         |
| osc_inc           | 68H         | focus/radial AGC  | –         | AGC control                                 |
|                   |             |                   | –         | frequency of injected signal                |
| phase_shift       | 67H         | focus/radial AGC  | –         | phase shift of injected signal              |
| level1            | 69H         | focus/radial AGC  | –         | amplitude of signal injected                |
| level2            | 6AH         | focus/radial AGC  | –         | amplitude of signal injected                |
| agc_gain          | 6CH         | focus/radial AGC  | –         | focus/radial gain                           |



# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL         | PARAMETER  | CONDITIONS | MIN.         | MAX.                   | UNIT   |
|----------------|--|------------|--------------|------------------------|--------|
| $V_{DD}$       | supply voltage   | note 1     | -0.5         | +3.6                   | V      |
| $V_{I(max)}$   | maximum input voltage<br>any input<br>pins RESET, SDA, SCL, RAB and SILD |            | -0.5<br>-0.5 | $V_{DD} + 0.5$<br>+5.5 | V<br>V |
| $V_O$          | output voltage (any output)  |            | -0.5         | +3.6                   | V      |
| $V_{DD(diff)}$ | difference between $V_{DDA}$ , $V_{DDD}$ and $V_{pos}$                   |            | -            | $\pm 0.25$             | V      |
| $I_O$          | output current (continuous)  |            | -            | $\pm 20$               | mA     |
| $I_{I(d)}$     | DC input diode current (continuous)                                      |            | -            | $\pm 20$               | mA     |
| $V_{es}$       | electrostatic handling   | note 2     | -2000        | +2000                  | V      |
|                |  | note 3     | -200         | +200                   | V      |
| $T_{amb}$      | ambient temperature  |            | -10          | +70                    | °C     |
| $T_{stg}$      | storage temperature  |            | -55          | +125                   | °C     |

### Notes

- All  $V_{DD}$  (and  $V_{pos}$ ) connections and  $V_{SS}$  (and  $V_{neg}$ ) connections must be made externally to the same power supply.
- Equivalent to discharging a 100 pF capacitor via a 1.5 k $\Omega$  series resistor with a rise time of 15 ns.
- Equivalent to discharging a 200 pF capacitor via a 2.5  $\mu$ H series inductor.

## 9 CHARACTERISTICS

$V_{DD} = 3.0$  to  $3.6$  V;  $V_{SS} = 0$  V;  $T_{amb} = -10$  to  $+70$  °C; unless otherwise specified.

| SYMBOL  | PARAMETER  | CONDITIONS                   | MIN. | TYP. | MAX. | UNIT       |
|---|--|------------------------------|------|------|------|------------|
| <b>Supply</b>   |  |                              |      |      |      |            |
| $V_{DD}$  | supply voltage                                       |                              | 3.0  | 3.3  | 3.6  | V          |
| $I_{DD}$  | supply current                                       | $V_{DD} = 3.3$ V; n = 1 mode | -    | 20   | -    | mA         |
|   |  | $V_{DD} = 3.3$ V; n = 2 mode | -    | 25   | -    | mA         |
|   |  | $V_{DD} = 3.3$ V; n = 4 mode | -    | 30   | -    | mA         |
| <b>Bitstream DAC output (<math>V_{DDD} = 3.3</math> V, <math>V_{pos} = 3.3</math> V; <math>V_{SS} = 0</math> V, <math>V_{neg} = 0</math> V; <math>T_{amb} = 25</math> °C)</b> |  |                              |      |      |      |            |
| DIFFERENTIAL OUTPUTS: PINS LN, LP, RN AND RP  |  |                              |      |      |      |            |
| S/N   | signal-to-noise ratio                                | note 1                       | -85  | -90  | -    | dB         |
| (THD + N)/S   | total harmonic distortion plus noise-to-signal ratio | at 0 dB; note 1              | -    | -83  | -80  | dB         |
| <b>Servo and decoder analog functions (<math>V_{DDA} = 3.3</math> V; <math>V_{SSA} = 0</math> V; <math>T_{amb} = 25</math> °C)</b>  |  |                              |      |      |      |            |
| REFERENCE GENERATOR: PIN $I_{REF}$  |  |                              |      |      |      |            |
| $V_{Iref}$  | reference voltage level                              |                              | 1.14 | 1.2  | 1.26 | V          |
| $I_{ref}$   | input reference current                              |                              | -    | 40   | -    | $\mu$ A    |
| $R_{Iref}$  | external resistor                                    | $\pm 2\%$                    | -    | 30   | -    | k $\Omega$ |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL  | PARAMETER   | CONDITIONS                                    | MIN.         | TYP.        | MAX.              | UNIT             |
|---|---|---|--------------|-------------|-------------------|------------------|
| <b>Decoder analog front-end (<math>V_{DDA} = 3.3\text{ V}</math>; <math>V_{SSA} = 0\text{ V}</math>; <math>T_{amb} = 25\text{ }^{\circ}\text{C}</math>)</b>                                     |   |   |              |             |                   |                  |
| COMPARATOR INPUTS: PINS HFIN AND HFREF  |   |   |              |             |                   |                  |
| $f_{clk}$   | clock frequency   | note 2  | 8            | –           | 70                | MHz              |
| $V_{th(sw)}$  | switching voltage threshold                                 |   | –            | $0.5V_{DD}$ | –                 | V                |
| $V_{i(HFIN)}$   | input voltage level pin HFIN                                |   | –            | 1.0         | –                 | V                |
| <b>Servo analog part (<math>V_{DDA} = 3.3\text{ V}</math>; <math>V_{SSA} = 0\text{ V}</math>; <math>T_{amb} = 25\text{ }^{\circ}\text{C}</math>; <math>R_{Iref} = 30\text{ k}\Omega</math>)</b> |   |   |              |             |                   |                  |
| PINS D1 TO D4; R1 AND R2  |   |   |              |             |                   |                  |
| $I_{D(max)}$  | maximum input current for central diode input signal        | note 3  | 1.006        | –           | 16.1              | $\mu\text{A}$    |
| $I_{R(max)}$  | maximum input current for satellite diode input signal      | note 3  | 1.006        | –           | 16.1              | $\mu\text{A}$    |
| $V_{RIN}$   | internally generated reference voltage                      | note 4  | –            | 0.75        | –                 | V                |
|   | externally generated reference voltage applied to $V_{RIN}$ | note 4  | 0.5          | –           | $0.5V_{DD} + 0.1$ | V                |
| (THD + N)/S   | total harmonic distortion plus noise-to-signal ratio        | at 0 dB; note 5                               | –            | –50         | –45               | dB               |
| S/N   | signal-to-noise ratio                                       |   | –            | 55          | –                 | dB               |
| PSRR  | power supply ripple rejection at $V_{DDA2}$                 | note 6  | –            | 45          | –                 | dB               |
| $G_{tol}$   | gain tolerance  | note 7  | –20          | 0           | +20               | %                |
| $\Delta G_v$  | variation of gain between channels                          |   | –            | –           | 2                 | %                |
| $\alpha_{CS}$   | channel separation  |   | –            | 60          | –                 | dB               |
| <b>Digital inputs</b>   |   |   |              |             |                   |                  |
| PINS RESET 5 V TOLERANT (CMOS INPUT WITH PULL-UP RESISTOR AND HYSTERESIS)   |   |   |              |             |                   |                  |
| $V_{thr(sw)}$   | switching voltage threshold rising                          |   | –            | –           | $0.8V_{DDD}$      | V                |
| $V_{thf(sw)}$   | switching voltage threshold falling                         |   | $0.2V_{DDD}$ | –           | –                 | V                |
| $V_{hys}$   | hysteresis voltage  |   | 0.4          | –           | –                 | V                |
| $R_{i(pu)}$   | input pull-up resistance                                    | $V_i = 0\text{ V}$ , $V_{DDD} = 3.3\text{ V}$ | –            | 50          | –                 | $\text{k}\Omega$ |
| $C_i$   | input capacitance   |   | –            | –           | 10                | pF               |
| $t_{resL}$  | reset pulse width (active LOW)                              | RESET only                                    | 1            | –           | –                 | $\mu\text{s}$    |
| PIN V1 (CMOS INPUT WITH PULL-UP RESISTOR)   |   |   |              |             |                   |                  |
| $V_{thr(sw)}$   | switching voltage threshold rising                          |   | –            | –           | $0.8V_{DDD}$      | V                |
| $V_{thf(sw)}$   | switching voltage threshold falling                         |   | $0.2V_{DDD}$ | –           | –                 | V                |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL  | PARAMETER                  | CONDITIONS  | MIN.             | TYP.          | MAX.             | UNIT          |
|---|----------------------------|---|------------------|---------------|------------------|---------------|
| $V_{hys}$   | hysteresis voltage         |   | –                | $0.3V_{DDDD}$ | –                | V             |
| $R_{i(pu)}$   | input pull-up resistor     | $V_i = 0\text{ V}; V_{DDDD} = 3.3\text{ V}$                         | –                | 50            | –                | $k\Omega$     |
| $C_i$   | input capacitance          |   | –                | –             | 10               | pF            |
| <b>PIN SELPLL (CMOS INPUT WITH PULL-UP RESISTOR)</b>                      |                            |   |                  |               |                  |               |
| $V_{IL}$  | LOW-level input voltage    |   | –0.3             | –             | $0.3V_{DDDD}$    | V             |
| $V_{IH}$  | HIGH-level input voltage   |   | $0.7V_{DDDD}$    | –             | $V_{DDDD} + 0.3$ | V             |
| $R_{i(pu)}$   | input pull-up resistance   | $V_i = 0\text{ V}; V_{DDDD} = 3.3\text{ V}$                         | –                | 50            | –                | $k\Omega$     |
| $C_i$   | input capacitance          |   | –                | –             | 10               | pF            |
| <b>PINS TEST1, TEST2 AND TEST3 (CMOS INPUTS WITH PULL-DOWN RESISTORS)</b> |                            |   |                  |               |                  |               |
| $V_{IL}$  | LOW-level input voltage    |   | –0.3             | –             | $0.3V_{DDDD}$    | V             |
| $V_{IH}$  | HIGH-level input voltage   |   | $0.7V_{DDDD}$    | –             | $V_{DDDD} + 0.3$ | V             |
| $R_{i(pd)}$   | input pull-down resistance | $V_i = V_{DDDD} = 3.3\text{ V}$                                     | –                | 50            | –                | $k\Omega$     |
| $C_i$   | input capacitance          |   | –                | –             | 10               | pF            |
| <b>PINS RCK, WCLI, SDI AND SCLI (CMOS INPUTS)</b>                         |                            |   |                  |               |                  |               |
| $V_{IL}$  | LOW-level input voltage    |   | –0.3             | –             | $0.3V_{DDDD}$    | V             |
| $V_{IH}$  | HIGH-level input voltage   |   | $0.7V_{DDDD}$    | –             | $V_{DDDD} + 0.3$ | V             |
| $I_{LI}$  | input leakage current      | $V_i = 0\text{ to }V_{DDDD}$  | –5               | –             | +5               | $\mu\text{A}$ |
| $C_i$   | input capacitance          |   | –                | –             | 10               | pF            |
| <b>PINS SCL, SILD AND RAB (5 V TOLERANT CMOS INPUTS)</b>                  |                            |   |                  |               |                  |               |
| $V_{IL}$  | LOW-level input voltage    |   | –0.3             | –             | $0.2V_{DDDD}$    | V             |
| $V_{IH}$  | HIGH-level input voltage   |   | $0.8V_{DDDD}$    | –             | 5.5              | V             |
| $I_{LI}$  | input leakage current      | $V_i = 0\text{ to }V_{DDDD}$  | –5               | –             | +5               | $\mu\text{A}$ |
| $C_i$   | input capacitance          |   | –                | –             | 10               | pF            |
| <b>Digital outputs</b>  |                            |   |                  |               |                  |               |
| <b>PINS V4 AND V5</b>   |                            |   |                  |               |                  |               |
| $V_{OL}$  | LOW-level output voltage   | $I_{OL} = 4\text{ mA}$  | 0                | –             | 0.4              | V             |
| $V_{OH}$  | HIGH-level output voltage  | $I_{OH} = -4\text{ mA}$   | $V_{DDDD} - 0.4$ | –             | $V_{DDDD}$       | V             |
| $C_L$   | load capacitance           |   | –                | –             | 100              | pF            |
| $t_{o(r)}$  | output rise time           | $C_L = 20\text{ pF};$<br>$0.4\text{ to } (V_{DDDD} - 0.4)\text{ V}$ | –                | –             | 10               | ns            |
| $t_{o(f)}$  | output fall time           | $C_L = 20\text{ pF};$<br>$(V_{DDDD} - 0.4)\text{ to }0.4\text{ V}$  | –                | –             | 10               | ns            |
| <b>Open-drain outputs</b>   |                            |   |                  |               |                  |               |
| <b>PINS CFLG, STATUS, KILL AND LDON (OPEN-DRAIN OUTPUT)</b>               |                            |   |                  |               |                  |               |
| $V_{OL}$  | LOW-level output voltage   | $I_{OL} = 1\text{ mA}$  | 0                | –             | 0.4              | V             |
| $I_{OL}$  | LOW-level output current   |   | –                | –             | 2                | mA            |
| $C_L$   | load capacitance           |   | –                | –             | 50               | pF            |
| $t_{o(f)}$  | output fall time           | $C_L = 50\text{ pF};$<br>$(V_{DDDD} - 0.4)\text{ to }0.4\text{ V}$  | –                | –             | 30               | ns            |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL  | PARAMETER                                   | CONDITIONS  | MIN.            | TYP.         | MAX.          | UNIT          |
|---|---|---|-----------------|--------------|---------------|---------------|
| <b>3-state outputs</b>  |   |   |                 |              |               |               |
| PINS EF, SCLK, WCLK, DATA, CL16, RA, FO, SL, SBSY, SFSY, SUB AND CL11/4       |   |   |                 |              |               |               |
| $V_{OL}$  | LOW-level output voltage                    | $I_{OL} = 1 \text{ mA}$   | 0               | –            | 0.4           | V             |
| $V_{OH}$  | HIGH-level output voltage                   | $I_{OH} = -1 \text{ mA}$  | $V_{DDD} - 0.4$ | –            | $V_{DDD}$     | V             |
| $C_L$   | load capacitance                            |   | –               | –            | 35            | pF            |
| $t_{o(r)}$  | output rise time                            | $C_L = 20 \text{ pF};$<br>0.4 to $(V_{DDD} - 0.4) \text{ V}$          | –               | –            | 15            | ns            |
| $t_{o(f)}$  | output fall time                            | $C_L = 20 \text{ pF};$<br>$(V_{DDD} - 0.4) \text{ to } 0.4 \text{ V}$ | –               | –            | 15            | ns            |
| $I_{ZO}$  | output 3-state leakage current              | $V_i = 0 \text{ to } V_{DD}$  | –5              | –            | +5            | $\mu\text{A}$ |
| (WHEN CL11/4 IS CONFIGURED AS CL11 OUTPUT)                                    |   |   |                 |              |               |               |
| $t_{OH}$  | output HIGH time (relative to clock period) | $V_o = 1.5 \text{ V}$   | 45              | 50           | 55            | %             |
| PINS MOTO1, MOTO2 AND DOBM  |   |   |                 |              |               |               |
| $V_{OL}$  | LOW-level output voltage                    | $I_{OL} = 4 \text{ mA}$   | 0               | –            | 0.4           | V             |
| $V_{OH}$  | HIGH-level output voltage                   | $I_{OH} = -4 \text{ mA}$  | $V_{DDD} - 0.4$ | –            | $V_{DD}$      | V             |
| $C_L$   | load capacitance                            |   | –               | –            | 100           | pF            |
| $t_{o(r)}$  | output rise time                            | $C_L = 20 \text{ pF};$<br>0.4 to $(V_{DDD} - 0.4) \text{ V}$          | –               | –            | 10            | ns            |
| $t_{o(f)}$  | output fall time                            | $C_L = 20 \text{ pF};$<br>$(V_{DDD} - 0.4) \text{ to } 0.4 \text{ V}$ | –               | –            | 10            | ns            |
| $I_{ZO}$  | output 3-state leakage current              | $V_i = 0 \text{ to } V_{DDD}$   | –5              | –            | +5            | $\mu\text{A}$ |
| <b>Digital input/output</b>   |   |   |                 |              |               |               |
| PIN SDA (5 V TOLERANT CMOS INPUT/OPEN-DRAIN I <sup>2</sup> C-BUS OUTPUT)      |   |   |                 |              |               |               |
| $V_{IL}$  | LOW-level input voltage                     |   | –0.3            | –            | $+0.2V_{DDD}$ | V             |
| $V_{IH}$  | HIGH-level input voltage                    |   | $0.8V_{DDD}$    | –            | 5.5           | V             |
| $I_{ZO}$  | 3-state leakage current                     | $V_i = 0 \text{ to } V_{DDD}$   | –5              | –            | +5            | $\mu\text{A}$ |
| $C_i$   | input capacitance                           |   | –               | –            | 10            | pF            |
| $V_{OL}$  | LOW-level output voltage                    | $I_{OL} = 2 \text{ mA}$   | 0               | –            | 0.4           | V             |
| $I_{OL}$  | LOW-level output current                    |   | –               | –            | 6             | mA            |
| $C_L$   | load capacitance                            |   | –               | –            | 50            | pF            |
| $t_{o(f)}$  | output fall time                            | $C_L = 20 \text{ pF};$<br>$0.85V_{DDD} \text{ to } 0.4 \text{ V}$     | –               | –            | 15            | ns            |
| PIN V2/V3 (CMOS INPUT WITH PULL-UP RESISTOR AND HYSTERESIS/OPEN-DRAIN OUTPUT) |   |   |                 |              |               |               |
| $V_{thr(sw)}$   | switching voltage threshold rising          |   | –               | –            | $0.8V_{DDD}$  | V             |
| $V_{thf(sw)}$   | switching voltage threshold falling         |   | $0.2V_{DDD}$    | –            | –             | V             |
| $V_{hys}$   | hysteresis voltage                          |   | –               | $0.3V_{DDD}$ | –             | V             |

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL                              | PARAMETER                      | CONDITIONS   | MIN.        | TYP.   | MAX.           | UNIT          |
|-------------------------------------|--------------------------------|--|-------------|--------|----------------|---------------|
| $R_{I(pu)}$                         | input pull-up resistance       | $V_i = 0 \text{ V}; V_{DD} = 3.3 \text{ V}$                          | –           | 50     | –              | $k\Omega$     |
| $C_i$                               | input capacitance              |  | –           | –      | 10             | $\mu\text{F}$ |
| $V_{OL}$                            | LOW-level output voltage       | $I_{OL} = 1 \text{ mA}$  | 0           | –      | 0.4            | V             |
| $I_{OL}$                            | LOW-level output current       |  | –           | –      | 1              | mA            |
| $C_L$                               | load capacitance               |  | –           | –      | 25             | $\mu\text{F}$ |
| $t_{o(f)}$                          | output fall time               | $C_L = 20 \text{ pF};$<br>$(V_{DD} - 0.4) \text{ to } 0.4 \text{ V}$ | –           | –      | 15             | ns            |
| <b>Crystal oscillator</b>           |                                |  |             |        |                |               |
| INPUT: PIN CRIN (EXTERNAL CLOCK)    |                                |  |             |        |                |               |
| $V_{IL}$                            | LOW-level input voltage        |  | –0.3        | –      | $+0.2V_{DD}$   | V             |
| $V_{IH}$                            | HIGH-level input voltage       |  | $0.8V_{DD}$ | –      | $V_{DD} + 0.3$ | V             |
| $I_{LI}$                            | input leakage current          |  | –10         | –      | +10            | $\mu\text{A}$ |
| $C_i$                               | input capacitance              |  | –           | –      | 10             | $\mu\text{F}$ |
| OUTPUT: PIN CROUT; SEE FIGS 3 AND 4 |                                |  |             |        |                |               |
| $f_{xtal}$                          | crystal frequency              | $\pm 100 \text{ ppm}$  | 8           | 8.4672 | 35             | MHz           |
| $g_m$                               | mutual conductance at start-up |  | 17          | –      | –              | $\text{mA/V}$ |
| $C_{fb}$                            | feedback capacitance           |  | –           | –      | 2              | $\mu\text{F}$ |
| $C_o$                               | output capacitance             |  | –           | –      | 7              | $\mu\text{F}$ |

**Notes**

- Assumes use of external components as shown in the application diagram (Figs 38 or 39).
- Highest clock frequency at which data slicer produces 1010 output in analog self-test mode.
- The maximum input current depends on the value of the external resistor connected to  $I_{ref}$  and the settings of shadow registers A and C:
  - With  $R_{Iref} = 30 \text{ k}\Omega$ , minimum  $I_{max} = (0.025) \cdot I_{ref} \Rightarrow (0.025) \times (40 \text{ }\mu\text{A}) = 1 \text{ }\mu\text{A}$ .
  - With  $R_{Iref} = 30 \text{ k}\Omega$ , maximum  $I_{max} = (0.4) \cdot I_{ref} \Rightarrow (0.4) \times (40 \text{ }\mu\text{A}) = 16 \text{ }\mu\text{A}$ .
- $V_{RIN}$  can be set to an internal source or an externally applied reference voltage using shadow register 7.
- Measuring bandwidth: 200 Hz to 20 kHz,  $f_{i(ADC)} = 1 \text{ kHz}$ .
- $f_{ripple} = 1 \text{ kHz}$ ,  $V_{ripple} = 0.5 \text{ V (p-p)}$ .
- Gain of the ADC is defined as  $G_{ADC} = f_{sys}/I_{max}$  (counts/ $\mu\text{A}$ ); thus digital output =  $I_i \times G_{ADC}$  where:
  - Digital output = the number of pulses at the digital output in counts/s and  $I_i$  = the DC input current in  $\mu\text{A}$ .
  - The maximum input current depends on  $R_{Iref}$  and on shadow registers A and C.
  - The gain tolerance is the deviation from the calculated gain.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 10 OPERATING CHARACTERISTICS (SUBCODE INTERFACE TIMING)

$V_{DD} = 3.0$  to  $3.6$  V;  $V_{SS} = 0$  V;  $T_{amb} = -10$  to  $+70$  °C; unless otherwise specified.

| SYMBOL   | PARAMETER                             | MIN.   | TYP.   | MAX.   | UNIT    |
|--|---------------------------------------|--------|--------|--------|---------|
| <b>Subcode interface timing (single speed <math>\times n</math>); see Fig.32; note 1</b> |                                       |        |        |        |         |
| INPUT: PIN RCK   |                                       |        |        |        |         |
| $t_{CLKH}$   | input clock HIGH time                 | 2/n    | 4/n    | 6/n    | $\mu s$ |
| $t_{CLKL}$   | input clock LOW time                  | 2/n    | 4/n    | 6/n    | $\mu s$ |
| $t_r$  | input clock rise time                 | –      | –      | 80/n   | ns      |
| $t_f$  | input clock fall time                 | –      | –      | 80/n   | ns      |
| $t_{d(SFSY-RCK)}$  | delay time SFSY to RCK                | 10/n   | –      | 20/n   | $\mu s$ |
| OUTPUTS: PINS SBSY, SFSY AND SUB ( $C_L = 20$ PF)  |                                       |        |        |        |         |
| $T_{cy(block)}$  | block cycle time                      | 12.0/n | 13.3/n | 14.7/n | ms      |
| $t_{W(SBSY)}$  | SBSY pulse width                      | –      | –      | 300/n  | $\mu s$ |
| $T_{cy(frame)}$  | frame cycle time                      | 122/n  | 136/n  | 150/n  | $\mu s$ |
| $t_{W(SFSY)}$  | SFSY pulse width (3-wire mode only)   | –      | –      | 366/n  | $\mu s$ |
| $t_{SFSYH}$  | SFSY HIGH time                        | –      | –      | 66/n   | $\mu s$ |
| $t_{SFSYL}$  | SFSY LOW time                         | –      | –      | 84/n   | $\mu s$ |
| $t_{d(SFSY-SUB)}$  | delay time SFSY to SUB (P data) valid | –      | –      | 1/n    | $\mu s$ |
| $t_{d(RCK-SUB)}$   | delay time RCK falling to SUB         | –      | –      | 0      | $\mu s$ |
| $t_{h(RCK-SUB)}$   | hold time RCK to SUB                  | –      | –      | 0.7/n  | $\mu s$ |

### Note

- The subcode timing is directly related to the overspeed factor 'n' in normal operating mode. 'n' is replaced by the disc speed factor 'd', in lock-to-disc mode.

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

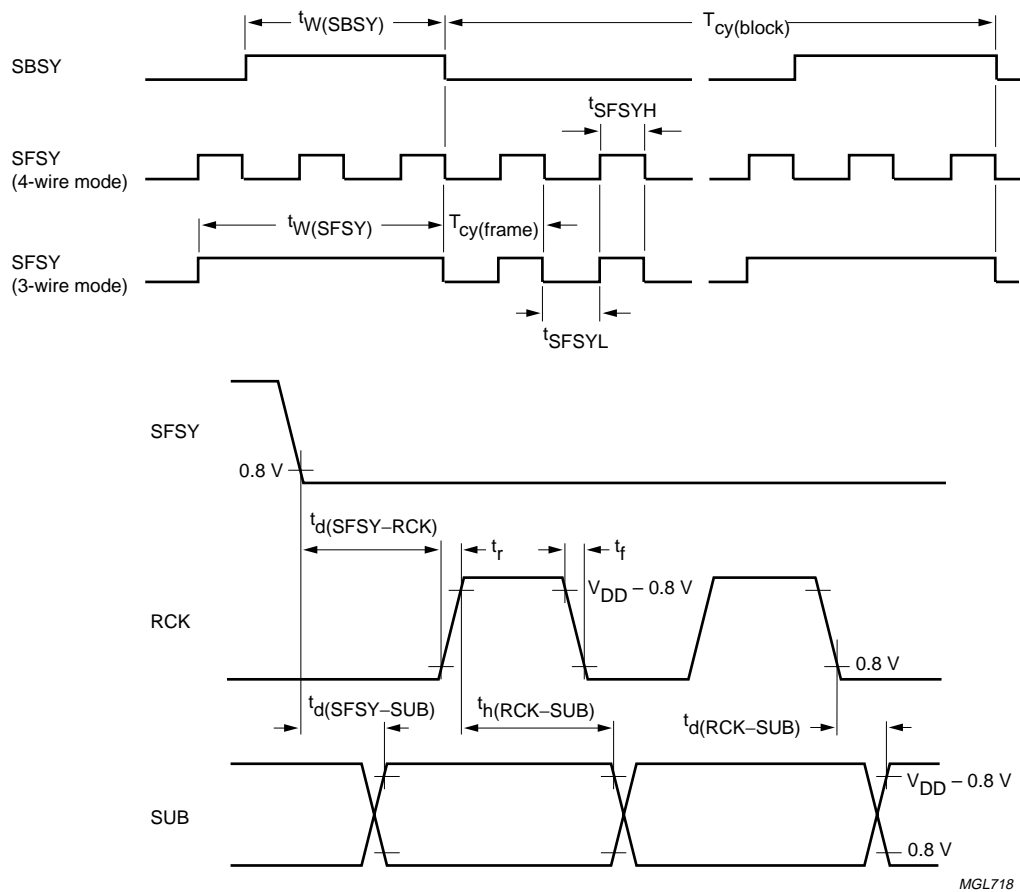


Fig.32 Subcode interface timing diagram.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 11 OPERATING CHARACTERISTICS (I<sup>2</sup>S-BUS TIMING)

V<sub>DD</sub> = 3.0 to 3.6 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -10 to +70 °C; unless otherwise specified.

| SYMBOL  | PARAMETER           | CONDITIONS                    | MIN.  | TYP.    | MAX. | UNIT |
|---|---------------------|-------------------------------|-------|---------|------|------|
| <b>I<sup>2</sup>S-bus timing (single-speed × n); see Fig.33; note 1</b> |                     |                               |       |         |      |      |
| CLOCK OUTPUT: PIN SCLK (C <sub>L</sub> = 20 pF)                         |                     |                               |       |         |      |      |
| T <sub>cy</sub>   | output clock period | sample rate = f <sub>s</sub>  | –     | 472.4/n | –    | ns   |
|   |                     | sample rate = 2f <sub>s</sub> | –     | 236.2/n | –    | ns   |
|   |                     | sample rate = 4f <sub>s</sub> | –     | 118.1/n | –    | ns   |
| t <sub>CH</sub>   | clock HIGH time     | sample rate = f <sub>s</sub>  | 166/n | –       | –    | ns   |
|   |                     | sample rate = 2f <sub>s</sub> | 83/n  | –       | –    | ns   |
|   |                     | sample rate = 4f <sub>s</sub> | 42/n  | –       | –    | ns   |
| t <sub>CL</sub>   | clock LOW time      | sample rate = f <sub>s</sub>  | 166/n | –       | –    | ns   |
|   |                     | sample rate = 2f <sub>s</sub> | 83/n  | –       | –    | ns   |
|   |                     | sample rate = 4f <sub>s</sub> | 42/n  | –       | –    | ns   |
| OUTPUTS: PINS WCLK, DATA AND EF (C <sub>L</sub> = 20 pF)                |                     |                               |       |         |      |      |
| t <sub>su</sub>   | set-up time         | sample rate = f <sub>s</sub>  | 95/n  | –       | –    | ns   |
|   |                     | sample rate = 2f <sub>s</sub> | 48/n  | –       | –    | ns   |
|   |                     | sample rate = 4f <sub>s</sub> | 24/n  | –       | –    | ns   |
| t <sub>h</sub>  | hold time           | sample rate = f <sub>s</sub>  | 95/n  | –       | –    | ns   |
|   |                     | sample rate = 2f <sub>s</sub> | 48/n  | –       | –    | ns   |
|   |                     | sample rate = 4f <sub>s</sub> | 24/n  | –       | –    | ns   |

**Note**

- The I<sup>2</sup>S-bus timing is directly related to the overspeed factor 'n' in the normal operating mode. In the lock-to-disc mode 'n' is replaced by the disc speed factor 'd'.

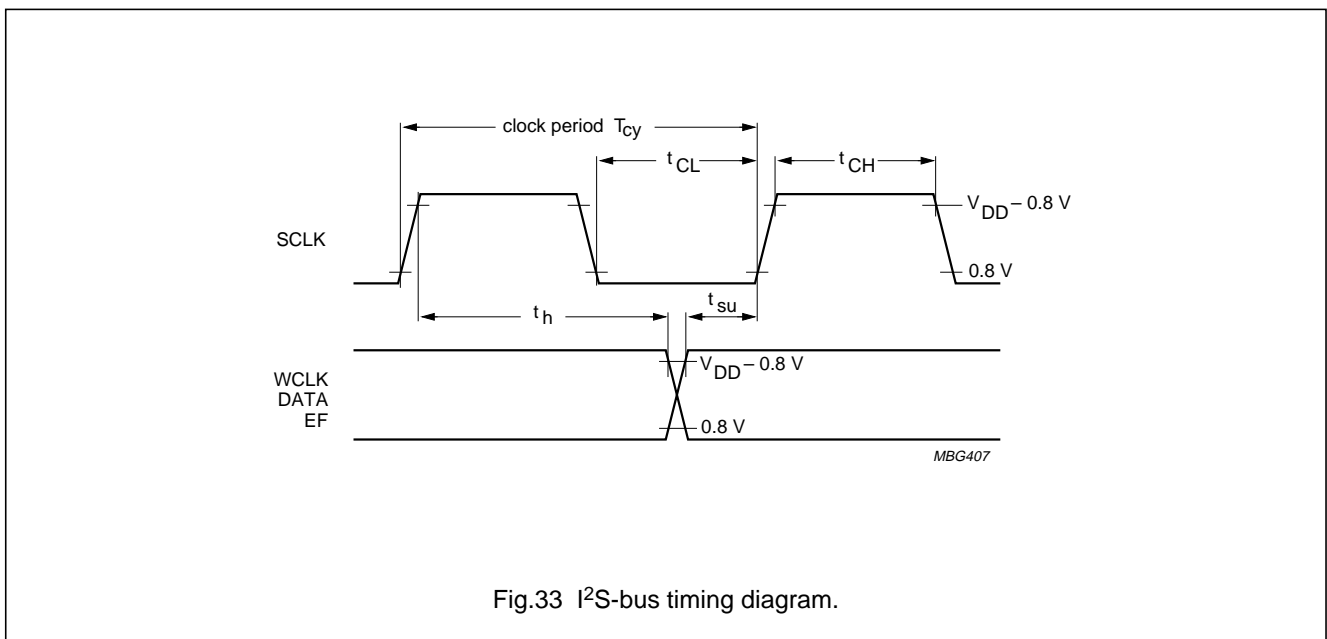


Fig.33 I<sup>2</sup>S-bus timing diagram.



# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 12 OPERATING CHARACTERISTICS (MICROCONTROLLER INTERFACE TIMING)

$V_{DD} = 3.0$  to  $3.6$  V;  $V_{SS} = 0$  V;  $T_{amb} = -10$  to  $+70$  °C; unless otherwise specified.

| SYMBOL   | PARAMETER                             | CONDITIONS | NORMAL MODE  |              | LOCK-TO-DISC MODE |               | UNIT |
|--|---------------------------------------|------------|--------------|--------------|-------------------|---------------|------|
|  |                                       |            | MIN.         | MAX.         | MIN.              | MAX.          |      |
| <b>Microcontroller interface timing (4-wire bus mode; writing to decoder registers 0 to F; reading Q-channel subcode and decoder status); see Figs 34 and 35; note 1</b> |                                       |            |              |              |                   |               |      |
| INPUTS SCL AND RAB   |                                       |            |              |              |                   |               |      |
| $t_{CL}$   | input LOW time                        |            | $480/n + 20$ | –            | $2400/n + 20$     | –             | ns   |
| $t_{CH}$   | input HIGH time                       |            | $480/n + 20$ | –            | $2400/n + 20$     | –             | ns   |
| $t_r$  | rise time                             |            | –            | $480/n$      | –                 | $480/n$       | ns   |
| $t_f$  | fall time                             |            | –            | $480/n$      | –                 | $480/n$       | ns   |
| READ MODE ( $C_L = 20$ pF)   |                                       |            |              |              |                   |               |      |
| $t_{dRD}$  | delay time RAB to SDA valid           |            | –            | 50           | –                 | 50            | ns   |
| $t_{PD}$   | propagation delay SCL to SDA          |            | $720/n - 20$ | $960/n + 20$ | $720/n + 20$      | $4800/n + 20$ | ns   |
| $t_{dRZ}$  | delay time RAB to SDA high-impedance  |            | –            | 50           | –                 | 50            | ns   |
| WRITE MODE ( $C_L = 20$ pF)  |                                       |            |              |              |                   |               |      |
| $t_{suD}$  | set-up time SDA to SCL                | note 2     | $20 - 720/n$ | –            | $20 - 720/n$      | –             | ns   |
| $t_{hD}$   | hold time SCL to SDA                  |            | –            | $960/n + 20$ | –                 | $4800/n + 20$ | ns   |
| $t_{suCR}$   | set-up time SCL to RAB                |            | $240/n + 20$ | –            | $1200/n + 20$     | –             | ns   |
| $t_{dWZ}$  | delay time SDA high-impedance to RAB  |            | 0            | –            | 0                 | –             | ns   |
| <b>Microcontroller interface timing (4-wire bus mode; servo commands); see Figs 36 and 37; note 3</b>  |                                       |            |              |              |                   |               |      |
| INPUTS SCL AND SILD  |                                       |            |              |              |                   |               |      |
| $t_L$  | input LOW time                        |            | 710          | –            | 710               | –             | ns   |
| $t_H$  | input HIGH time                       |            | 710          | –            | 710               | –             | ns   |
| $t_r$  | rise time                             |            | –            | 240          | –                 | 240           | ns   |
| $t_f$  | fall time                             |            | –            | 240          | –                 | 240           | ns   |
| READ MODE ( $C_L = 20$ pF)   |                                       |            |              |              |                   |               |      |
| $t_{dLD}$  | delay time SILD to SDA valid          |            | –            | 25           | –                 | 25            | ns   |
| $t_{PD}$   | propagation delay SCL to SDA          |            | –            | 950          | –                 | 950           | ns   |
| $t_{dLZ}$  | delay time SILD to SDA high-impedance |            | –            | 50           | –                 | 50            | ns   |
| $t_{sCLR}$   | set-up time SCL to SILD               |            | 480          | –            | 480               | –             | ns   |
| $t_{hCLR}$   | hold time SILD to SCL                 |            | 830          | –            | 830               | –             | ns   |

Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

| SYMBOL                               | PARAMETER                             | CONDITIONS | NORMAL MODE |      | LOCK-TO-DISC MODE |      | UNIT          |
|--------------------------------------|---------------------------------------|------------|-------------|------|-------------------|------|---------------|
|                                      |                                       |            | MIN.        | MAX. | MIN.              | MAX. |               |
| WRITE MODE ( $C_L = 20 \text{ pF}$ ) |                                       |            |             |      |                   |      |               |
| $t_{sD}$                             | set-up time SDA to SCL                |            | 0           | –    | 0                 | –    | ns            |
| $t_{hD}$                             | hold time SCL to SDA                  |            | 950         | –    | 950               | –    | ns            |
| $t_{sCL}$                            | set-up time SCL to SILD               |            | 480         | –    | 480               | –    | ns            |
| $t_{hCL}$                            | hold time SILD to SCL                 |            | 120         | –    | 120               | –    | ns            |
| $t_{dPLP}$                           | delay between two SILD pulses         |            | 70          | –    | 70                | –    | $\mu\text{s}$ |
| $t_{dWZ}$                            | delay time SDA high-impedance to SILD |            | 0           | –    | 0                 | –    | ns            |

Notes

1. The 4-wire bus mode microcontroller interface timing for writing to decoder registers 0 to F, and reading Q-channel subcode and decoder status, is a function of the overspeed factor 'n'. In the lock-to-disc mode the maximum data rate is lower.
2. Negative set-up time means that the data may change after clock transition.
3. If a 16.9344 MHz crystal is used and SELPLL = 0 then the timings are divided-by-2 until the microcontroller has written X1XX to register B.

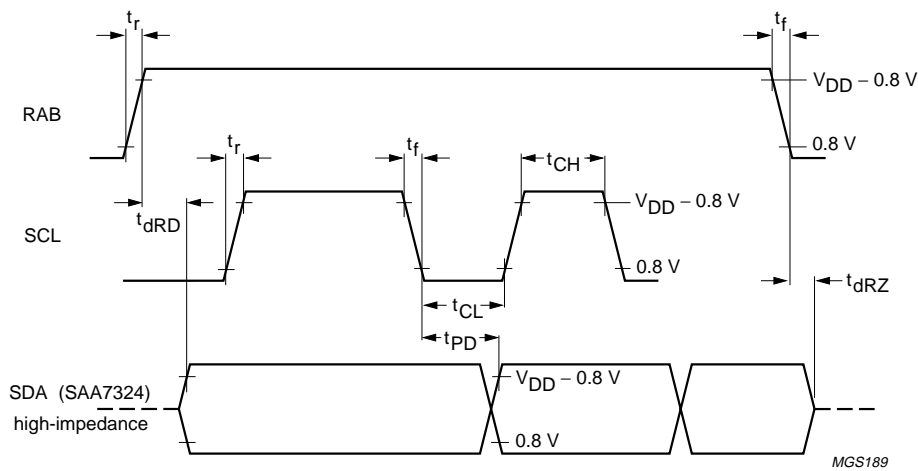
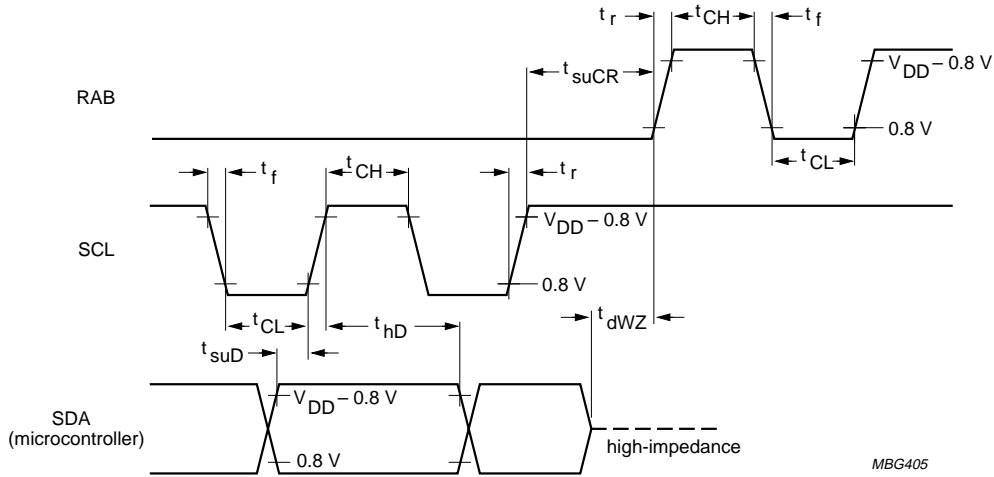


Fig.34 4-wire bus microcontroller timing; read mode (Q-channel subcode and decoder status information).

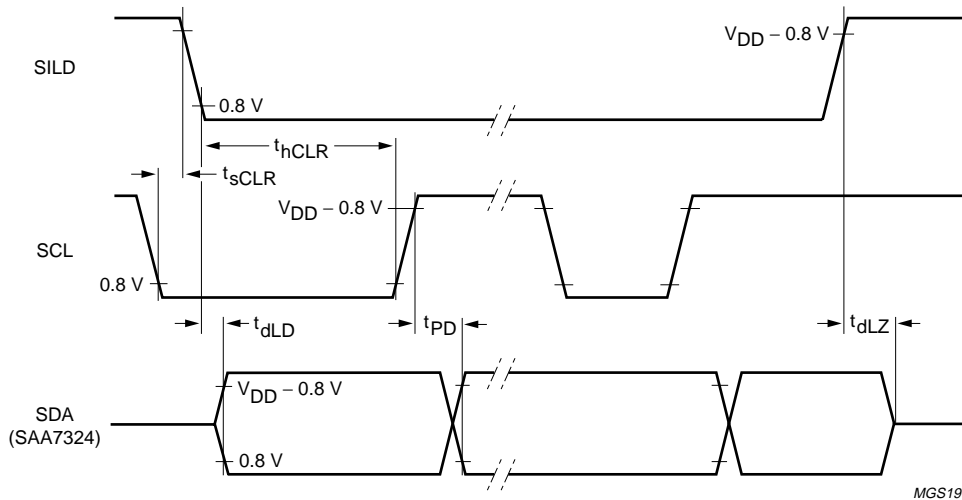
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MBG405

Fig.35 4-wire bus microcontroller timing; write mode (decoder registers 0 to F).

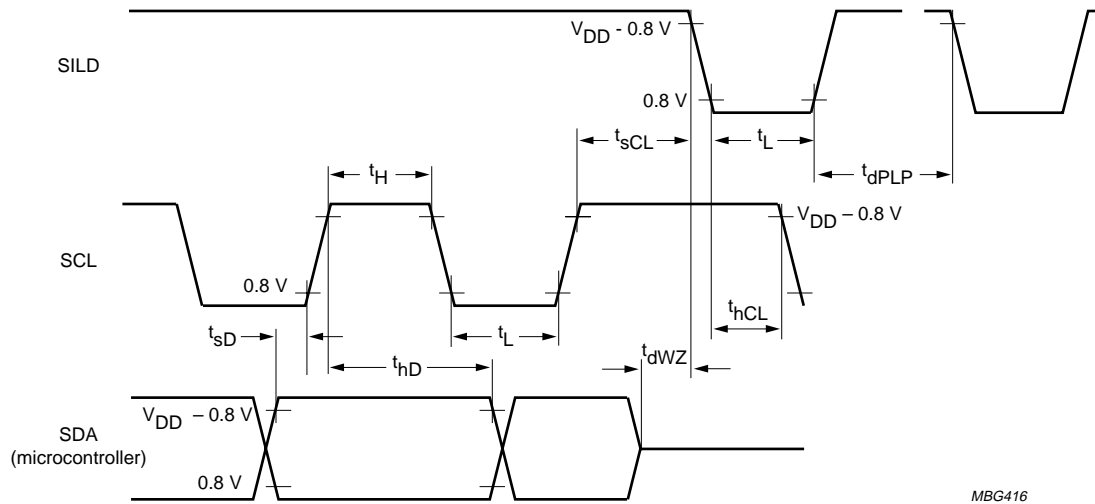


MGS190

Fig.36 4-wire bus microcontroller timing; read mode (servo commands).

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SAA7324



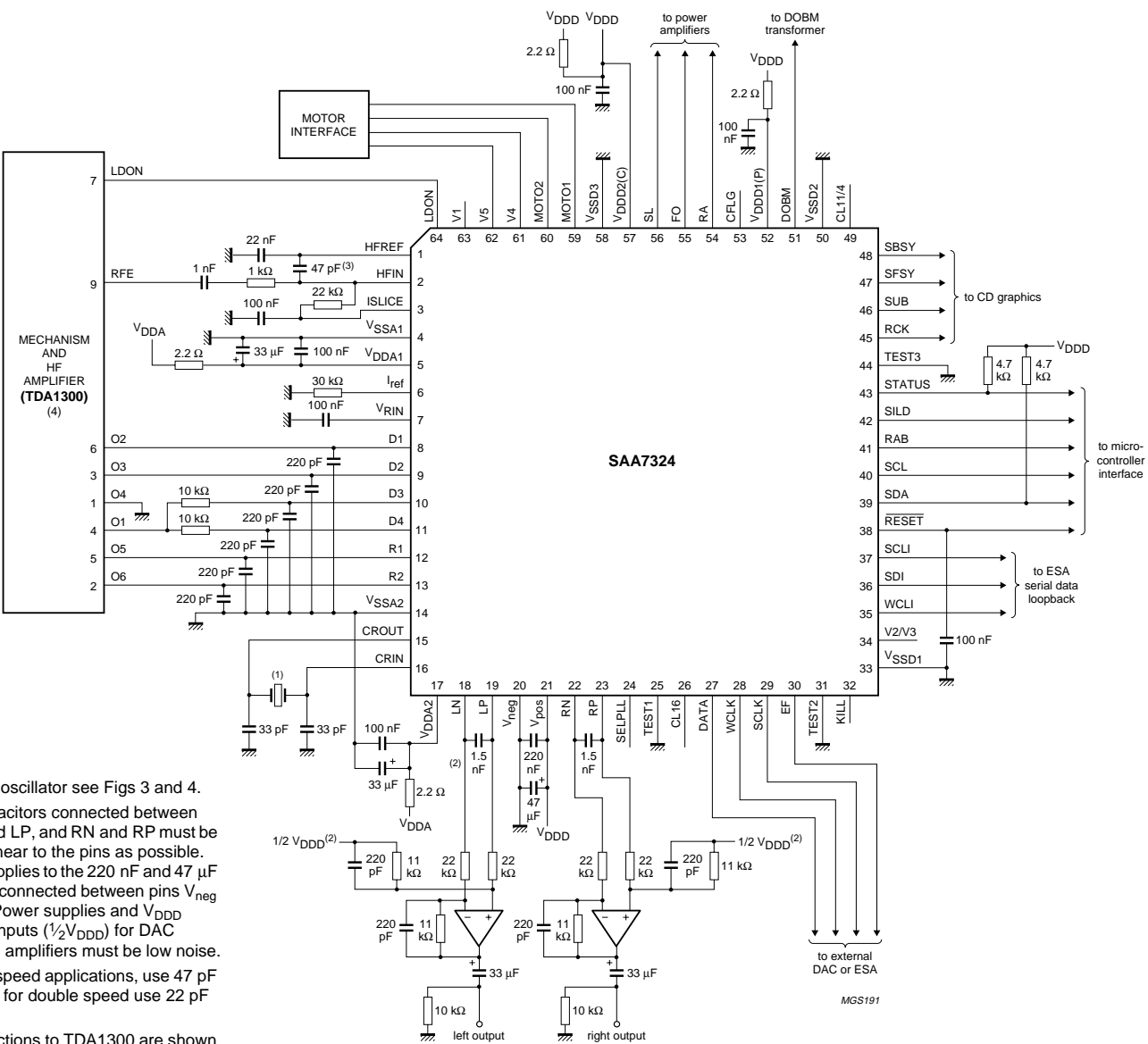
MBG416

Fig.37 4-wire bus microcontroller timing; write mode (servo commands).

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

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## 13 APPLICATION INFORMATION

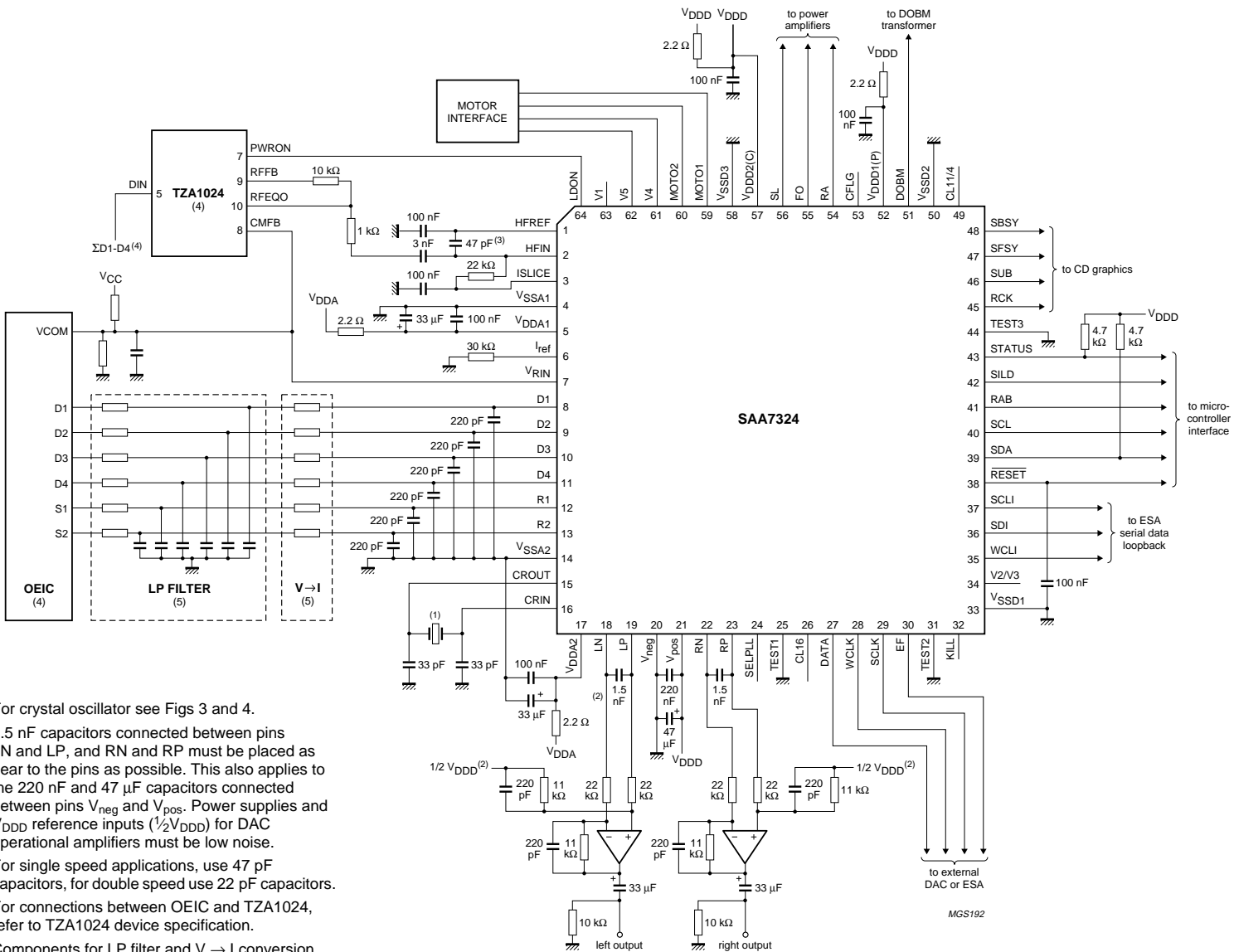


- (1) For crystal oscillator see Figs 3 and 4.
- (2) 1.5 nF capacitors connected between pins LN and LP, and RN and RP must be placed as near to the pins as possible. This also applies to the 220 nF and 47 μF capacitors connected between pins V<sub>neg</sub> and V<sub>pos</sub>. Power supplies and V<sub>DD</sub> reference inputs (1/2 V<sub>DD</sub>) for DAC operational amplifiers must be low noise.
- (3) For single speed applications, use 47 pF capacitors, for double speed use 22 pF capacitors.
- (4) The connections to TDA1300 are shown for single Foucault mechanisms.

Fig.38 Typical application diagram (for current mechanisms).

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324



- (1) For crystal oscillator see Figs 3 and 4.
- (2) 1.5 nF capacitors connected between pins LN and LP, and RN and RP must be placed as near to the pins as possible. This also applies to the 220 nF and 47 μF capacitors connected between pins V<sub>neg</sub> and V<sub>pos</sub>. Power supplies and V<sub>DDD</sub> reference inputs (1/2 V<sub>DDD</sub>) for DAC operational amplifiers must be low noise.
- (3) For single speed applications, use 47 pF capacitors, for double speed use 22 pF capacitors.
- (4) For connections between OEIC and TZA1024, refer to TZA1024 device specification.
- (5) Components for LP filter and V → I conversion depend on the OEIC and the current range set on SAA7324.

Fig.39 Typical application diagram (for voltage mechanisms).

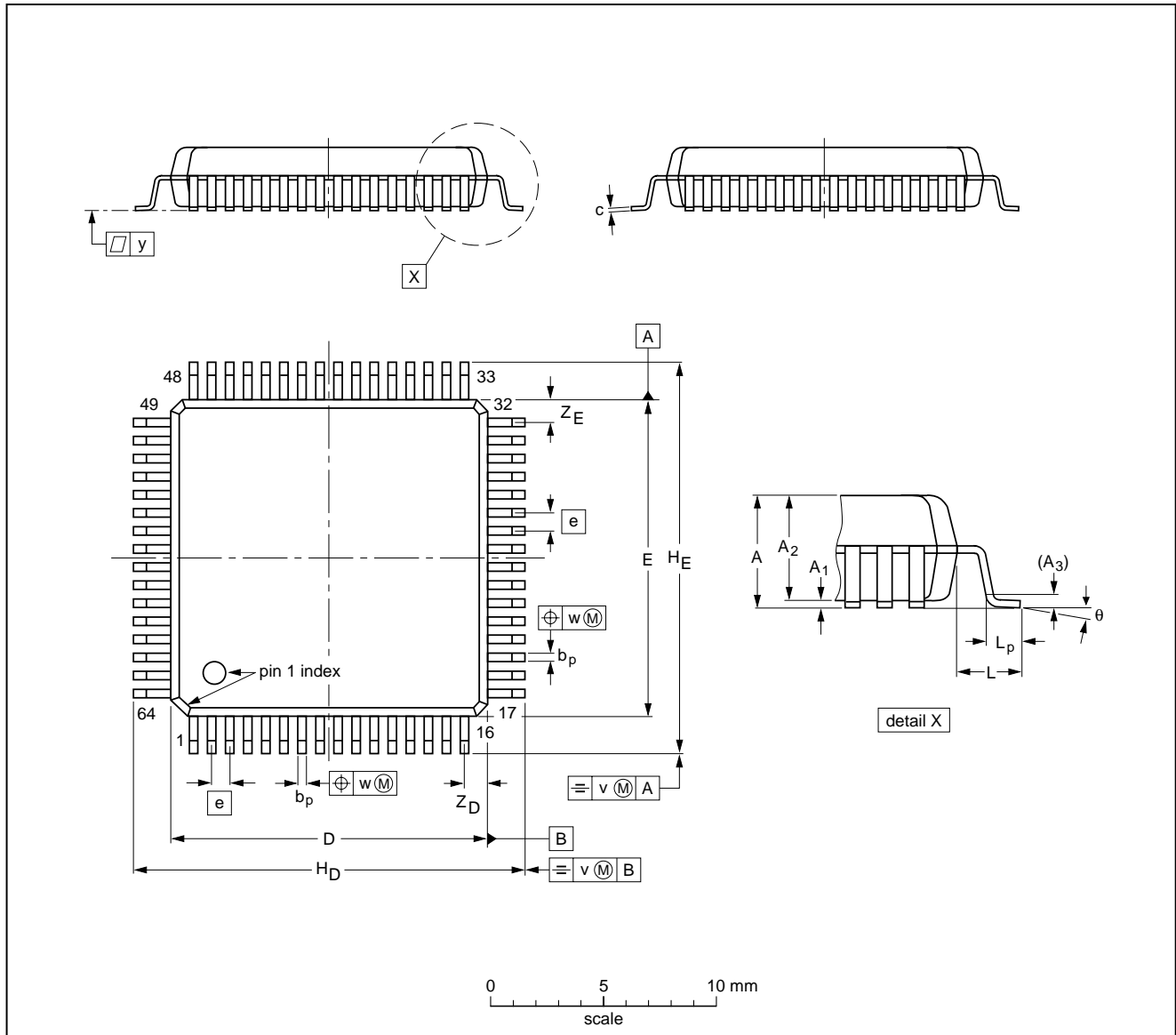
# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 14 PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm

SOT393-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L    | L <sub>p</sub> | v    | w    | y    | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|------|----------------|------|------|------|-------------------------------|-------------------------------|----------|
| mm   | 3.00   | 0.25<br>0.10   | 2.75<br>2.55   | 0.25           | 0.45<br>0.30   | 0.23<br>0.13 | 14.1<br>13.9     | 14.1<br>13.9     | 0.8 | 17.45<br>16.95 | 17.45<br>16.95 | 1.60 | 1.03<br>0.73   | 0.16 | 0.16 | 0.10 | 1.2<br>0.8                    | 1.2<br>0.8                    | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                      |
| SOT393-1        | 134E07     | MS-022 |      |  |                     | 99-12-27<br>00-01-19 |

## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 15 SOLDERING

#### 15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### 15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### 15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



## Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

### 15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                         | SOLDERING METHOD                  |                       |
|---------------------------------|-----------------------------------|-----------------------|
|                                 | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                       | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ   | suitable                          | suitable              |
| LQFP, QFP, TQFP                 | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                | not recommended <sup>(5)</sup>    | suitable              |

#### Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 16 DATA SHEET STATUS

| DATA SHEET STATUS         | PRODUCT STATUS | DEFINITIONS <sup>(1)</sup>   |
|---------------------------|----------------|--|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.  |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.   |

### Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

## 17 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

753503/02/pp68

Date of release: 2000 Jun 26

Document order number: 9397 750 06991

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