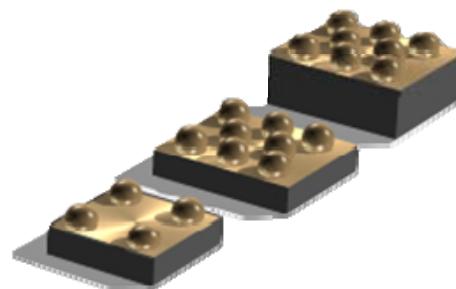




# ST Serial EEPROM WLCSP\* portfolio

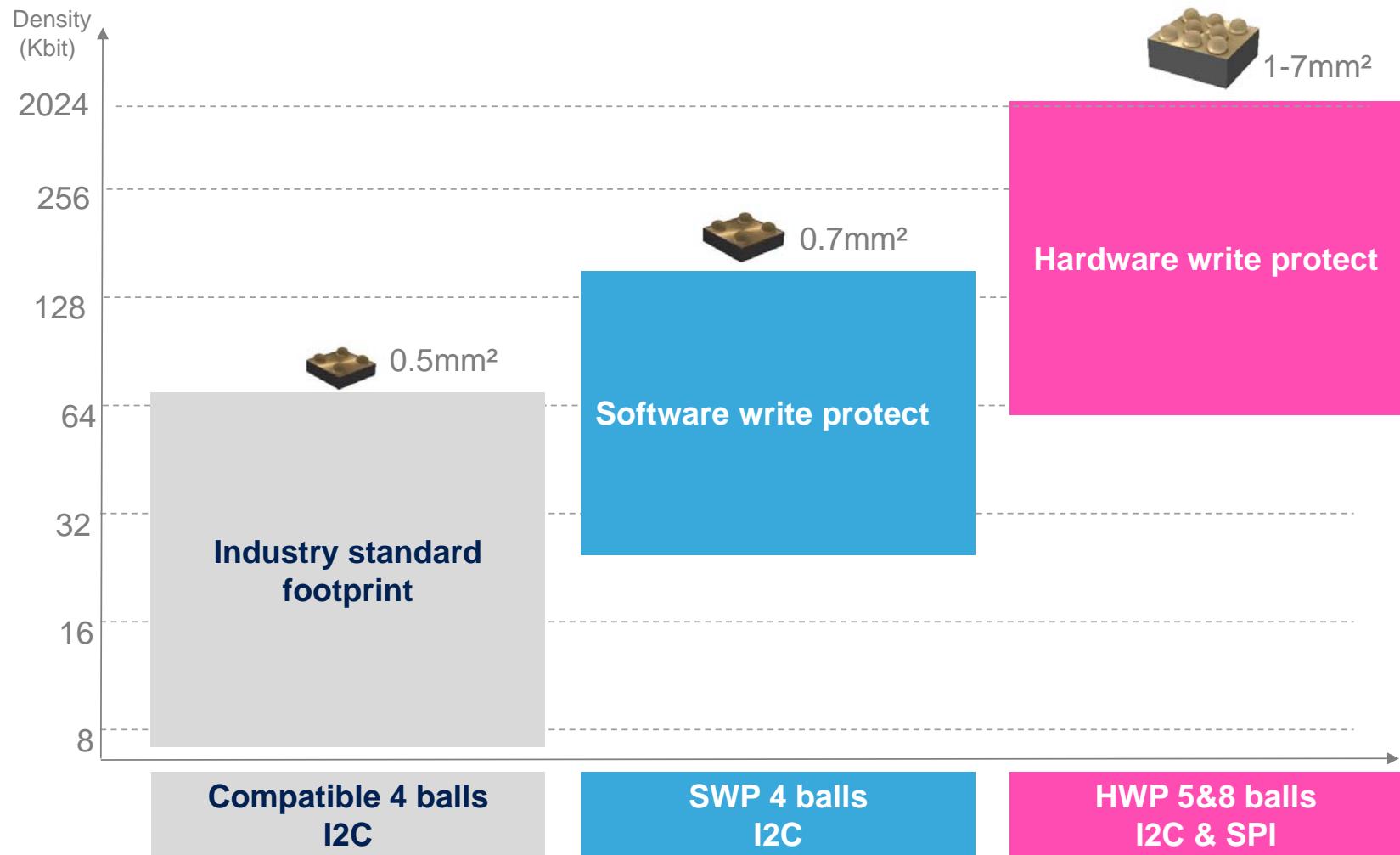
July 2016



\*WLCSP : Wafer Level Chip Scale Package

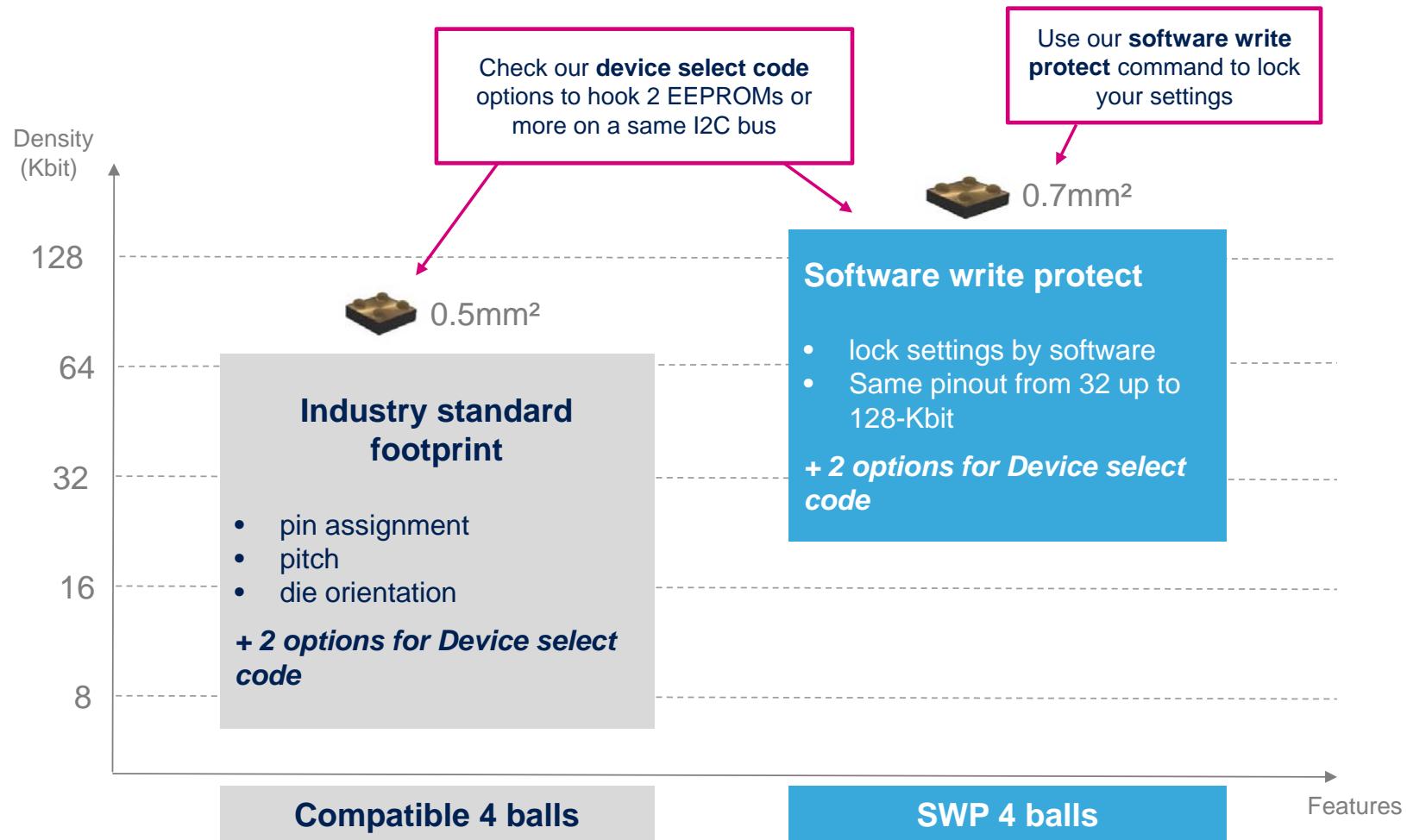
# Full WLCSP portfolio

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# 4 balls WLCSP portfolio

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# Software Write Protect feature

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- Designer's requirements
  - Lock partially or completely the memory array, even if device has no hardware write protect pin (4 balls design)
- ST's solution
  - ST developed a software write protect feature which allows customer to protect the whole/defined blocks of the EEPROM by software, against undesirable write instruction
  - Software write protect requires no design change, only software update
- Flexible configuration of protected area
  - the whole memory array
  - the upper 3/4 memory array
  - the upper half memory array
  - the upper quarter memory array

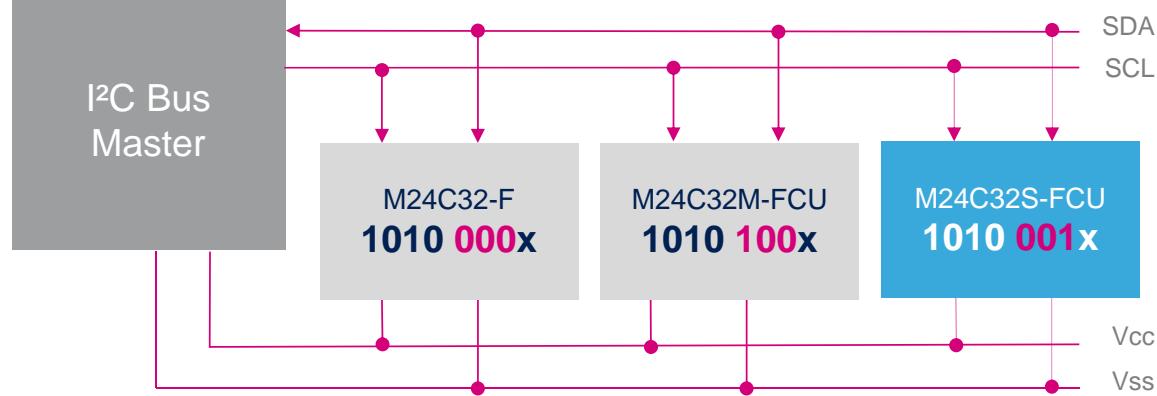
	Whole memory (b2,b1=1,1)
	Upper ¾ (b2,b1=1,0)
	Upper Half (b2,b1=0,1)
	Upper ¼ (b2,b1=0,0)
	Protect Register



# Device select code option

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- Designer's requirements
  - Hook several EEPROM on the same I<sup>2</sup>C bus, even if device has no chip select pin (4 balls design)
- ST's solution
  - ST designed chips with different “device select code” to identify 2 EEPROMs or more on the same bus:
    - 1010 001x
    - 1010 000x
    - 1010 100x
- Example :



# Compatibility Matrix of WLCSP 4-Ball EEPROM

Use different options to hook on the same I<sup>2</sup>C bus 2 EEPROMs or more (4 balls)

Density		8-Kbit	32-Kbit				64-Kbit				128-Kbit		Device select code
	RPN	M24C08-F	M24C32-F	M24C32M-FCU	M24C32S-FCU	M24C32T-FCU	M24C64-F	M24C64M-FCU	M24C64S-FCU	M24C64T-FCU	M24128S-FCU	M24128T-FCU	
<b>8-Kbit*</b>	M24C08-F			Y				Y					1010 0zzx
<b>32-Kbit</b>	M24C32-F			Y	Y			Y	Y			Y	1010 000x
	M24C32M-FCU	Y	Y		Y	Y	Y		Y	Y	Y	Y	1010 100x
	M24C32S-FCU		Y	Y		Y	Y	Y		Y		Y	1010 001x
	M24C32T-FCU			Y	Y			Y	Y		Y		1010 000x
<b>64-Kbit</b>	M24C64-F			Y	Y			Y	Y			Y	1010 000x
	M24C64M-FCU	Y	Y		Y	Y	Y		Y	Y	Y	Y	1010 100x
	M24C64S-FCU		Y	Y		Y	Y		Y			Y	1010 001x
	M24C64T-FCU			Y	Y			Y	Y		Y		1010 000x
<b>128-Kbit</b>	M24128S-FCU		Y	Y		Y	Y	Y		Y		Y	1010 001x
	M24128T-FCU			Y	Y			Y	Y		Y		1010 000x

Notes:

- M24C16-DFCU6TP can't share the same I<sup>2</sup>C bus with other EEPROM.
- \*8-Kbit needs only 1 address byte

# WLCSP Portfolio with 4 balls

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WLCSP	Part number	Memory density	Software Write Protect	Dimension (max X/Y) (mm)		Profile (max) (mm)	Ball size (typ) (mm)	Pinout compatibility	Min Pitch (mm)	Back side coating	Device select code
<b>I2C bus</b>											
SWP 4 balls	M24C32S-FCU6T/T	32-Kbit	Yes	0.871	0.871	0.300	0.185	M24C64S	0.4 x 0.5	No	1010 001x
	M24C32S-FCU6T/TF	32-Kbit	Yes	0.871	0.871	0.330	0.185	M24C64S	0.4 x 0.5	Yes	1010 001x
	M24C64S-FCU6T/T	64-Kbit	Yes	0.871	0.871	0.300	0.185	M24128S	0.4 x 0.5	No	1010 001x
	M24C64S-FCU6T/TF	64-Kbit	Yes	0.871	0.871	0.330	0.185	M24128S	0.4 x 0.5	Yes	1010 001x
	M24128S-FCU6T/T	128-Kbit	Yes	0.871	0.871	0.300	0.185	M24C64S	0.4 x 0.5	No	1010 001x
	M24128S-FCU6T/TF	128-Kbit	Yes	0.871	0.871	0.330	0.185	M24C64S	0.4 x 0.5	Yes	1010 001x
	M24C32T-FCU6T/TF	32-Kbit	Yes	0.871	0.871	0.330	0.185	M24C64T	0.4 x 0.5	Yes	1010 000x
	M24C64T-FCU6T/TF	64-Kbit	Yes	0.871	0.871	0.330	0.185	M24128T	0.4 x 0.5	Yes	1010 000x
	M24128T-FCU6T/TF	128-Kbit	Yes	0.871	0.871	0.330	0.185	M24C64T	0.4 x 0.5	Yes	1010 000x
Compatible 4 balls	M24C08-FCT6TP/T	8-Kbit	No	0.715	0.705	0.330	0.185	M24C16	0.4 x 0.4	No	1010 0zzx
	M24C16-DFCU6TP/K	16-Kbit	No	0.745	0.839	0.300	0.185	M24C08	0.4 x 0.4	No	N/A
	M24C32-FCU6TP/TF	32-Kbit	No	0.815	0.694	0.345	0.160	M24C64-FCU	0.4 x 0.4	Yes	1010 000x
	M24C32M-FCU6T/TF	32-Kbit	No	0.815	0.694	0.345	0.160	M24C64M-FCU	0.4 x 0.4	Yes	1010 100x
	M24C64-FCU6TP/TF	64-Kbit	No	0.815	0.694	0.345	0.160	M24C32-FCU	0.4 x 0.4	Yes	1010 000x
	M24C64M-FCU6T/TF	64-Kbit	No	0.815	0.694	0.345	0.160	M24C32M-FCU	0.4 x 0.4	Yes	1010 100x

# WLCSP Portfolio with Hardware Write Protect

All devices are embedding Hardware Write Protect and are in mass production

WLCSP	Part number	Memory density	Dimension (max X/Y) (mm)		Profile (max) (mm)	Ball size (typ) (mm)	Pinout compatibility	Bump number
HWP 5&8 balls	<b>I2C bus</b>							
	M24C64-FCS6TP/K	64-Kbit	1.168	1.074	0.645	0.27	-	5
	M24C64-DFCT6TP/K	64-Kbit	1.093	0.979	0.33	0.16	-	8
	M24128-DFCS6TP/K	128-Kbit	1.291	1.101	0.580	0.27	M24256	8
	M24256-DFCS6TP/K	256-Kbit	1.291	1.378	0.580	0.27	M24128	8
	M24512-DFCS6TP/K	512-Kbit	1.291	1.957	0.580	0.27	M24M01	8
	M24M01-DFCS6TP/K	1-Mbit	1.736	2.598	0.580	0.27	M24512	8
	M24M02-DRCS6TP/K	2-Mbit	2.031	3.576	0.580	0.27	-	8
	<b>SPI bus</b>							
	M95640-DFCT6TP/K	64-Kbit	1.093	0.979	0.330	0.16	-	8
	M95128-DFCS6TP/K	128-Kbit	1.291	1.101	0.580	0.27	M95256	8
	M95256-DFCS6TP/K	256-Kbit	1.291	1.378	0.580	0.27	M95128	8
	M95512-DFCS6TP/K	512-Kbit	1.291	1.957	0.580	0.27	M95M01	8
	M95M01-DFCS6TP/K	1-Mbit	1.736	2.598	0.580	0.27	M95512	8
	M95M02-DRCS6TP/K	2-Mbit	2.031	3.576	0.580	0.27	-	8

Thank you!

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