Two-Stage Hysteretic LED Driver Controller

General Description

The RT8476 is a two-stage controller with dual gate drivers consist of a Boost converter (first stage) and a Buck converter (second stage). The advantage of the two-stage topology is highly compatible with ET (Electronic Transformer) in MR16 / AR111 lighting market field applications.

The first stage is a Boost converter for constant voltage output with inductor peak current over current protection. The second stage is a Buck converter for constant output current by typical constant peak current regulation.

The RT8476 is equipped with dual output gate drivers for external power MOSFETs, suitable for higher power applications.

The RT8476 is available in the SOP-8 and SOP-8 (Exposed pad) packages.

Applications

- MR16 Lighting
- Signage and Decorative LED Lighting
- Architectural Lighting
- High Power LED Lighting
- Low Voltage Industrial Lighting
- Indicator and Emergency Lighting
- Automotive LED Lighting

Features

- **Two-Stage Topology (Boost + Buck)**
- **Wide Input Voltage Range : 4.5V to 40V**
- **Adjustable Peak Input Current Control**
- **Adjustable Boost Output Voltage**
- **Independent Dual Stage Function**
- **Adjustable LED Current with ±5% LED Current Accuracy**
- **Input Under Voltage Lockout Detection**
- **Thermal Shutdown Protection**
- **SOP-8 and SOP-8 (Exposed Pad) Packages**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8476 □□

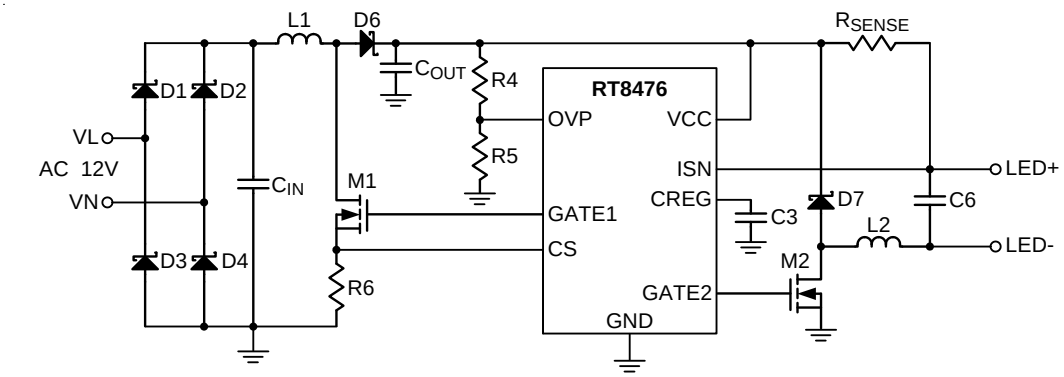
- Package Type
  - S : SOP-8
  - SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



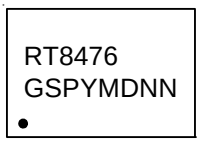
Marking Information

RT8476GS

RT8476GS : Product Number

YMDNN : Date Code

RT8476GSP

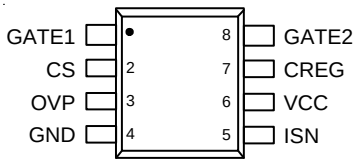


RT8476GSP : Product Number

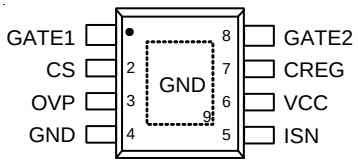
YMDNN : Date Code

Pin Configurations

(TOP VIEW)



SOP-8

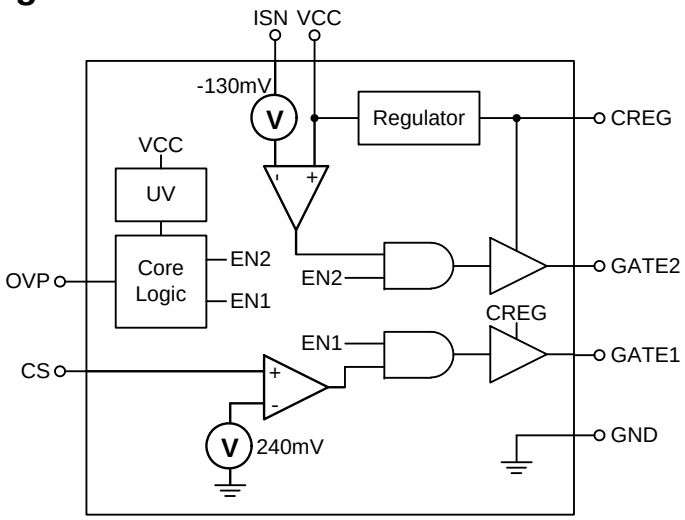


SOP-8 (Exposed Pad)

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8	SOP-8 (Exposed Pad)		
1	1	GATE1	Gate Driver Output for External MOSFET Switch in the First Stage.
2	2	CS	Current Sense Input for External MOSFET Switch.
3	3	OVP	Over Voltage Protection Sense Input.
4	4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	5	ISN	LED Current Sense Amplifier Negative Input.
6	6	VCC	Supply Voltage Input. For good bypass, place a ceramic capacitor near the VCC pin.
7	7	CREG	Internal Regulator Output. Place an 1μF capacitor between the CREG and GND pins.
8	8	GATE2	Gate Driver Output for External MOSFET Switch in the Second Stage.

Function Block Diagram



Operation

The VCC of the RT8476 is supplied from the first stage Boost output. The first stage is a constant output voltage Boost topology. The CS pin senses the peak inductor current for over current protection. The peak inductor current level can be adjusted by the sense resistor between MOSFET Source and GND pins.

The second stage is a constant output current Buck topology. The current sense voltage threshold between the VCC and ISN pins is only 130mV to reduce power loss.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VCC to GND ---------- –0.3V to 45V
- CS, GATE1, GATE2, CREG, OVP to GND ---------- –0.3V to 6V
- VCC to ISN ---------- –1V to 3V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.53W
  - SOP-8 (Exposed Pad) ---------- 3.44W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 188°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 29°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC ---------- 4.5V to 40V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 10V, No Load, C_{LOAD} = 1nF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
CREG UVLO_ ON	V_{UVOL_ON}	CS/OVP = 0V	4	4.3	4.6	V
CREG UVLO_ OFF	V_{UVOL_OFF}	CS/OVP = 0V	--	4.2	--	V
Supply Current						
VCC Shutdown Current	I_{SHDN}	Before Start-Up, V_{CC} = 3.5V	--	10	--	μA
VCC Quiescent Current	I_Q	After Start-Up, V_{CC} = 5V, GATE1 and GATE2 Stand Still	--	1.5	--	mA
Internal Reference Voltage	V_{CREG}		--	5	--	V
Internal Reference Voltage		I_{CREG} = 20mA	--	4.9	--	V
Current Sense Comparator						
CS Threshold Voltage	V_{CS}		215	240	265	mV
CS Pin Leakage Current	I_{CS}		--	1	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Threshold						
OVP High Level	V_{OVP_H}		1.71	1.9	2.09	V
OVP Low Level	V_{OVP_L}		1.44	1.6	1.76	V
OVP Pin Leakage Current	I_{OVP}		--	1	--	μA
Gate Driver						
GATE1 Duty Off-Time			--	1.5	--	μs
UGATE1 Drive Sink	$R_{UGATE1sk}$	Sink = 50mA	--	2	--	Ω
LGATE1 Drive Source	$R_{LGATE1sr}$	Source = −50mA	--	1.25	--	Ω
GATE1 Default Pull Down Resistor			--	90	--	kΩ
Buck Converter						
ISN Threshold	V_{ISN}		123.5	130	136.5	mV
ISN Hysteresis	ΔV_{ISN}		10	15	20	%
ISN Pin Leakage Current	I_{ISN}		--	1	--	μA
UGATE2 Drive Sink	$R_{UGATE2sk}$	Sink = 50mA	--	2	--	Ω
LGATE2 Drive Source	$R_{LGATE2sr}$	Source = −50mA	--	1.25	--	Ω
GATE2 Default Pull Down Resistor			--	90	--	kΩ
Temperature Protection						
Thermal Shutdown Temperature	T_{SD}		140	155	170	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	35	--	°C

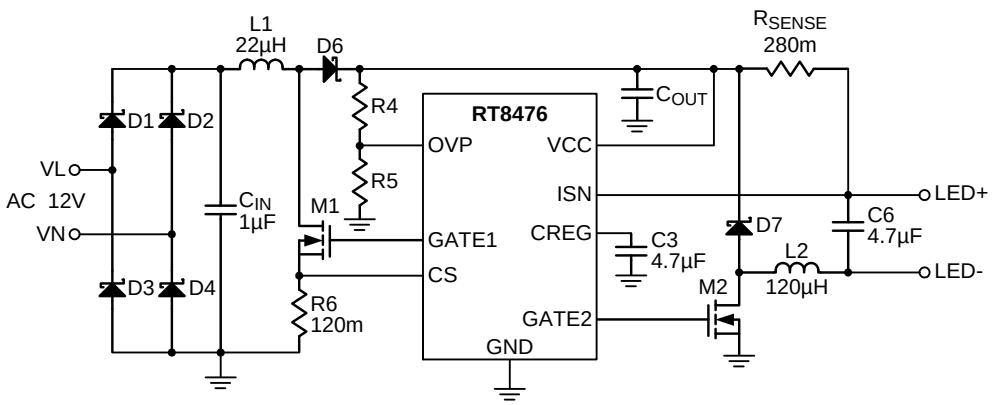
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

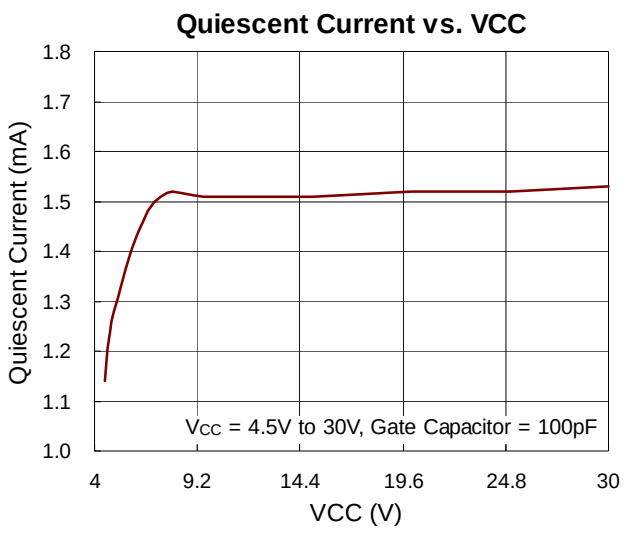
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

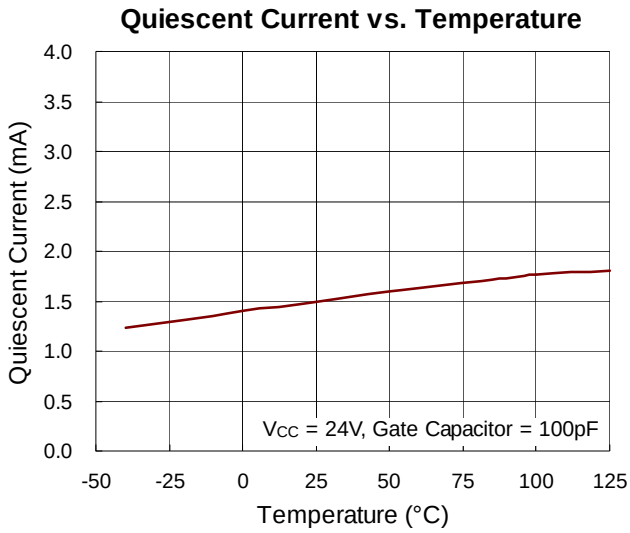
Note 4. The device is not guaranteed to function outside its operating conditions.

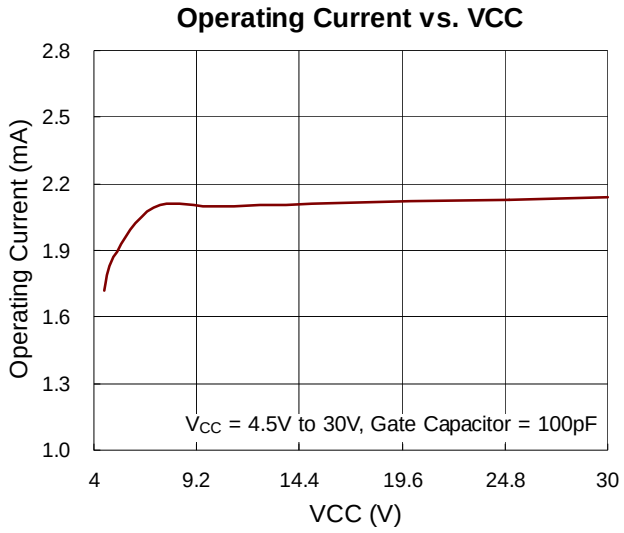
Typical Application Circuit

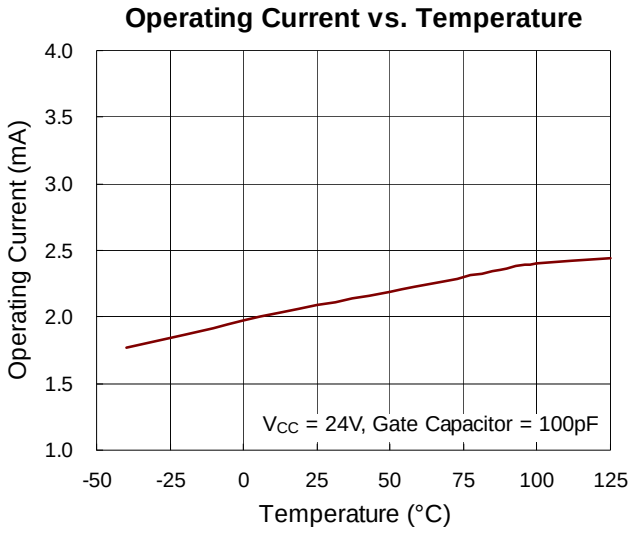


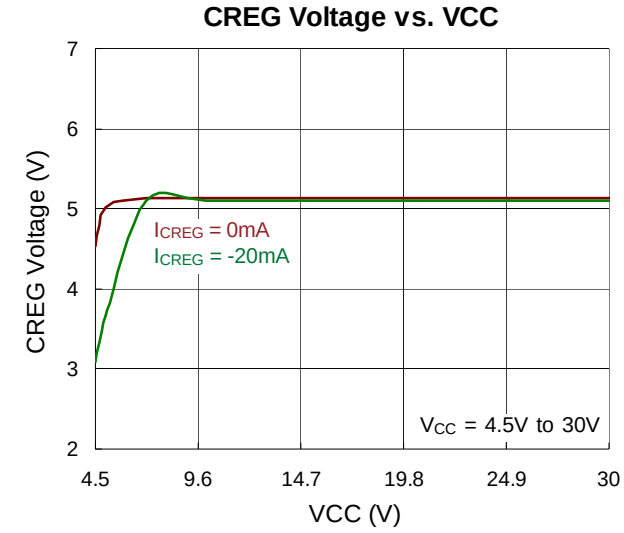
Typical Operating Characteristics

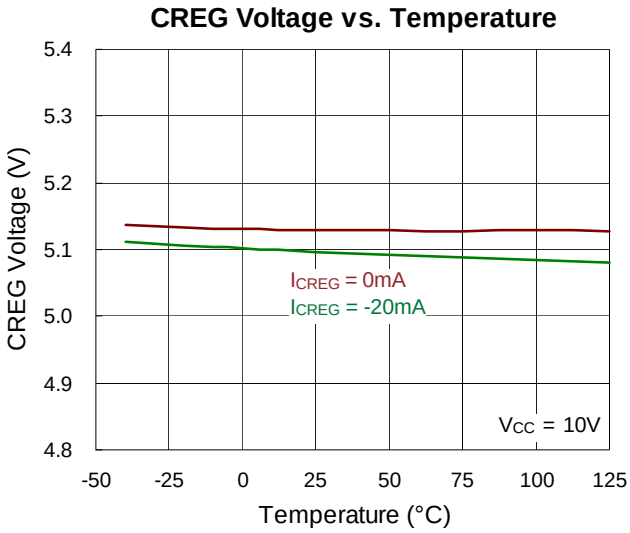




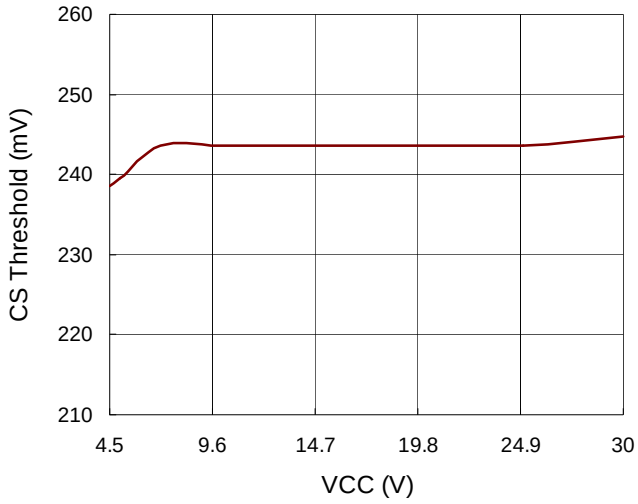




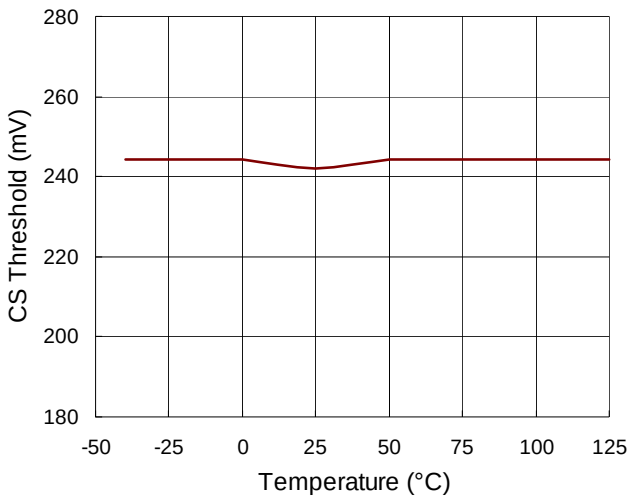




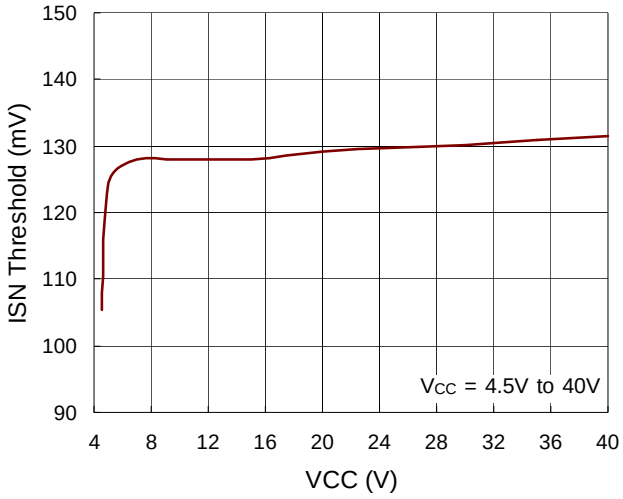
CS Threshold vs. VCC



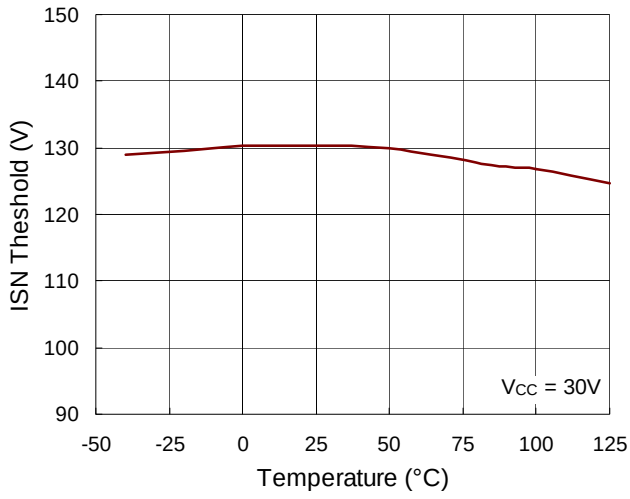
CS Threshold vs. Temperature



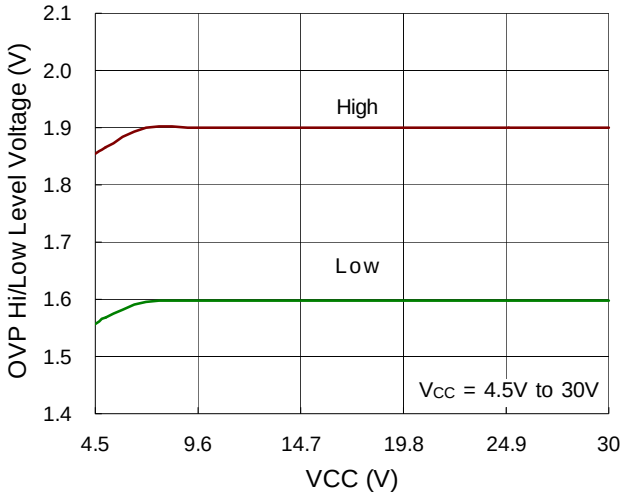
ISN Threshold vs. VCC



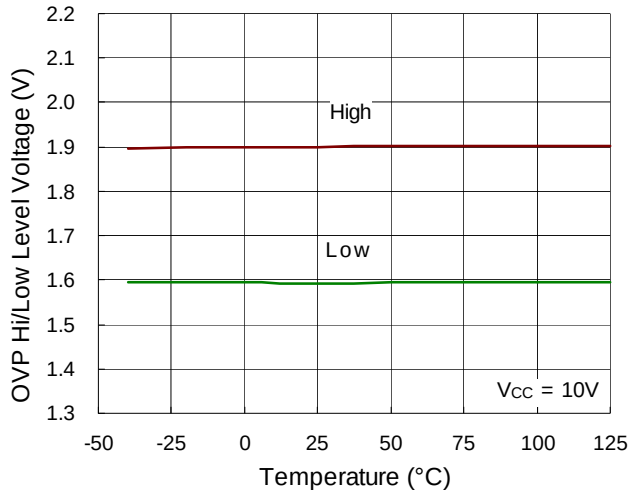
ISN Threshold vs. Temperature



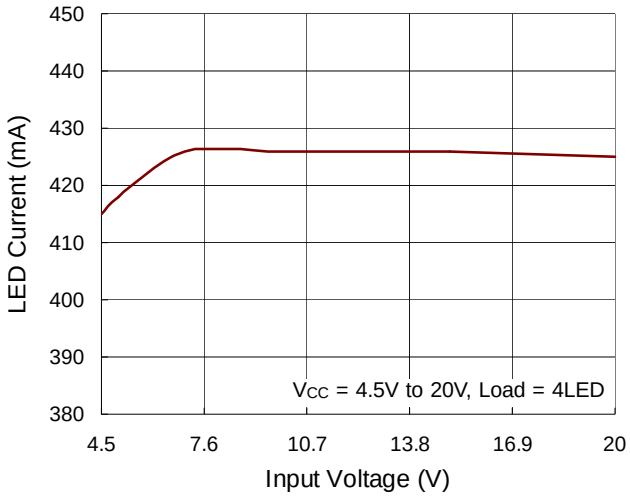
OVP Hi/Low Level Voltage vs. VCC



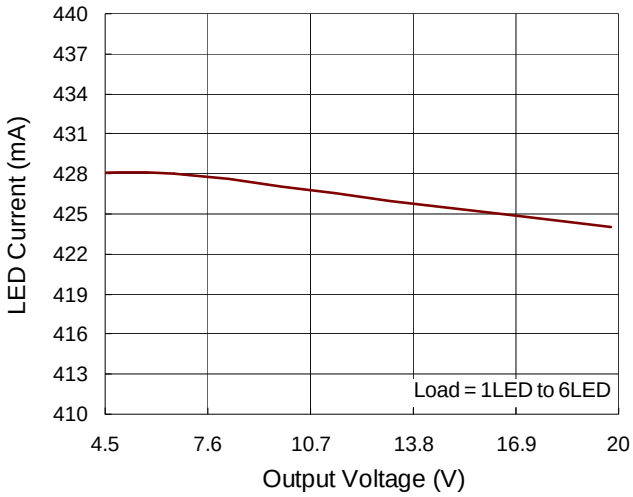
OVP Hi/Low Level Voltage vs. Temperature



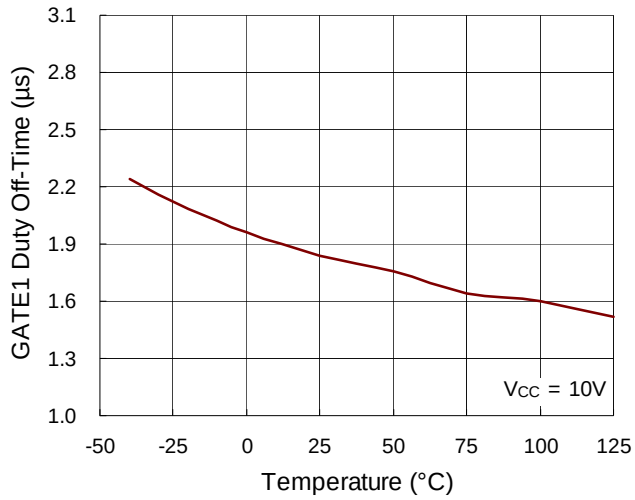
LED Current vs. Input Voltage



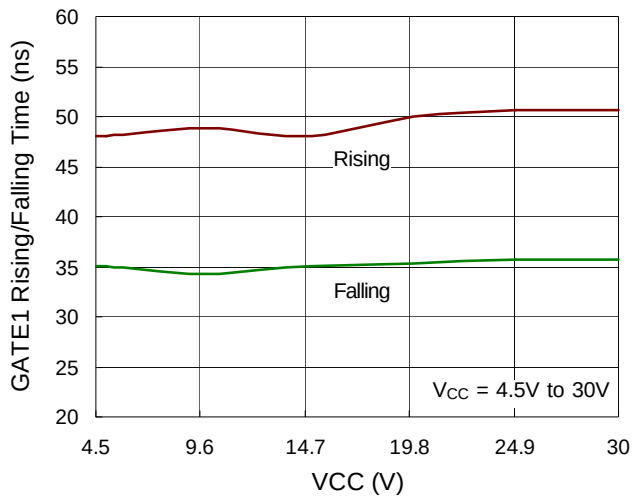
LED Current vs. Output Voltage



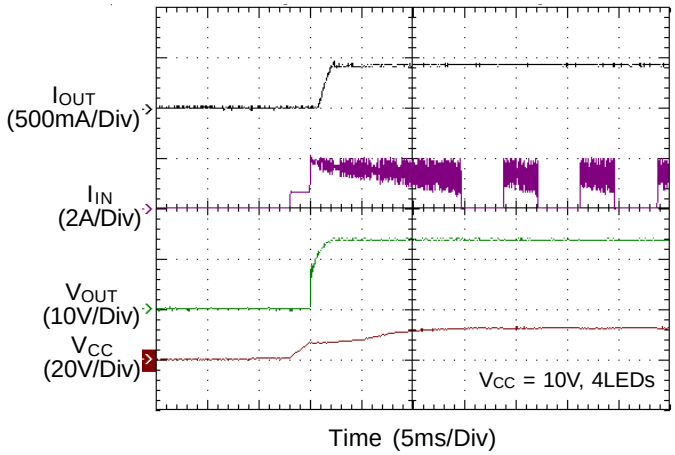
GATE1 Duty Off-Time vs. Temperature



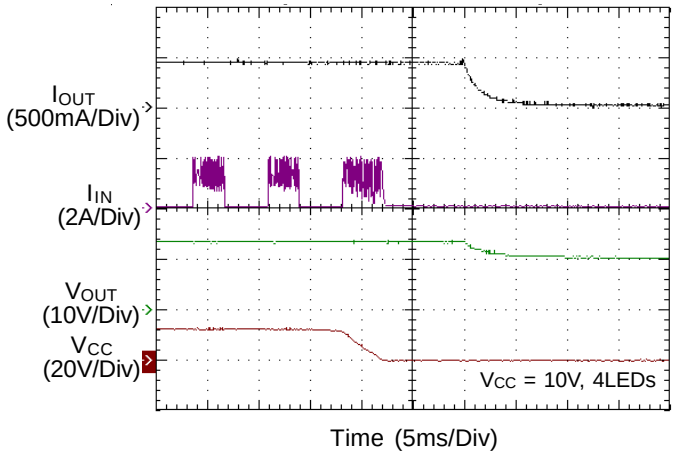
GATE1 Rising/Falling Time vs. VCC



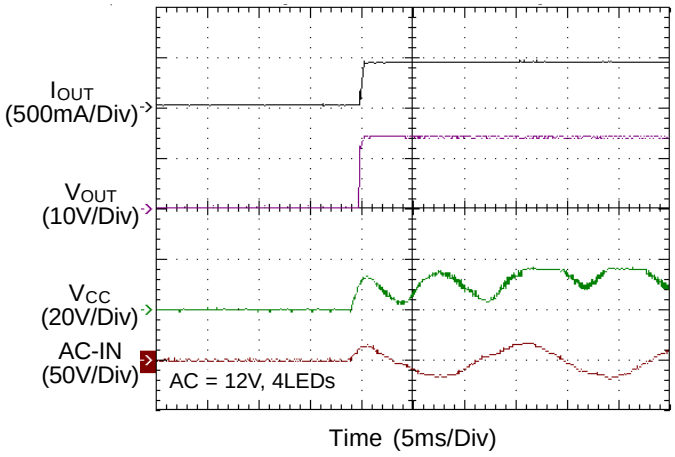
Power On From VCC



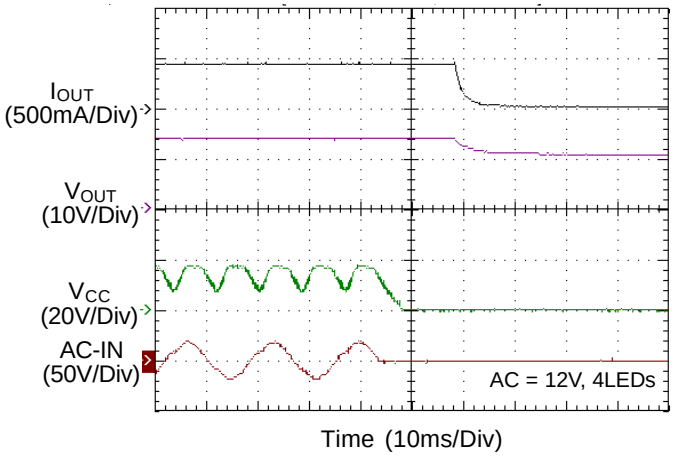
Power Off From VCC



Power On From AC-IN



Power Off From AC-IN



Application Information

The RT8476 consists of a constant output current Buck controller and a fixed off-time controlled Boost controller. The Boost controller is based on a peak current, fixed off-time control architecture and designed to operate up to 800kHz to use a very small inductor for space constrained applications. A high side current sense resistor is used to set the output current of the Buck controller. A 1% sense resistor performs a ±5% LED current accuracy for the best performance.

Under Voltage Lockout (UVLO)

The RT8476 includes an under voltage lookout function with 100mV hysteresis. The internal MOSFET turns off when VCC falls below 4.2V (typ.).

CREG Regulator

The CREG pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R, ceramic capacitor for best performance. A 4.7μF capacitor will be adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the CREG pin and to the IC ground. An internal current limit on the CREG output protects the RT8476 from excessive on-chip power dissipation.

The CREG pin has set the output to 4.3V (typ.) to protect the external FETs from excessive power dissipation caused by not being fully enhanced. If the CREG pin is used to drive extra circuits beside RT8476, the extra loads should be limited to less than 10mA.

Gate Driver

There are two gate drivers, GATE1 and GATE2, in the RT8476. The Gate driver consists of a CMOS buffer designed to drive the external power MOSFET. It features unbalanced source and sink capabilities to optimize switch on and off performance without additional external components. Whenever the IC supply voltage is lower than the under voltage threshold, the Gate Driver is pulled low.

Average Output Current Setting

The output current that flows through the LED string is set by an external resistor, R_{SENSE}, which is connected between the VCC and ISN terminal. The relationship between output current, I_{OUT}, and R_{SENSE} is shown below :

$$I_{OUT} = \frac{130mV}{R_{SENSE}}$$

LED Current Ripple Reduction

Higher LED current ripple will shorten the LED life time and increase heat accumulation of LED. To reduce the LED current ripple, an output capacitor in parallel with the LED should be added. The typical value of output capacitor is 4.7μF.

VCC Voltage Setting

The VCC voltage setting is equipped with an Over Voltage Protection (OVP) function. When the voltage at the OVP pin exceeds threshold approximately 1.9V, the power switch is turned off. The power switch can be turned on again once the voltage at the OVP pin drops below 1.6V. For Boost applications, the output voltage can be set by the following equation :

$$V_{CC(MAX)} = 1.9 \times (1 + R4 / R5)$$

R4 and R5 are the voltage divider resistors from VOUT to GND with the divider center node connected to the OVP pin. For MR16 LED lamp application, the minimum voltage of V_{CC} should maintain above 25V for stable operation.

Step-Down Converter Inductor Selection

The RT8476 implemented a simple high efficiency, continuous mode inductive step-down converter. The inductance L2 in Buck converter is determined by the following factors : inductor ripple current, switching frequency, VOUT/VIN ratio, internal MOSFET, topology specifications, and component parameter. The inductance L2 is calculated according to the following equation :

$$L2 \geq [V_{CC(MAX)} - V_{OUT} - V_{ISN} - (R_{DS2(ON)} \times I_{OUT})] \times D / [f_{SW} \times \Delta I_{OUT}]$$

where

fsw is switching frequency (Hz).

$R_{DS2(ON)}$ is the low side switch on-resistance of external MOSFET (M2). The typical value is 0.35Ω.

D is the duty cycle = V_{OUT} / V_{IN}

I_{OUT} is the required LED current (A)

ΔI_{OUT} is the inductor peak-peak ripple current (internally set to 0.3 x I_{OUT})

V_{CC} is the supply input voltage (V)

V_{OUT} is the total LED forward voltage (V)

V_{ISN} is the voltage cross current sense resistor (V)

L2 is the inductance (H)

The selected inductor must have saturation current higher than the peak output LED current and continuous current rating above the required average output LED current. In general, the inductor saturation current should be 1.5 times the LED current. In order to minimize output current ripple, higher values of inductance are recommended at higher supply voltages. Because high values of inductance has high line resistance, it will cause lower efficiency.

Step-Up Converter Inductor Selection

The RT8476 uses a constant off-time control to provide high efficiency step-up converter. The resistor, R6, between the Source of the external N-MOSFET and GND should be selected to provide adequate switch maximum current to drive the application. The current limit threshold on the CS pin of the RT8476 is 240mV (typ.). When the CS pin voltage is higher than the 240mV reference, the comparator will disable the power section. The GATE1 will pull low after fixed delay time 1.5μs (typ.) and then turn on again after OVP operation is removed. This cycle repeats, keeping the output voltage within a small window. Following the constant off-time mechanism, the inductance L1 is calculated according to the following equation :

$L1 > t_{OFF} \times (V_{CC(MAX)} - V_{IN(MIN)} + V_F) / I_{LIM}$

where

t_{OFF} is Off-Time. The typical value is 1.5μs.

I_{LIM} is the input current. The typical value is 2A for MR16 application.

V_{CC} is the supply input voltage (V)

V_{IN} is the input voltage after bridge diodes (V)

V_F is the forward voltage (V)

L1 is the inductance (H)

$D = 1 - (V_{IN} / V_{OUT})$

$f_{SW} = (1 - D) / t_{OFF}$

where

D is the operation duty

f_{SW} is the switching frequency of Boost controller.

Check the I_{LIM} setting satisfied the output LED current request by the following equation :

$(I_{OUT} + \Delta I_{OUT}) < [2 \times L1 \times I_{LIM} + t_{OFF} \times (V_{IN} - V_{OUT} - V_F)] \times V_{IN} / [2 \times L1 \times (V_{CC})]$

Diode Selection

To obtain better efficiency, the Schottky diode is recommended for its low reverse leakage current, low recovery time and low forward voltage. With its low power dissipation, the Schottky diode outperforms other silicon diodes and increases overall efficiency.

Input Capacitor selection

Input capacitor has to supply peak current to the inductor and flatten the current ripple on the input. The low ESR condition is required to avoid increasing power loss. The ceramic capacitor is recommended due to its excellent high frequency characteristic and low ESR, which are suitable for the RT8476. For maximum stability over the entire operating temperature range, capacitors with better dielectric are suggested.

Thermal Protection

A thermal protection feature is to protect the RT8476 from excessive heat damage. When the junction temperature exceeds 150°C, the thermal protection will turn off the LX terminal. When the junction temperature drops below 125°C, the RT8476 will turn on the LX terminal and return to normal operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 188°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 29°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (188°C/W) = 0.53W for SOP-8 package

$P_{D(MAX)}$ = (125°C – 25°C) / (29°C/W) = 3.44W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

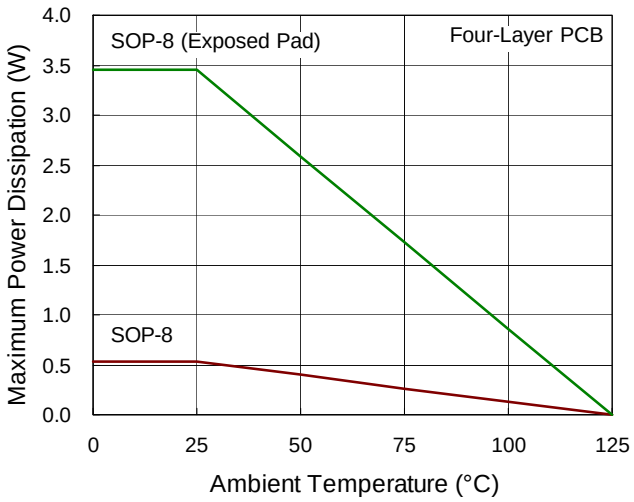


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important to design power switching converter circuits. Some recommended layout guidelines are suggested as follows :

- The power components L1, D6, M1, C_{IN}, and C_{OUT} must be placed as close to each other as possible to reduce the ac current loop area. The power components L2, D7, and M2 must be placed as close to each other as possible to reduce the ac current loop area. The PCB trace between power components must be as short and wide as possible due to large current flow through these traces during operation.
- The capacitor C_{OUT}, C6 and external resistor, R_{SENSE}, must be placed as close as possible to the VIN and SENSE pins of the device respectively.
- The GND should be connected to a strong ground plane.
- Keep the main current traces as short and wide as possible.

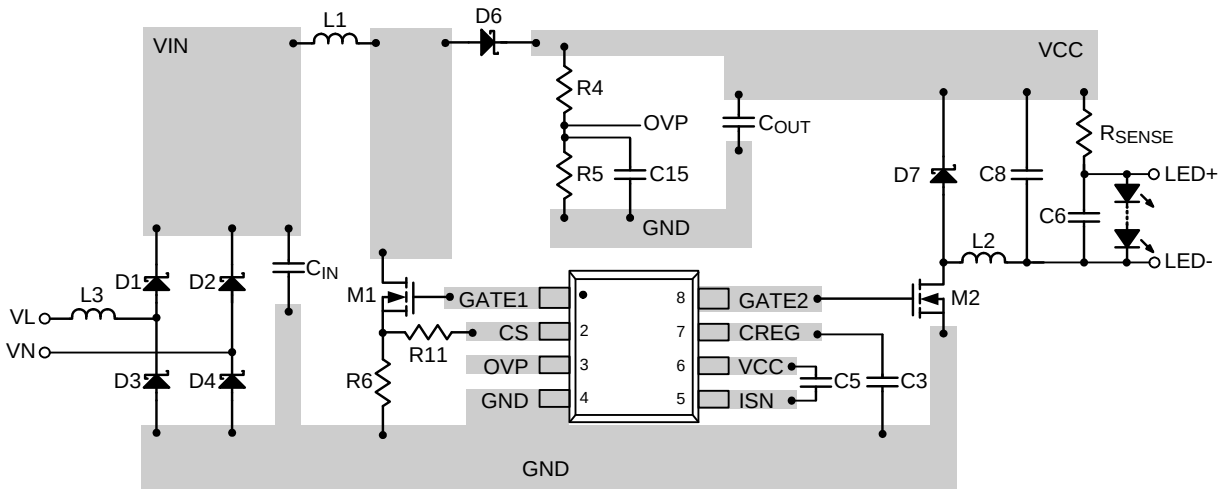
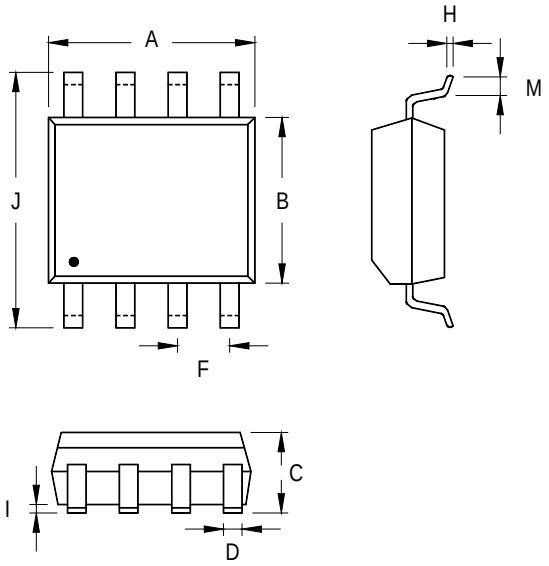


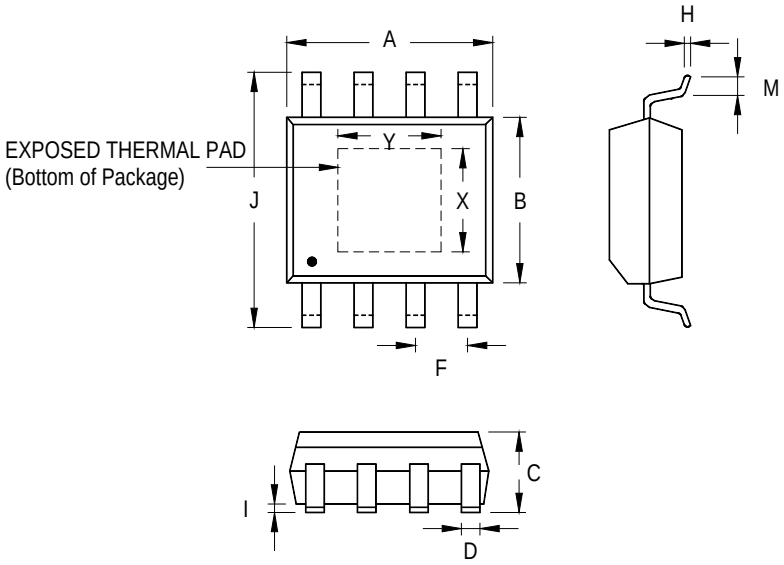
Figure 2. PCB Layout Guide for SOP-8 Package

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



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D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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