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S4E5B001B000A00 Epson EPD Controller Module

Command and Waveform Flash Programming

SEIKO EPSON CORPORATION

Rev. 1.0

NOTICE

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Chapter 1 Command and Waveform Flash Programming

This document describes how to program the command and waveform, that are matched with the panel to be driven by the Epson EPD Controller Module, into the flash memory on the module.

1.1 Overview

Different panels require a different command and waveform file. The waveform that matches with the panel being used may be provided by Epson, or customer if the panel is purchased directly from the panel manufacturer by customer. The command file will be generated by Epson according to the timing requirement from the specification of panel. Together with the matching waveform, a single binary file including both the commands and waveform will be generated.

Each Epson EPD Controller Module is pre-programmed with a factory default command and waveform file for used during the production testing of the module. Customers are required to re-program the flash memory with the matching command and waveform file for their panel.

The Epson instruction code is stored in the serial flash from address 0x0000 through 0x1089. The Waveform data must be stored in the serial flash from the starting address 0x108A. The command and waveform files may be appended together with any binary file editor (hex editor).

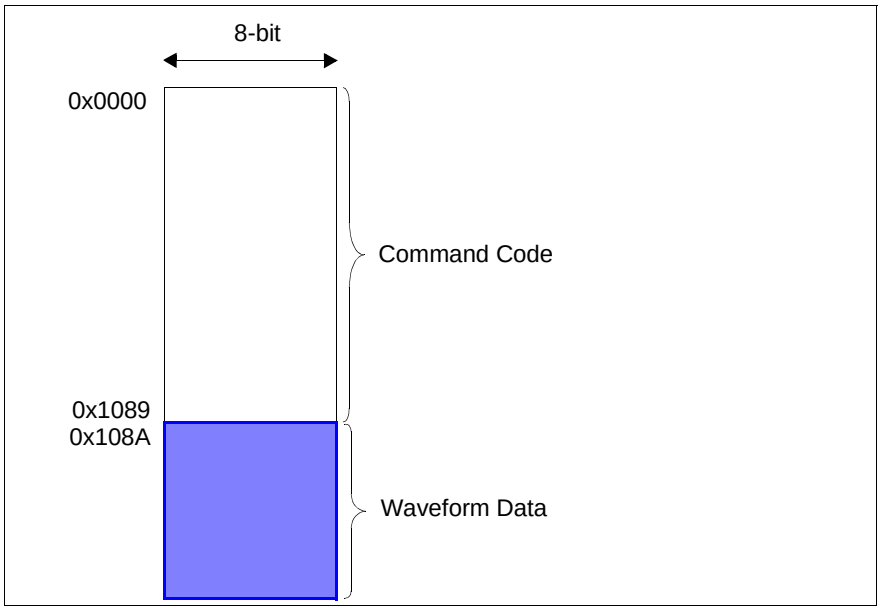

Figure 1-1: Command Code and Waveform Storage

1.2 Recommended Programming Flow

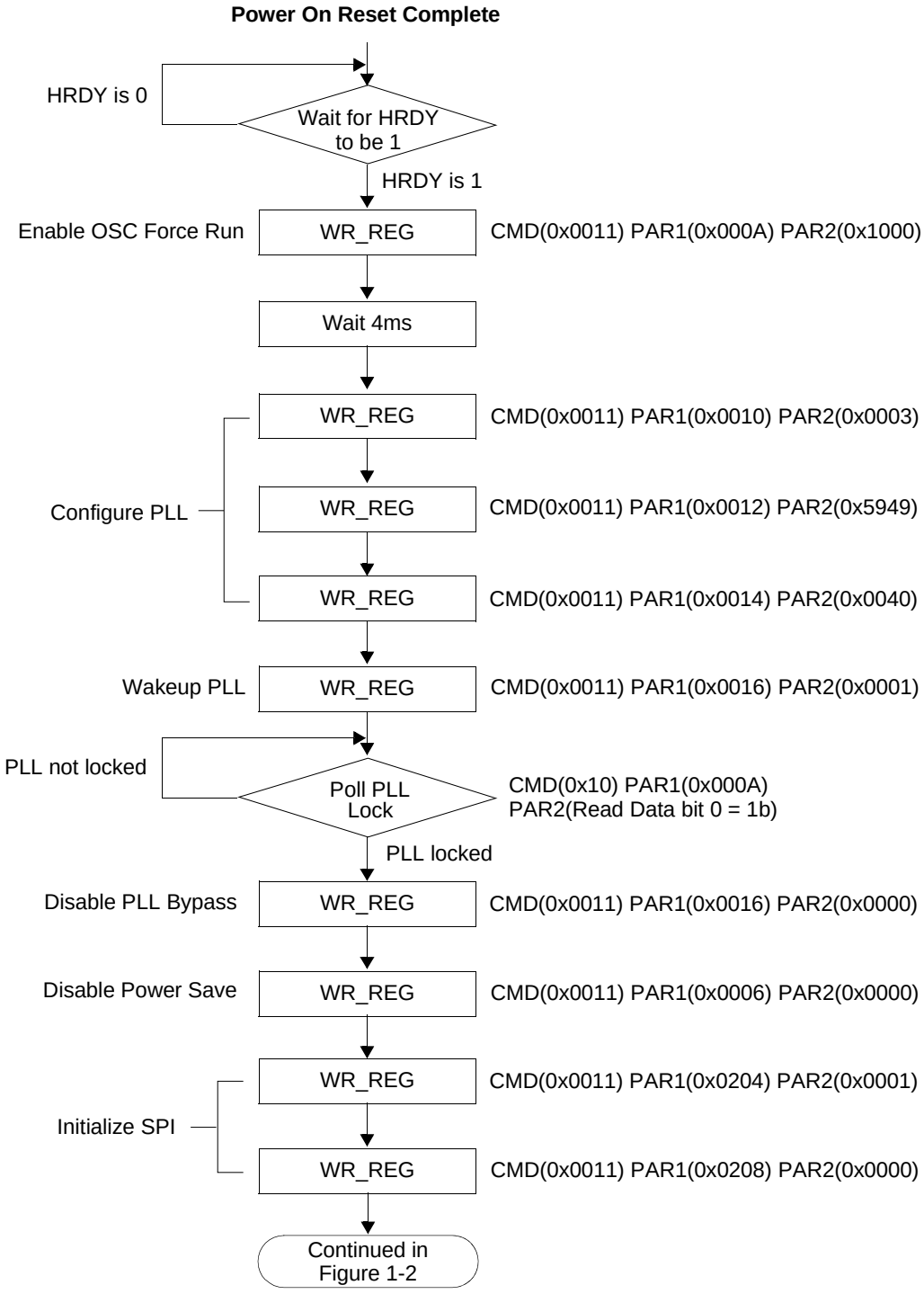

Figure 1-2: Command and Waveform Programming Flow (1 of 7)

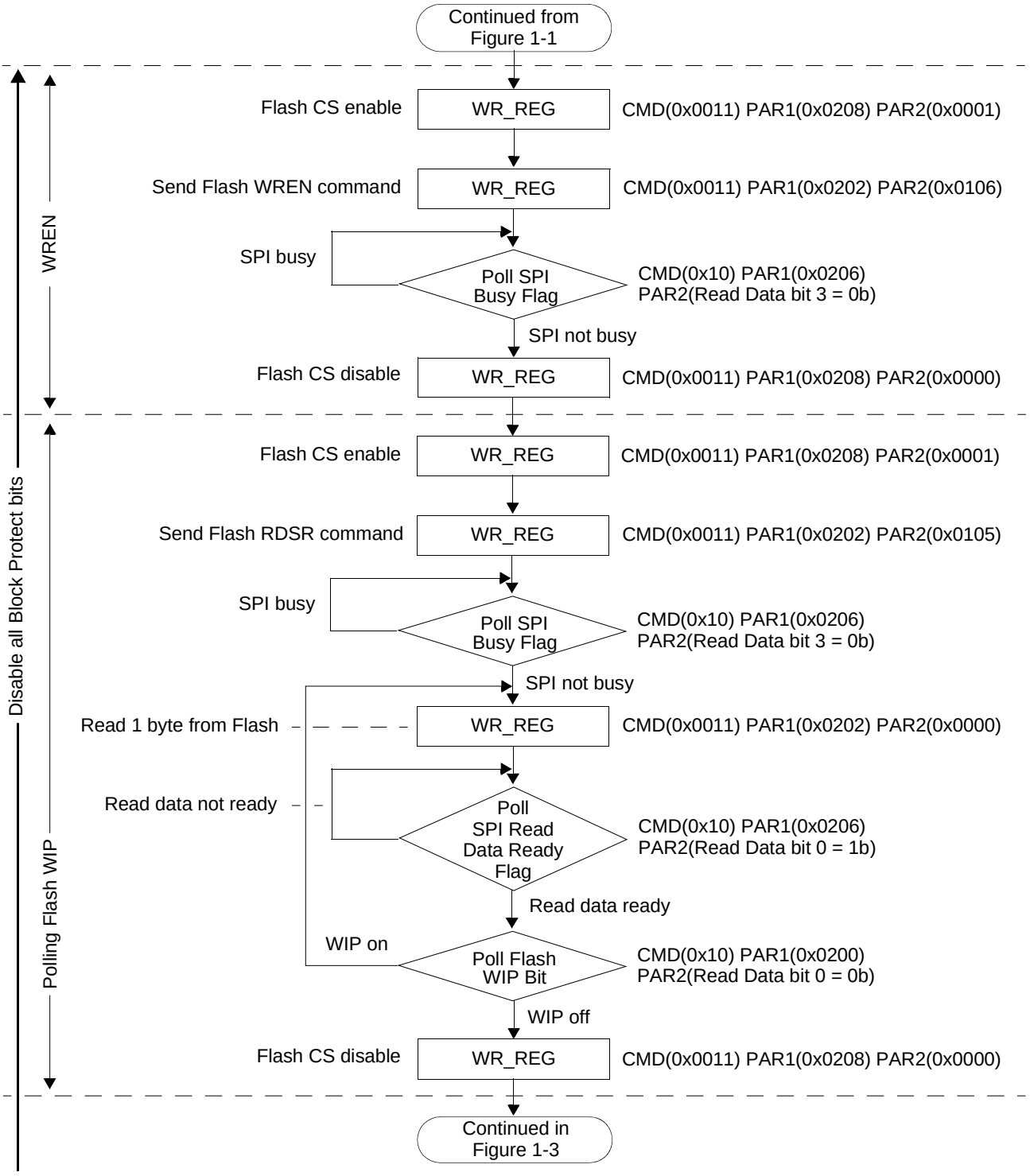

Figure 1-3: Command and Waveform Programming Flow (2 of 7)

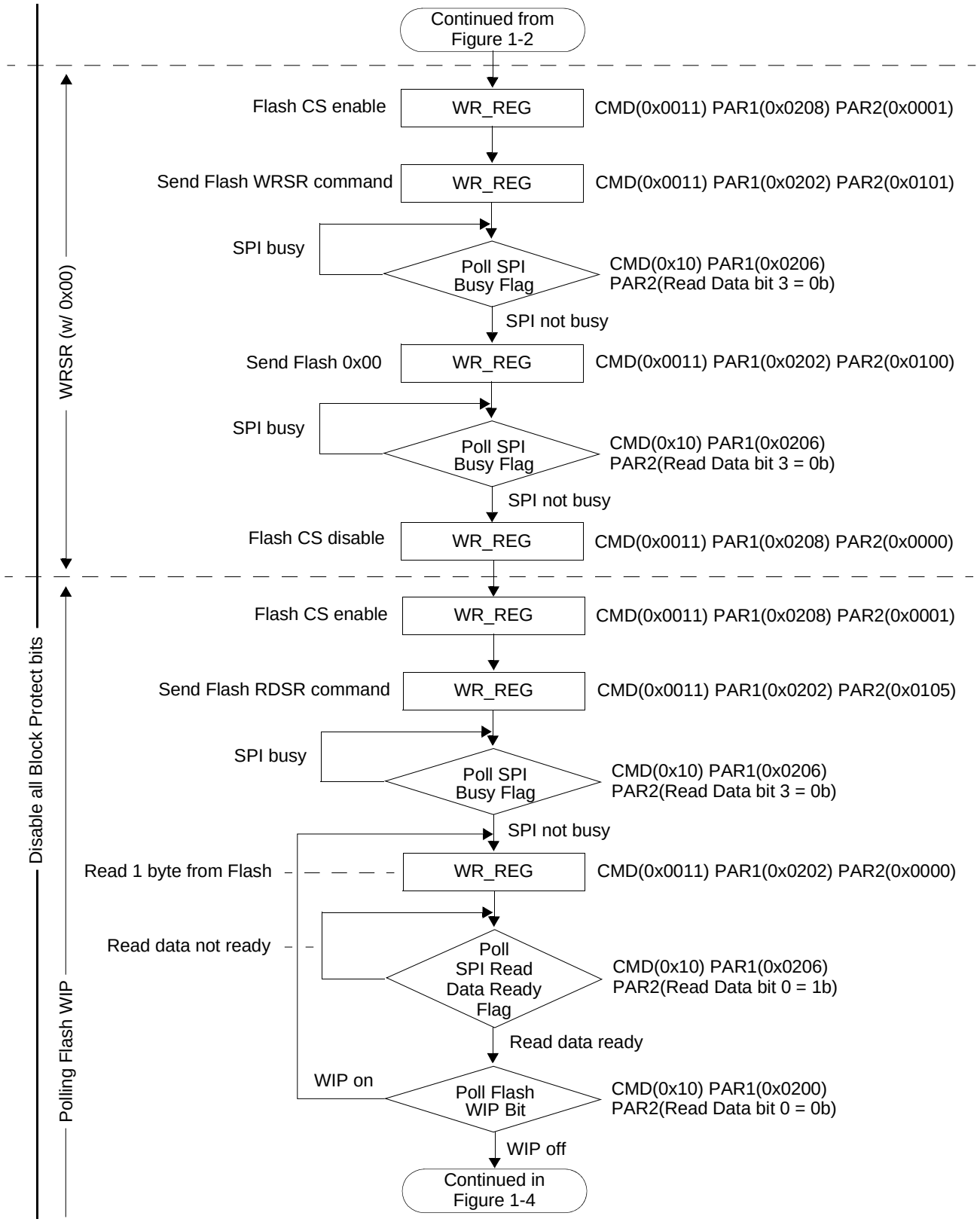

Figure 1-4: Command and Waveform Programming Flow (3 of 7)

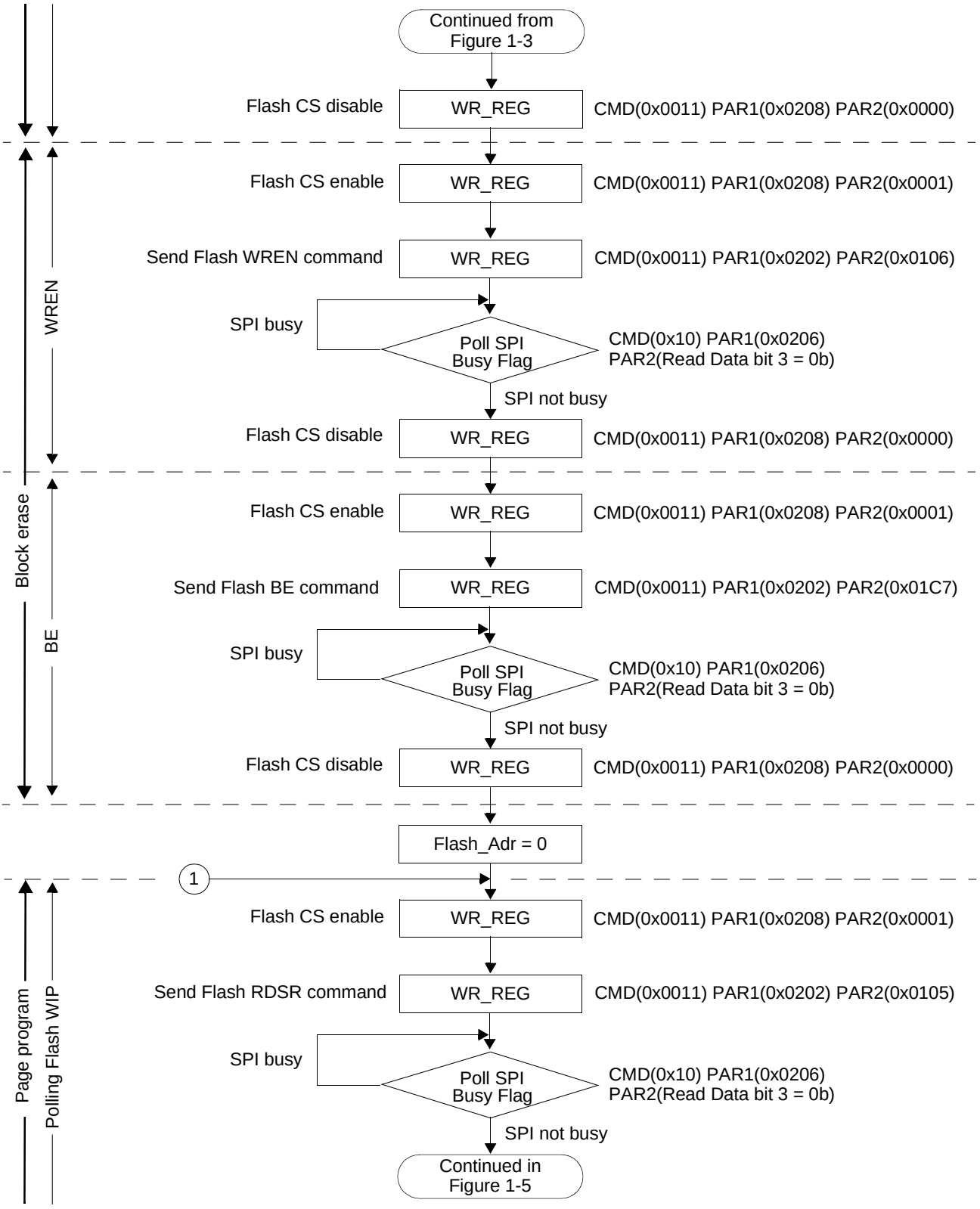

Figure 1-5: Command and Waveform Programming Flow (4 of 7)

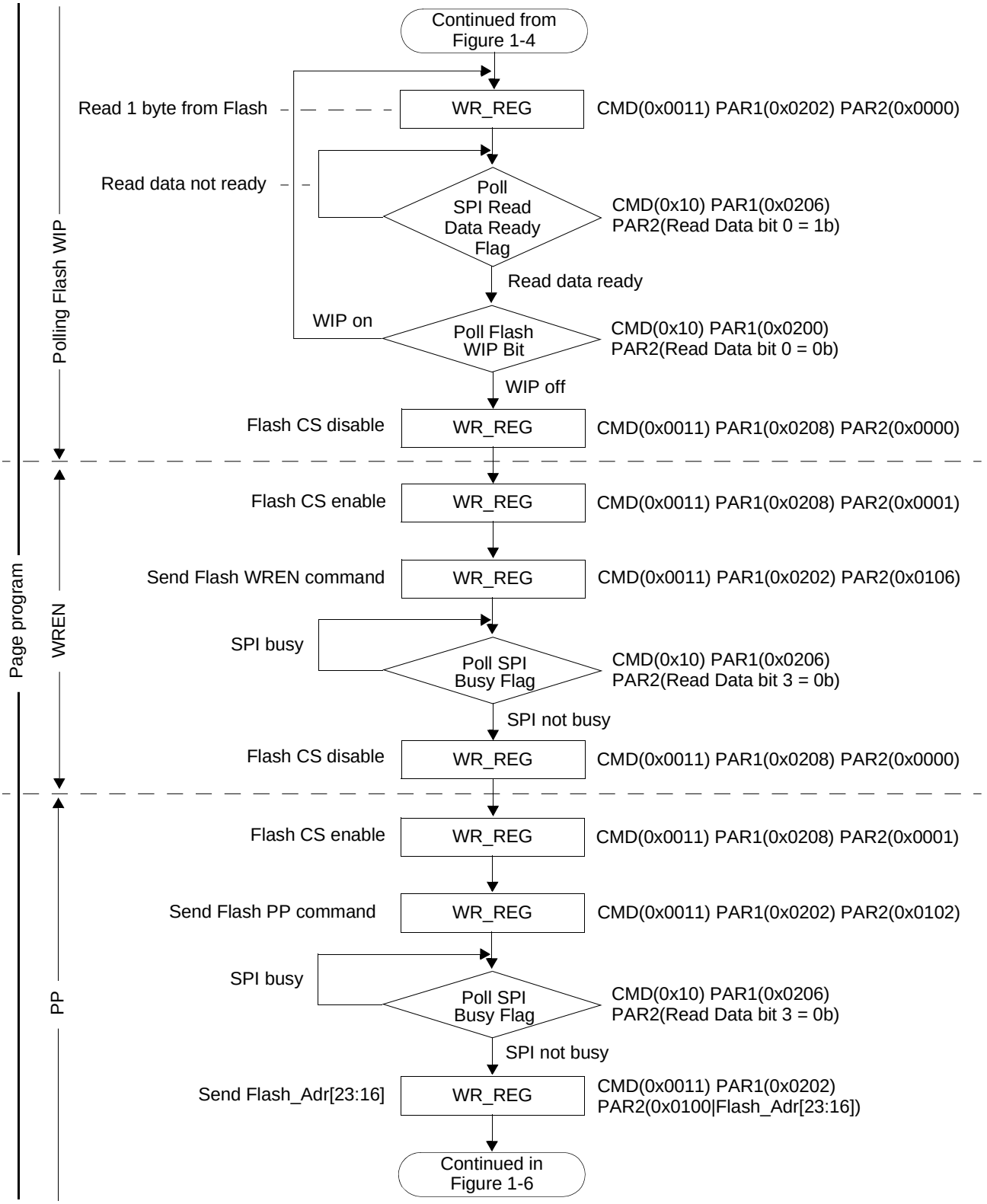

Figure 1-6: Command and Waveform Programming Flow (5 of 7)

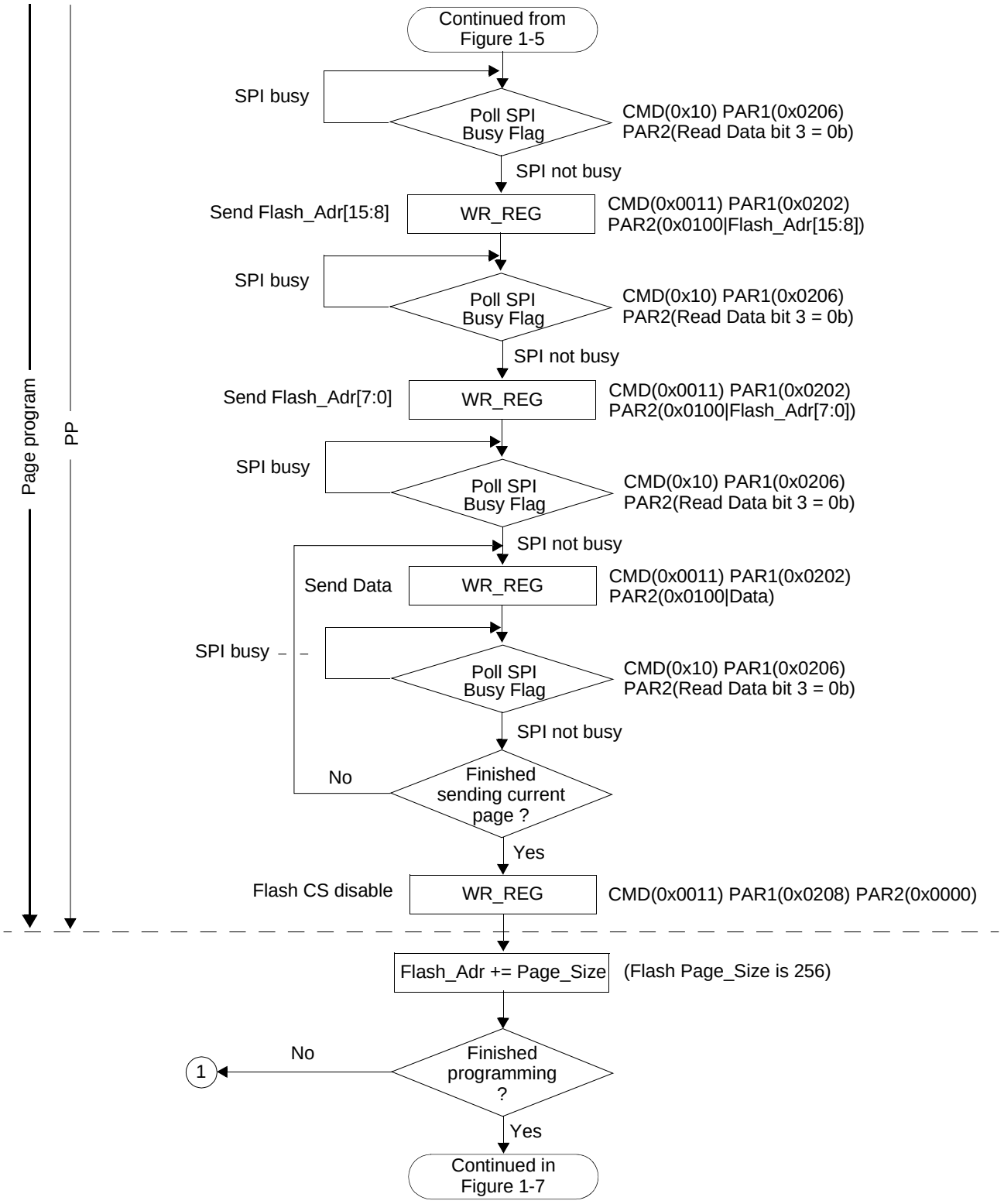

Figure 1-7: Command and Waveform Programming Flow (6 of 7)

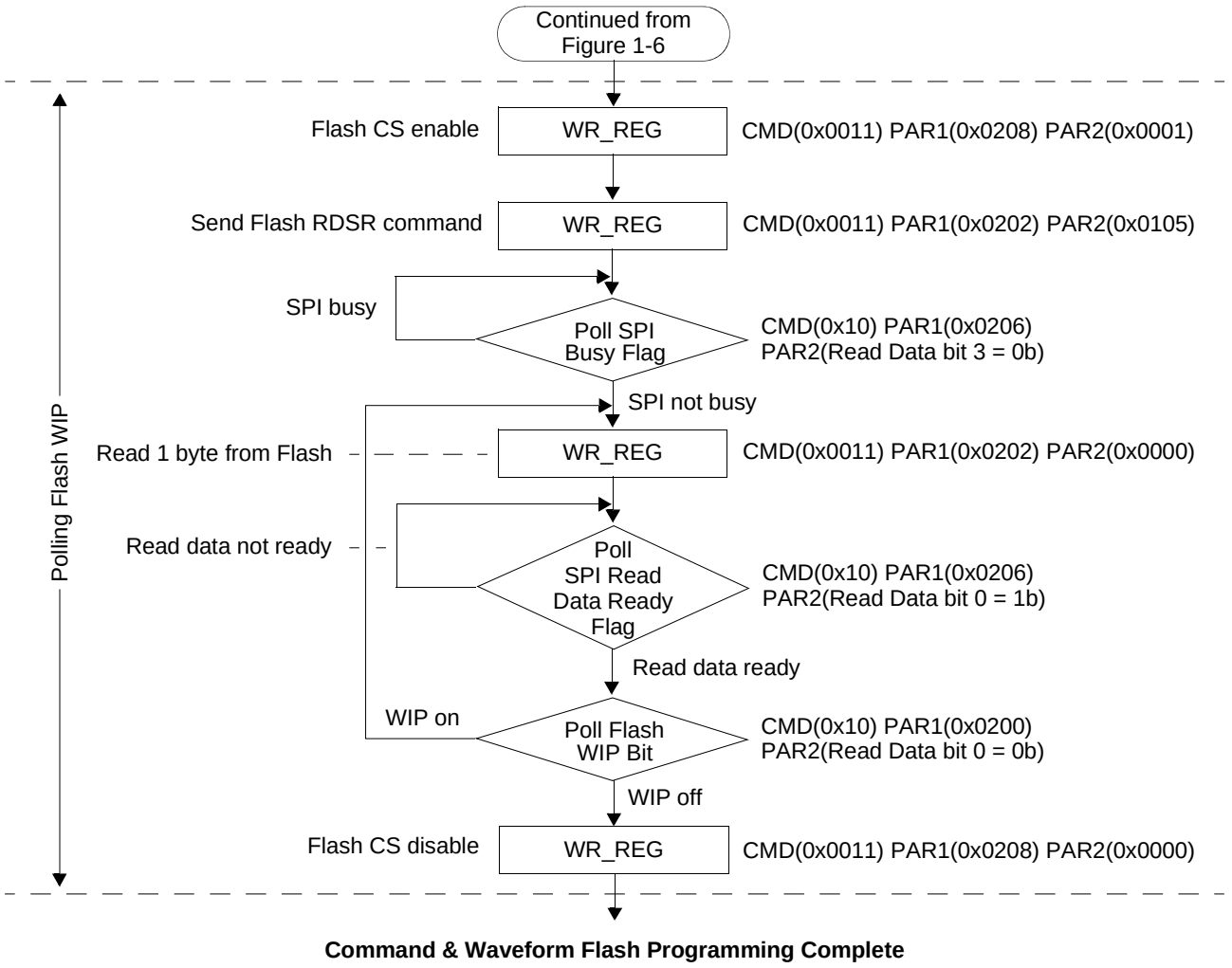

Figure 1-8: Command and Waveform Programming Flow (7 of 7)

1.3 Reference Sample Code

```
// Defines for M25P80
#define WREN    0x06
#define RDSR    0x05
#define WRSR    0x01
#define PP      0x02
#define SE      0xD8
#define BE      0xC7

BYTE buf_256[256];      // Buffer for page program, 256 bytes per page
BYTE buf_index;         // Buffer index
WORD byte_cnt;          // Byte count for page program loop
DWORD src_adr;          // Current address on the external 64Mbit font & image storage flash
DWORD des_adr;          // Current address on the EPD Controller Module flash
DWORD total_size;       // Current total size remaining to be programmed
DWORD page_size;        // Current page size to be programmed

                  :
                  :


WORD epd_cmd_rd_reg(WORD index)
{
    // Platform-specific implementation of CMD(0x0010) PAR1(index)
    return PAR2;
}

void epd_cmd_wr_reg(WORD index, WORD value)
{
    // Platform-specific implementation of CMD(0x0011) PAR1(index) PAR2(value)
}

void epd_cmd_flash_en(void)
{
    epd_cmd_wr_reg(0x0208, 0x0001);
}

void epd_cmd_flash_dis(void)
{
    epd_cmd_wr_reg(0x0208, 0x0000);
}

void epd_cmd_flash_wr(BYTE value)
{
    epd_cmd_wr_reg(0x0202, 0x0100|value);
    while ((epd_cmd_rd_reg(0x0206)&0x0008) == 0x0008);
}

BYTE epd_cmd_flash_rd(void)
{
    epd_cmd_wr_reg(0x0202, 0x0000);
    while ((epd_cmd_rd_reg(0x0206)&0x0001) == 0x0000);
    return epd_cmd_rd_reg(0x0200);
}

void epd_cmd_flash_wait_wip_end(void)
{
    epd_cmd_flash_en();
    epd_cmd_flash_wr(RDSR);
    while ((epd_cmd_flash_rd()&0x01) == 0x01);
    epd_cmd_flash_dis();
}

void epd_cmd_flash_wren(void)
{
    epd_cmd_flash_en();
    epd_cmd_flash_wr(WREN);
    epd_cmd_flash_dis();
    epd_cmd_flash_wait_wip_end();
```

```
}
                :
                :

    epd_cmd_wr_reg(0x000A, 0x1000);                 // OSC Cell Force Run Enable
    DelayMs(4);                                     // Delay 4ms, wait for OSC input clock stable

    // Config PLL
    epd_cmd_wr_reg(0x0010, 0x0003);
    epd_cmd_wr_reg(0x0012, 0x5949);
    epd_cmd_wr_reg(0x0014, 0x0040);

    epd_cmd_wr_reg(0x0016, 0x0001);                 // Wakeup PLL, keep PLL bypass
    while ((epd_cmd_rd_reg(0x000A)&0x0001) != 1);   // Wait for PLL lock
    epd_cmd_wr_reg(0x0016, 0x0000);                 // Disable PLL bypass
    epd_cmd_wr_reg(0x0006, 0x0000);                 // Disable power save

    // Initialize SPI
    epd_cmd_wr_reg(0x0204, 0x0001);                 // The flash memory has a max clock rate of 75MHz
    epd_cmd_wr_reg(0x0208, 0x0000);

    // Disable all Block Protect bits
    epd_cmd_flash_wren();
    epd_cmd_flash_en();
    epd_cmd_flash_wr(WRSR);
    epd_cmd_flash_wr(0x00);
    epd_cmd_flash_dis();
    epd_cmd_flash_wait_wip_end();

    // Block erase
    epd_cmd_flash_wren();
    epd_cmd_flash_en();
    epd_cmd_flash_wr(BE);
    epd_cmd_flash_dis();

    // Page program
    total_size = <Command & Waveform file size>;
    des_adr = 0;
    while (total_size > 0)
    {
        if (total_size >= 256)
            page_size = 256;
        else
            page_size = total_size;

        // Read 256 bytes from the source Command & Waveform file into buf_256

        epd_cmd_flash_wait_wip_end();               // Wait for previous operation to complete
        epd_cmd_flash_wren();
        epd_cmd_flash_en();
        epd_cmd_flash_wr(PP);
        epd_cmd_flash_wr((des_adr>>16) & 0x000000FF);
        epd_cmd_flash_wr((des_adr>>8)  & 0x000000FF);
        epd_cmd_flash_wr( des_adr      & 0x000000FF);
        buf_index = 0;
        byte_cnt = page_size;
        while (byte_cnt>0)
        {
            epd_cmd_flash_wr(buf_256[buf_index]);
            buf_index++;
            byte_cnt--;
        }
        epd_cmd_flash_dis();
        total_size = total_size - page_size;
        des_adr = des_adr + page_size;
    }
    epd_cmd_flash_wait_wip_end();                   // Wait for the last page program to complete
                :
                :
```

Change Record

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