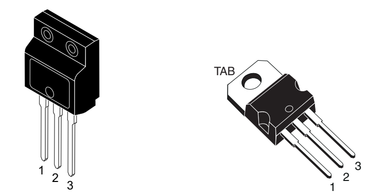
STFILED625, STPLED625

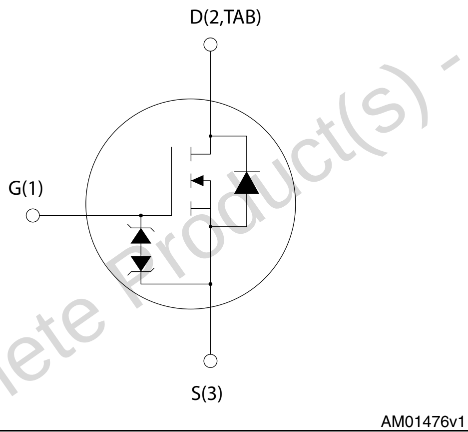
N-channel 620 V, 1.28 Ω typ., 5.0 A Power MOSFET in I²PAKFP and TO-220 packages

Datasheet — preliminary data



I²PAKFP **TO-220**

Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STFILED625	620 V	1.6 Ω	5.0 A	25 W
STPLED625				70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STFILED625	LED625	I^2PAKFP (TO-281)	Tube
STPLED625		TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I^2PAKFP	TO-220	
V_{DS}	Drain- source voltage	620		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	5.0 (1)	5.0	A
I_D	Drain current (continuous) at T_C = 100 °C	3.5 (1)	3.5	A
I_{DM} (2)	Drain current (pulsed)	20.0 (1)	20.0	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.2		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120		mJ
dv/dt (3)	Peak diode recovery voltage slope	12		V/ns
di/dt (3)	Diode reverse recovery current slope	400		A/µs
V_{ISO}	Insulation withstand voltage (AC)	2500		V
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq I_D$, peak $V_{DS} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		I^2PAKFP	TO-220	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	5	1.79	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.50		°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	620			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V; V_{DS}=0			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.6	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.1 A		1.28	1.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	690 52 8.5	-	pF pF pF
$C_{OSS\ eq}$(1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 496 V		16.6		pF
R_g	Gate input resistance	f=1 MHz open drain	-	4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 496 V, I_D = 4.2 A, V_{GS} = 10 V *(see Figure 18)*	-	27 4 16	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_DS increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 310 V, I_D = 4.2 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 17)*	-	12 8 40 21	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		4.2 16.8	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.2 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.2 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 19)*	-	290 1900 13		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.2 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 19)*	-	320 2200 14		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for I²PAKFP

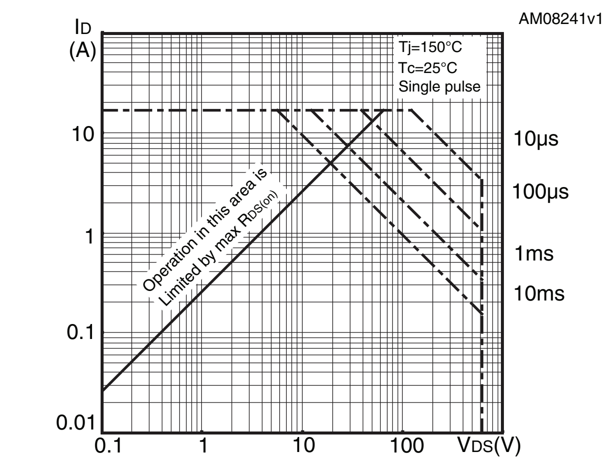


Figure 3. Thermal impedance for I²PAKFP

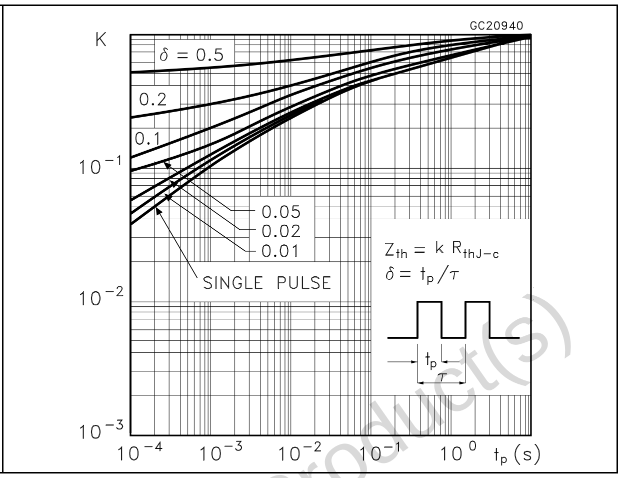


Figure 4. Safe operating area for TO-220

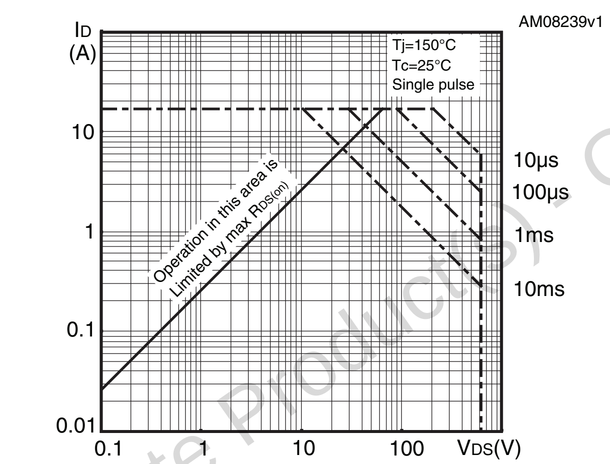


Figure 5. Thermal impedance TO-220

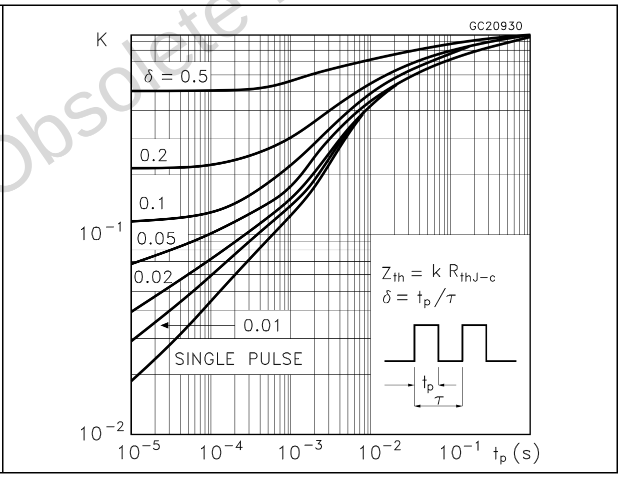


Figure 6. Output characteristics

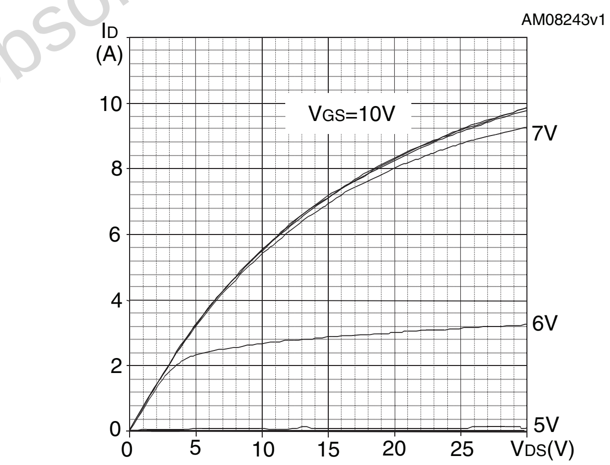


Figure 7. Transfer characteristics

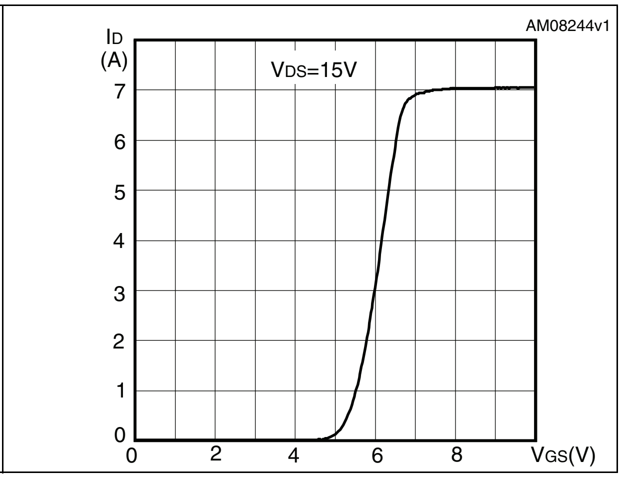


Figure 8. Gate charge vs gate-source voltage

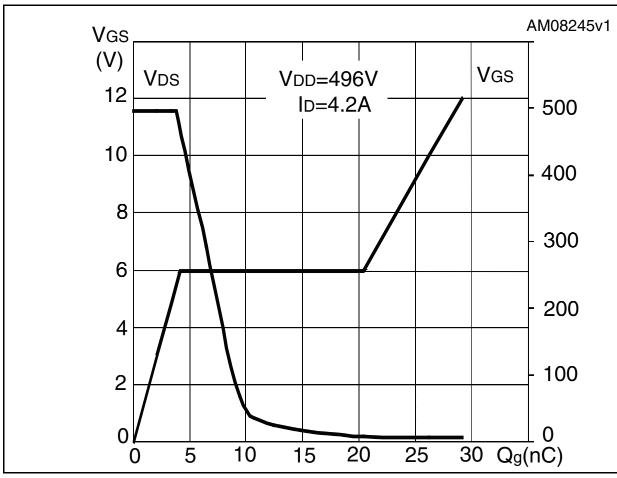


Figure 9. Static drain-source on-resistance

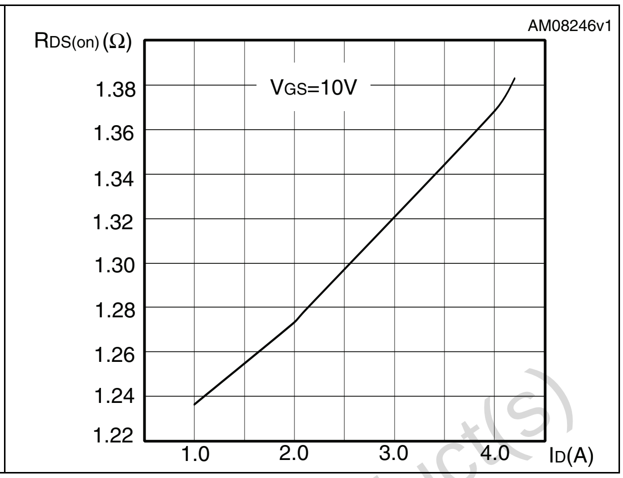


Figure 10. Capacitance variations

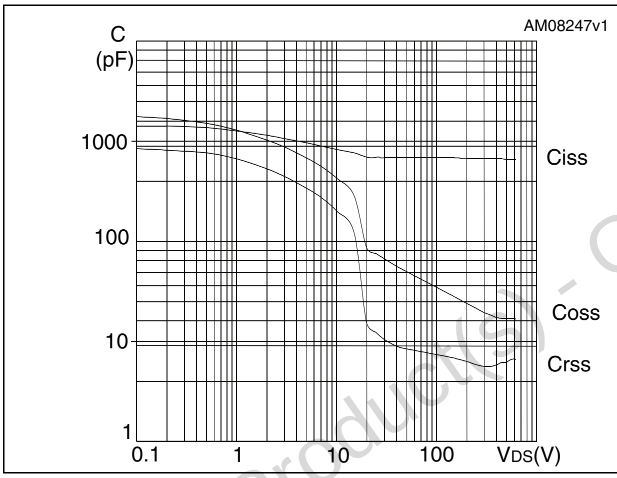


Figure 11. Output capacitance stored energy

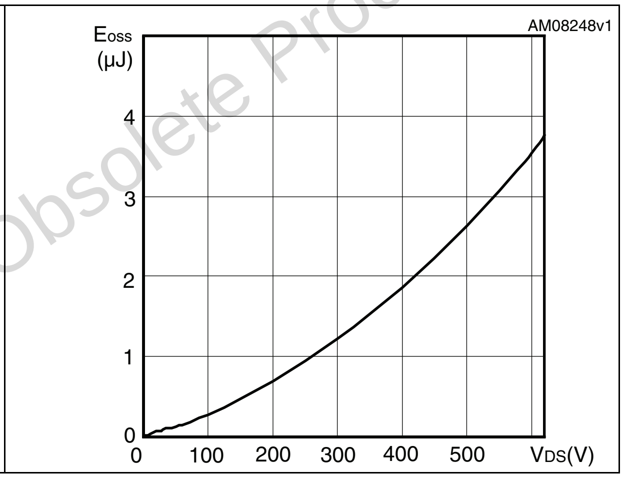


Figure 12. Normalized gate threshold voltage vs temperature

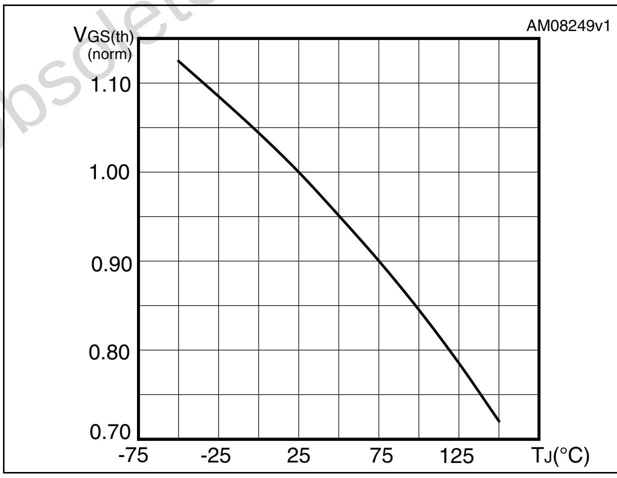


Figure 13. Normalized on-resistance vs temperature

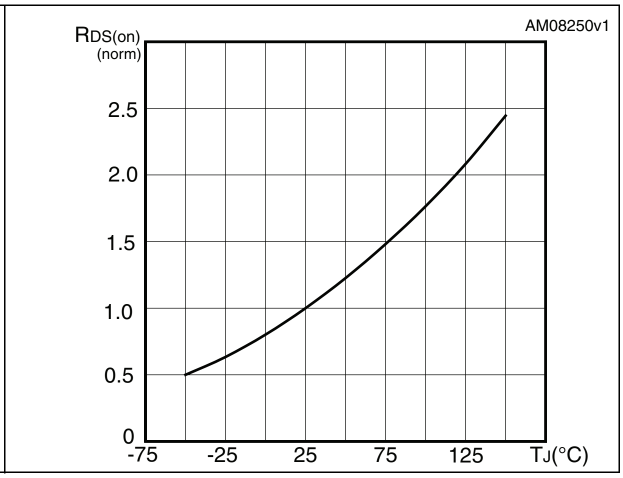


Figure 14. Source-drain diode forward characteristics

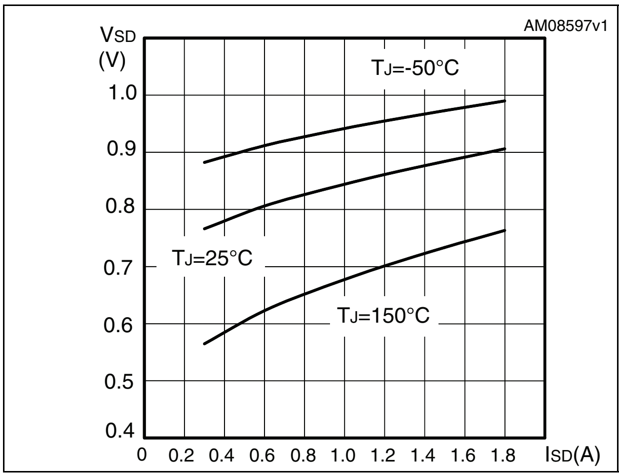


Figure 15. Normalized B_{VDSS} vs temperature

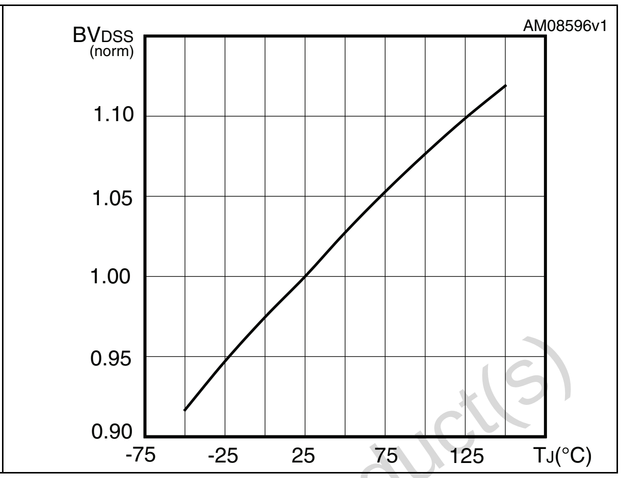
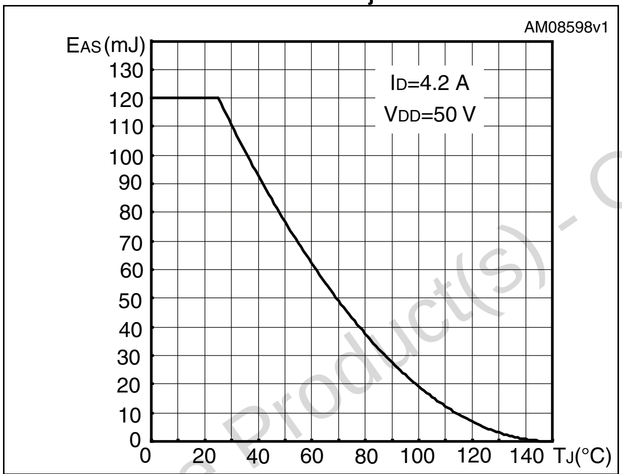


Figure 16. Maximum avalanche energy vs starting T_j



3 Test circuits

Figure 17. Switching times test circuit for resistive load

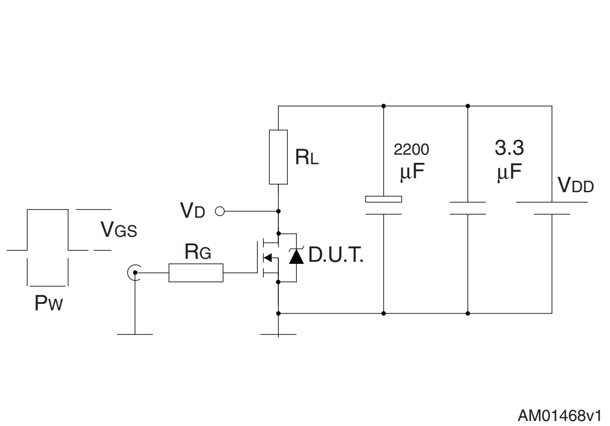


Figure 18. Gate charge test circuit

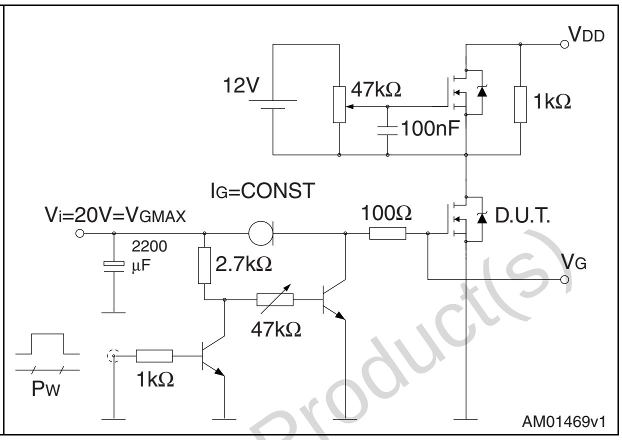


Figure 19. Test circuit for inductive load switching and diode recovery times

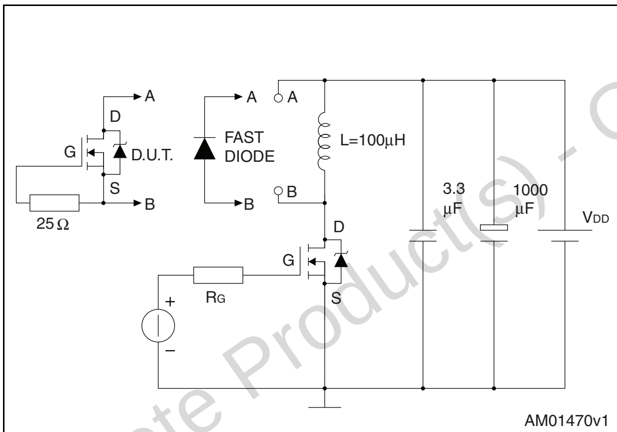


Figure 20. Unclamped inductive load test circuit

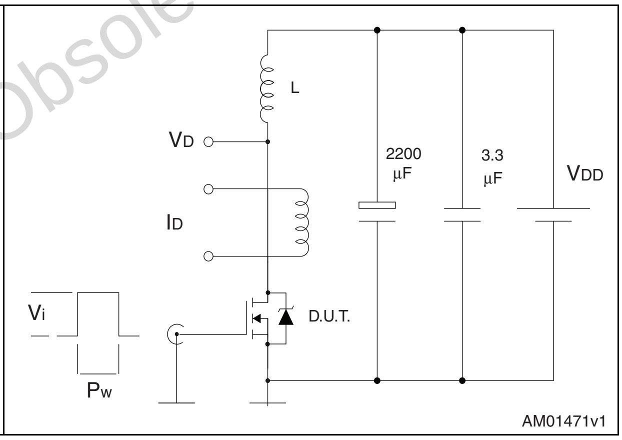


Figure 21. Unclamped inductive waveform

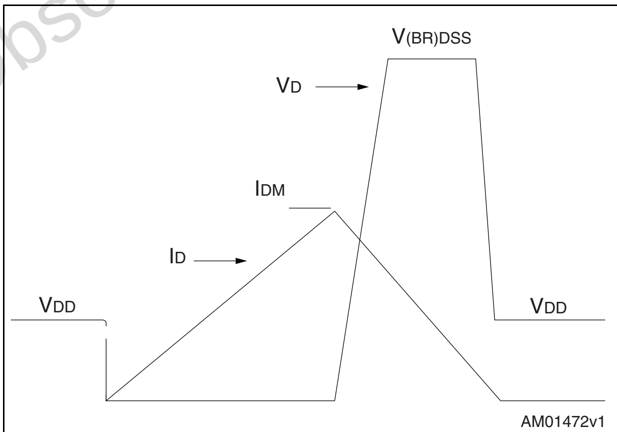
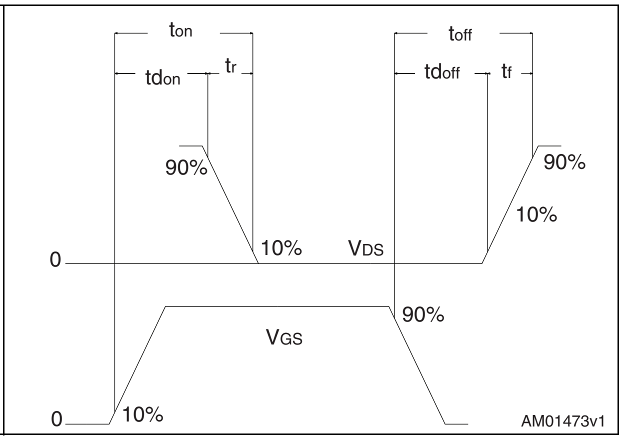


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 23. I^2PAKFP (TO-281) drawing

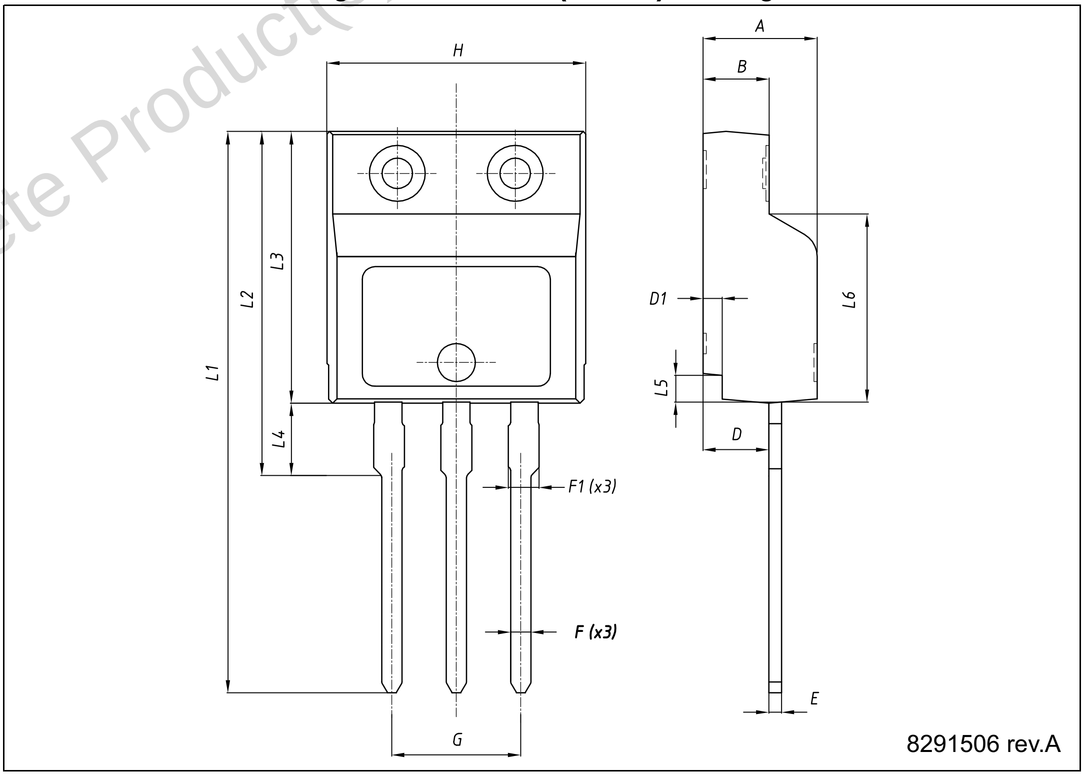
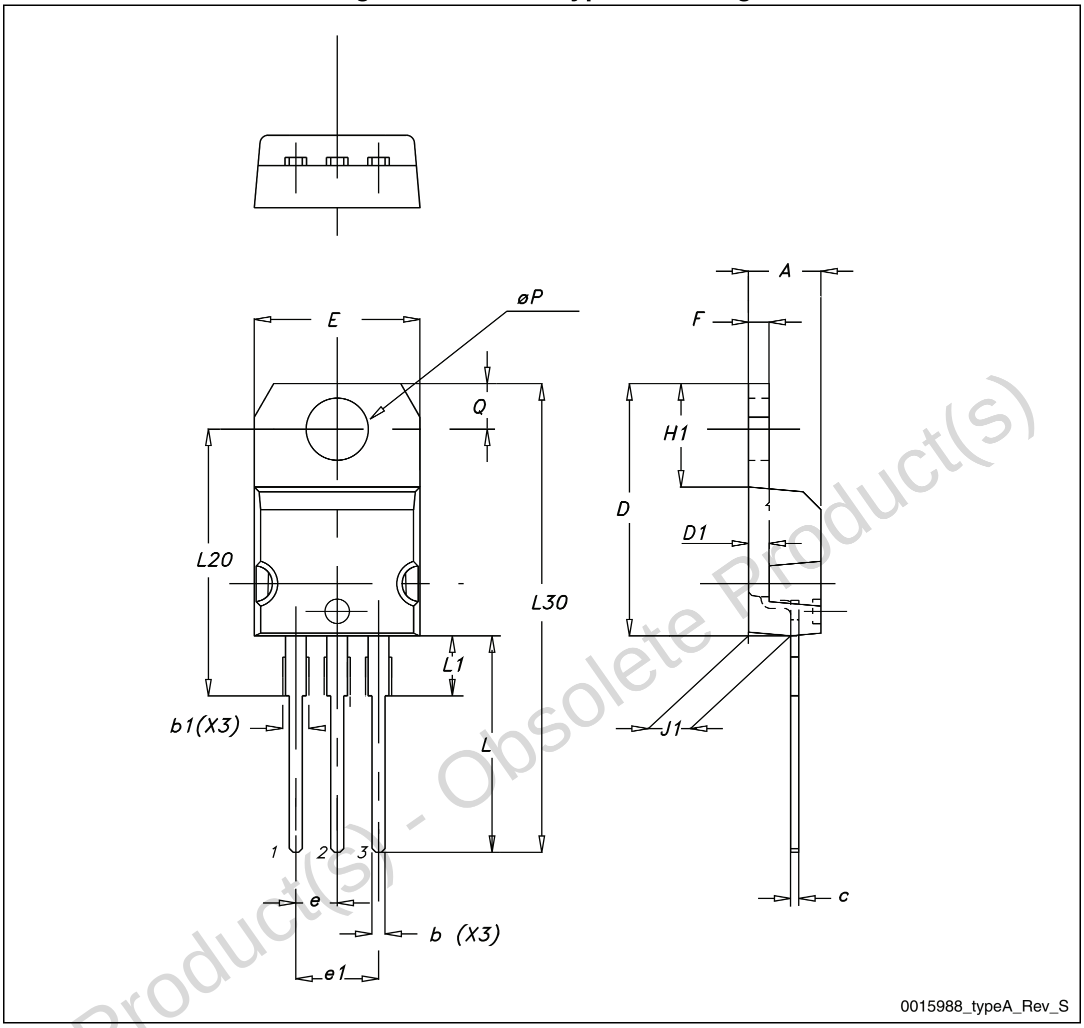


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
25-Mar-2013	1	First release.