



STS6NF20V

N-channel 20 V, 0.030 Ω typ., 6 A 2.7 V drive STripFET™ II
Power MOSFET in a SO-8 package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)}	I _D
STS6NF20V	20 V	< 0.040 Ω (@4.5 V)	6 A
		< 0.045 Ω (@2.7 V)	

- Ultra low threshold gate drive (2.5 V)
- Standard outline for easy automated surface mount assembly

Applications

- Switching application

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

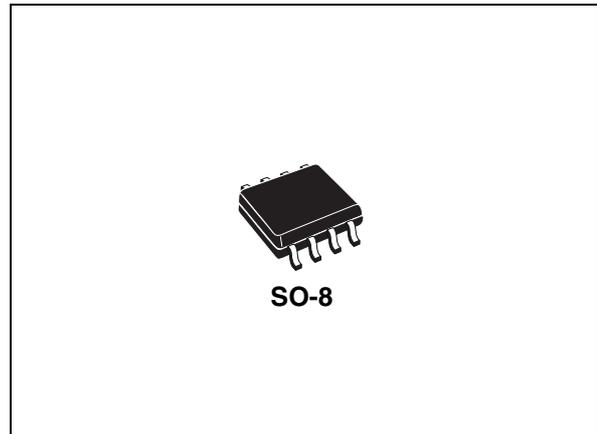


Figure 1. Schematic diagram

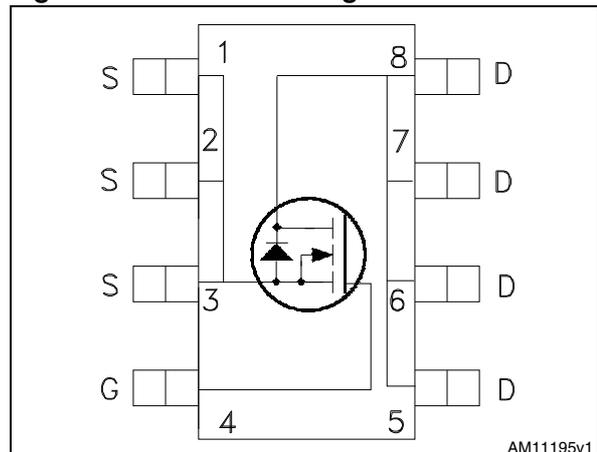


Table 1. Device summary

Order code	Marking	Package	Packaging
STS6NF20V	S6NF20V	SO-8	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate- source voltage	± 12	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.5	W
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C/W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20\ \text{V}$ $V_{DS} = 20\ \text{V}$, $T_C = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6			V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 4.5\ \text{V}$, $I_D = 3\ \text{A}$		0.030	0.040	Ω
		$V_{GS} = 2.7\ \text{V}$, $I_D = 3\ \text{A}$		0.037	0.045	Ω
		$V_{GS} = 1.95\ \text{V}$, $I_D = 0.9\ \text{A}$			0.09	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance		6.5	10	15	S
C_{iss}	Input capacitance	$V_{DS} = 15\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$	320	460	640	μF
C_{oss}	Output capacitance					
C_{rss}	Reverse transfer capacitance					
Q_g	Total gate charge	$V_{DD} = 16\ \text{V}$, $I_D = 6\ \text{A}$,	5.5	8.5	11.5	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\ \text{V}$	1.2	1.8	2.5	nC
Q_{gd}	Gate-drain charge	(see Figure 13)	1.6	2.4	3.4	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 12)	-	7	20	ns
t_r	Rise time			33	45	ns
$t_{d(off)}$	Turn-off-delay time			27	40	ns
t_f	Fall time			10	20	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 10\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	26		ns
Q_{rr}	Reverse recovery charge			13		nC
I_{RRM}	Reverse recovery current			1		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

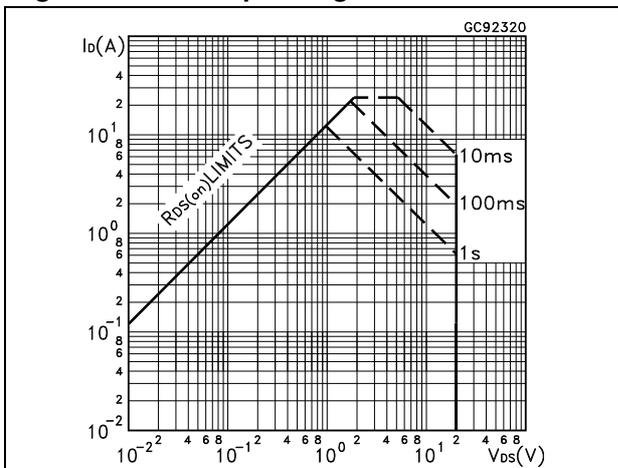


Figure 3. Thermal impedance

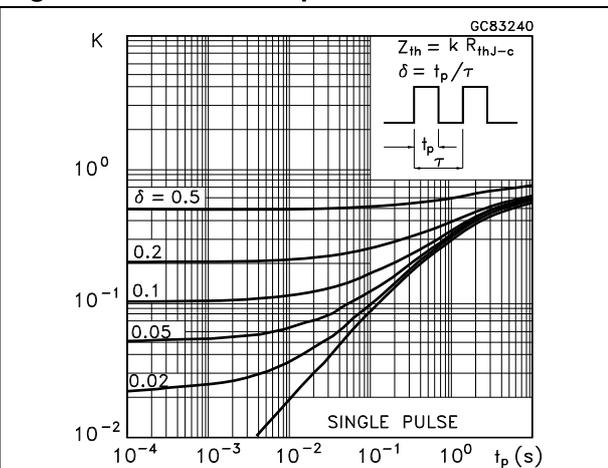


Figure 4. Output characteristics

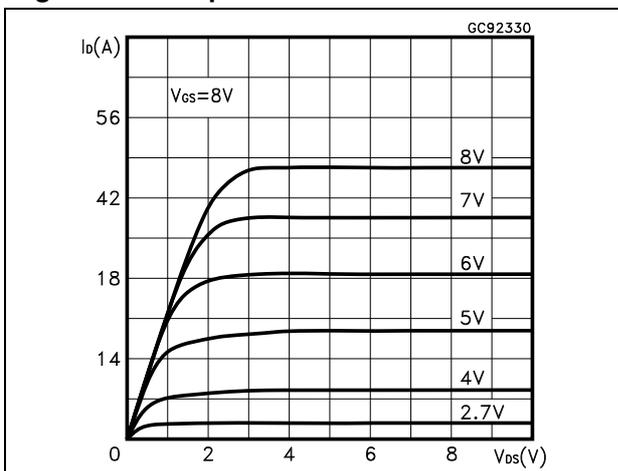


Figure 5. Transfer characteristics

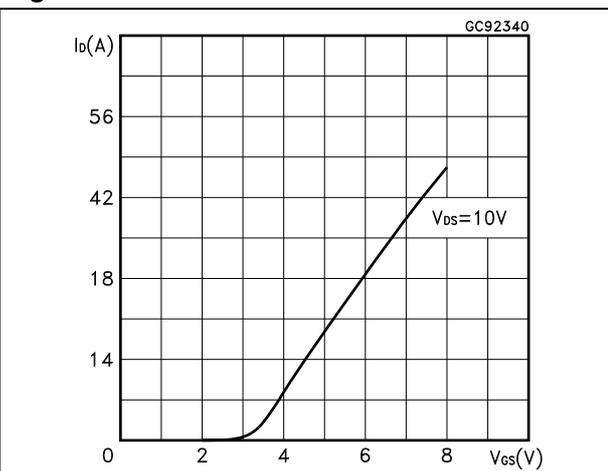


Figure 6. Source-drain diode forward characteristics

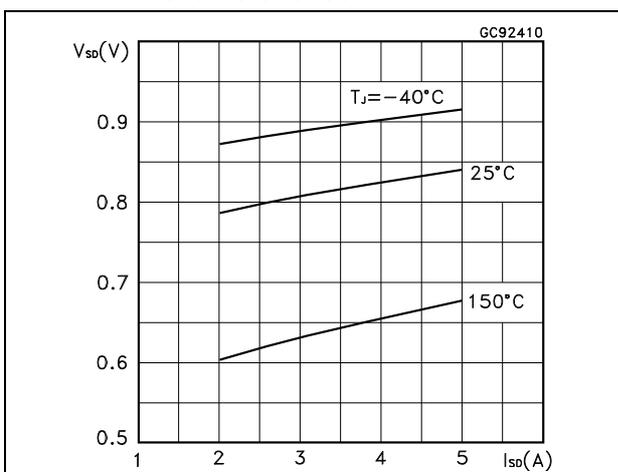


Figure 7. Static drain-source on-resistance

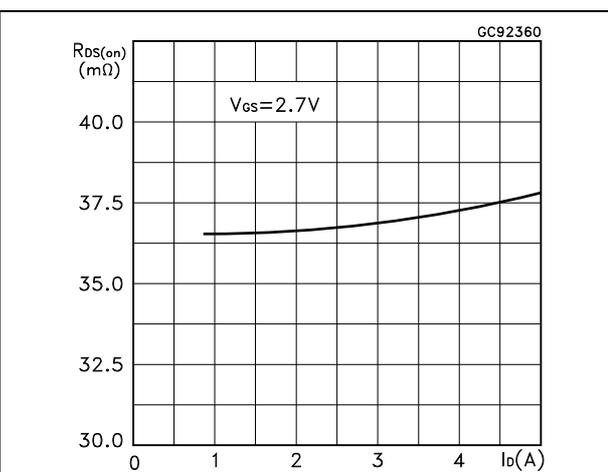


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

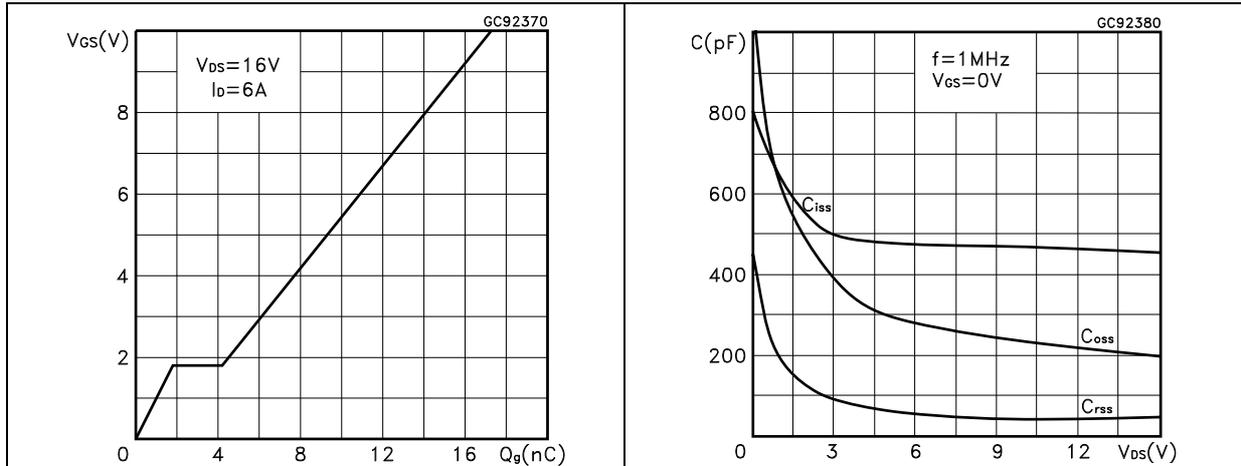
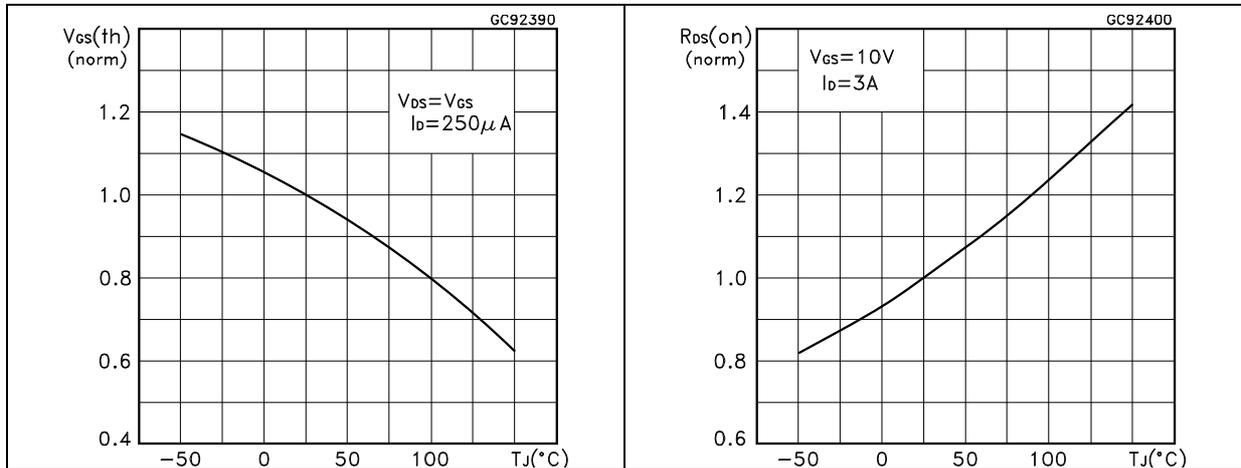
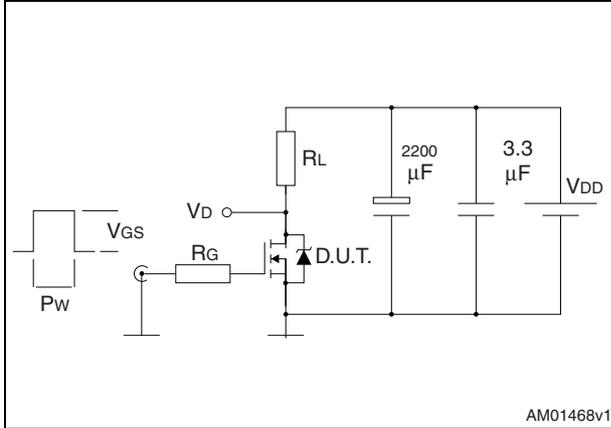


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature



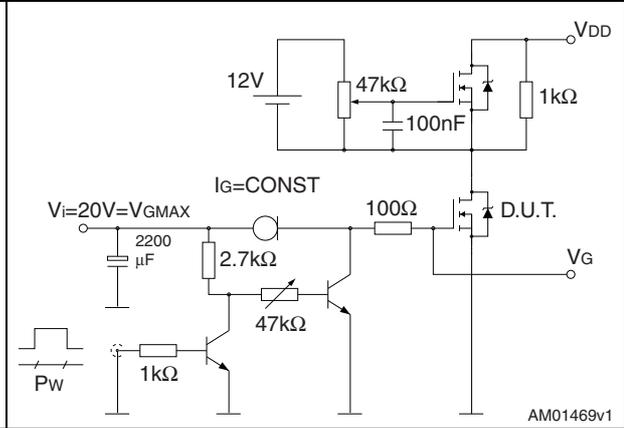
3 Test circuits

Figure 12. Switching times test circuit for resistive load



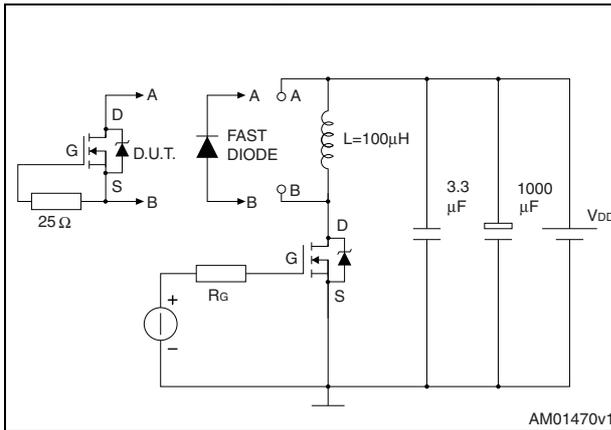
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Figure 13. Gate charge test circuit



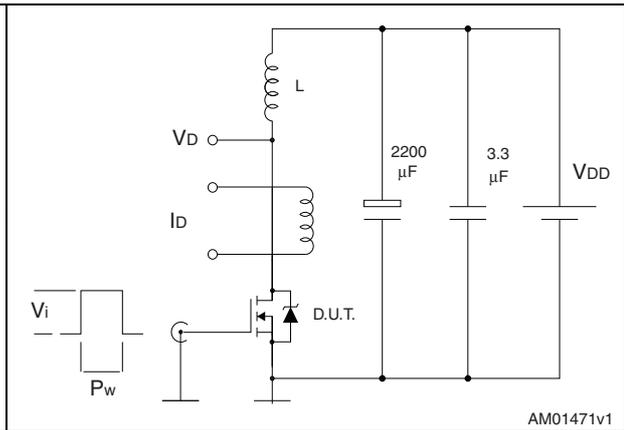
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Figure 14. Test circuit for inductive load switching and diode recovery times



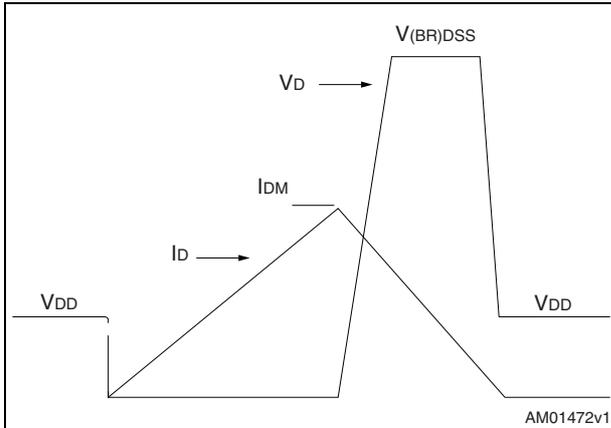
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Figure 15. Unclamped inductive load test circuit



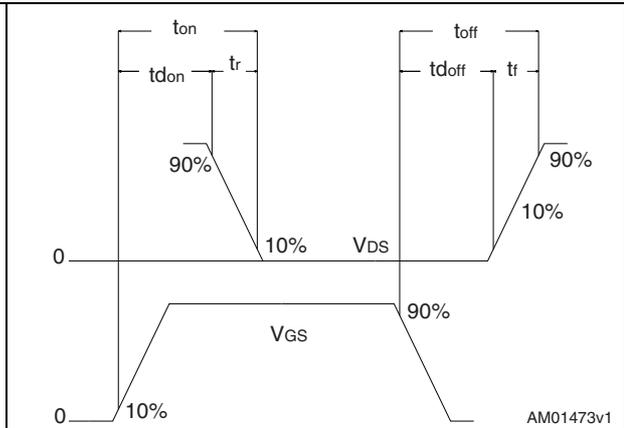
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Figure 16. Unclamped inductive waveform



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Figure 17. Switching time waveform



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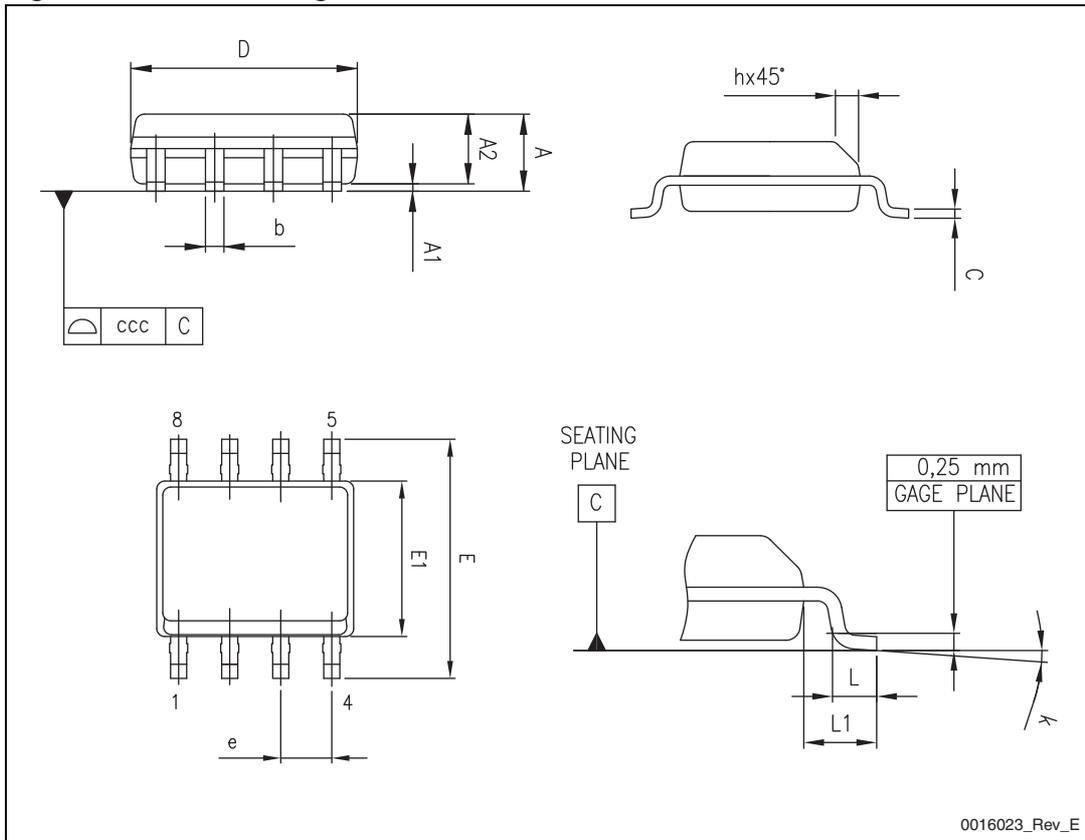
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 18. SO-8 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Feb-2008	1	First release
18-Nov-2009	2	Added new $R_{DS(on)}$ value on Table 4: On /off states
29-Nov-2012	3	Max values have been added in Table 5: Dynamic and Table 6: Switching times . Section 4: Package mechanical data has been updated. Minor text changes.

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