

V _{DSS}	30V
R _{DS(on)} (Max.)	71mΩ
Ι _D	±3A
P _D	1.25W

Features

Application

Switching

- 1) Low on resistance.
- 2) Low voltage drive(4V drive)
- 3) Small surface mount package(TSST8)



Inner circuit



Packaging specifications

	Packing	Embossed Tape
	Reel size (mm)	180
Туре	Tape width (mm)	8
,	Basic ordering unit (pcs)	3000
	Taping code	TR
	Marking	K11

• Absolute maximum ratings ($T_a = 25^{\circ}C$) <It is the same ratings for the Tr1 and Tr2>

U (u	0			
Parameter		Symbol	Value	Unit
Drain - Source voltage		V _{DSS}	30	V
Continuous drain current		I _D	±3	А
Pulsed drain current		*1 D,pulse	±12	А
Gate - Source voltage		V _{GSS}	±20	V
	total	– P _D *2	1.25	
Power dissipation	element		1.0	W
	total	P _D *3	0.6	
Junction temperature	·	Tj	150	°C
Range of storage temperature		T _{stg}	-55 to +150	°C

Thermal resistance

Parameter		Symbol	Values			Unit
		Symbol	Min.	Тур.	Max.	Unit
	total	D *2	-	-	100	
Thermal resistance, junction - ambient	element	R_{thJA}^{*2}	-	-	125	°C/W
	total	R_{thJA}^{*3}	-	-	208	

•Electrical characteristics (T_a = 25°C) <It is the same characteristics for the Tr1 and Tr2>

Deremeter	Currence of	mbol Conditions	Values			Linit
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Drain - Source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 1mA	30	-	-	V
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T}$	_	-	34.15	-	mV/°C
	Δ T _j	referenced to 25°C				
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	-	-	1	μA
Gate - Source leakage current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±10	μA
Gate threshold voltage	V _{GS(th)}	V _{DS} = 10V, I _D = 1A	1.0	-	2.5	V
Gate threshold voltage	$\Delta V_{GS(th)}$	I _D = -1mA				
temperature coefficient	ΔT _j	referenced to 25°C	-	-2.34	-	mV/°C
		V _{GS} = 10V, I _D = 3A	-	51	71	
Static drain - source on - state resistance	R _{DS(on)} *4	V _{GS} = 4.5V, I _D = 3A	-	67	94	mΩ
		V _{GS} = 4V, I _D = 3A	-	78	109	
Forward Transfer Admittance	Y _{fs} *4	V _{DS} = 10V, I _D = 3A	2.0	-	-	S



•Electrical characteristics (T_a = 25°C) <It is the same characteristics for the Tr1 and Tr2>

Parameter	Sumbol	Conditions		Unit		
	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input capacitance	C _{iss}	V _{GS} = 0V	-	140	-	
Output capacitance	C _{oss}	V _{DS} = 10V	-	55	-	pF
Reverse transfer capacitance	C _{rss}	f = 1MHz	-	28	-	
Turn - on delay time	t _{d(on)} *4	$V_{DD} \simeq 15 V, V_{GS} = 4.5 V$	-	5	-	
Rise time	t _r *4	I _D = 1.5A	-	13	-	20
Turn - off delay time	t _{d(off)} *4	R _L = 10Ω	-	20	-	ns
Fall time	t_{f}^{*4}	R _G = 10Ω	-	3	-	

•Gate charge characteristics (T_a = 25°C) <It is the same characteristics for the Tr1 and Tr2>

Deremeter	Sumbol	Conditions	Values			Unit	
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	
Total gate charge	Q_g^{*4}	$V_{DD} \simeq 15V$	-	2.5	-		
Gate - Source charge	Q _{gs} *4	I _D = 3A	-	0.8	-	nC	
Gate - Drain charge	Q _{gd} *4	V _{GS} = 5V	-	0.6	-		

●Body diode electrical characteristics (Source-Drain) (T_a = 25°C)

< It is the same characteristics for the Tr1 and Tr2>

Deremeter	Symbol	Conditions	Values			Unit
Parameter	Symbol Conditions –		Min.	Тур.	Max.	Unit
Body diode continuous forward current	I _S	T - 25°0	-	-	0.8	Δ
Body diode pulse current	I _{SP} *1	T _a = 25°C	-	-	12	A
Forward voltage	V _{SD} *4	V _{GS} = 0V, I _S = 3A	-	-	1.2	V

*1 Pw \leq 10µs , Duty cycle \leq 1%

- *2 Mounted on a ceramic board (30×30×0.8mm)
- *3 Mounted on a FR4 (20×20×0.8mm)
- *4 Pulsed





Fig.1 Power Dissipation Derating Curve

Fig.2 Maximum Safe Operating Area



Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width



Fig.4 Single Pulse Maximum Power dissipation





Drain Current : I_D [A]

• Electrical characteristic curves



Fig.5 Typical Output Characteristics(I)

T_a=25°C

Pulsed

V_{GS}=2.5V

0.8

1

Drain Current : I_D [A]

Drain - Source Voltage : V_{DS} [V]





Fig.7 Breakdown Voltage vs. Junction Temperature



Fig.8 Typical Transfer Characteristics







Fig.9 Gate Threshold Voltage vs.

Fig.10 Forward Transfer Admittance vs. Drain Current



Fig.11 Drain Current Derating Curve

Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage







Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current (I)







Fig.15 Static Drain - Source On - State Resistance vs. Drain Current (II) Fig.16 Static Drain - Source On - State Resistance vs. Drain Current (III)





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Fig.18 Typical Capacitance vs. Drain - Source Voltage

Fig.19 Switching Characteristics



Fig.20 Dynamic Input Characteristics

Fig.21 Source Current vs. Source Drain Voltage



Source - Drain Voltage : V_{SD} [V]

Gate - Source Voltage : V_{GS} [V]

10



Source Current : I_s [A]



•Measurement circuits <It is the same for the Tr1 and Tr2>





Fig. 1-2 SWITCHING WAVEFORMS



Fig. 2-2 GATE CHARGE WAVEFORM



Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.



Dimensions

TSST8



Pattern of terminal position areas [Not a pattern of soldering pads]

DIM	MILIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	0.75	0.85	0.030	0.033
A1	0.00	0.05	0.000	0.002
b	0.22	0.42	0.009	0.017
с	0.12	0.22	0.005	0.009
D	2.90	3.10	0.114	0.122
Е	1.50	1.70	0.059	0.067
е	0.	65	0.0	26
HE	1.80	2.00	0.071	0.079
L	0.05	0.25	0.002	0.010
L1	0.05	0.25	0.002	0.010
Lp	0.15	0.34	0.006	0.013
Lp1	0.15	0.34	0.006	0.013
х		0.10	-	0.004
У		0.10	-	0.004
DIM	MILIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
b2	-	0.52	-	0.020
e1	1.4	46	0.0	57
1	-	0.44	-	0.017
12	. . .	0.44	-	0.017

Dimension in mm/inches



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