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January 2015

FDMS86255ET150

N-Channel Shielded Gate PowerTrench® MOSFET

150 V, 63 A, 12.4 mΩ

Features

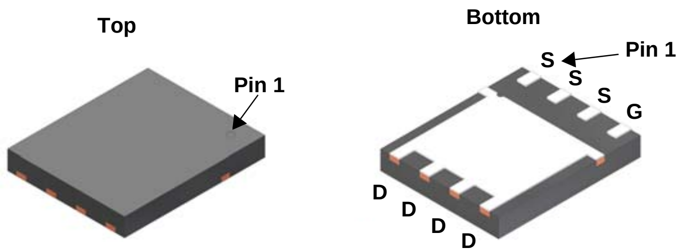
- Extended T_J rating to 175°C
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 12.4 mΩ at V_{GS} = 10 V, I_D = 10 A
- Max $r_{DS(on)}$ = 15.5 mΩ at V_{GS} = 6 V, I_D = 8 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

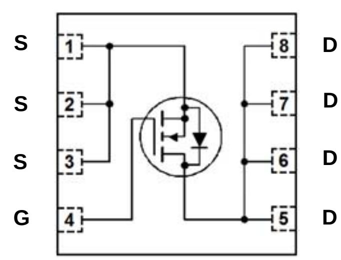
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- OringFET / Load Switching
- Synchronous rectification
- DC-DC Conversion



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				150	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	-Continuous	T_C = 25 °C	(Note 5)	63	A
		-Continuous	T_C = 100°C	(Note 5)	44	
		-Continuous	T_A = 25 °C	(Note 1a)	10	
		-Pulsed		(Note 4)	276	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	541	mJ
P_D	Power Dissipation		T_C = 25 °C		136	W
	Power Dissipation		T_A = 25 °C	(Note 1a)	3.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	45	

Package Marking and Ordering Information

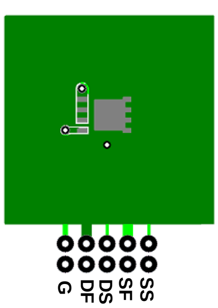
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86255ET	FDMS86255ET150	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

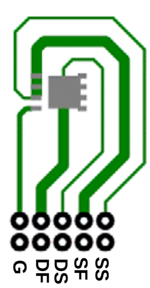
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		109		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A		9.5	12.4	mΩ
		V_{GS} = 6 V, I_D = 8 A		11.5	15.5	
		V_{GS} = 10 V, I_D = 10 A, T_J = 125 °C		19	25	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 10 A		35		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz		3200	4480	pF
C_{oss}	Output Capacitance			291	410	pF
C_{rss}	Reverse Transfer Capacitance			11	20	pF
R_g	Gate Resistance		0.1	0.7	2.1	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 75 V, I_D = 10 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		21	34	ns
t_r	Rise Time			4.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns
t_f	Fall Time			6.2	12	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 75 V, I_D = 10 A		45	63	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V; V_{DD} = 75 V, I_D = 10 A		29	41	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 75 V, I_D = 10 A		14		nC
Q_{gd}	Gate to Drain “Miller” Charge			8.8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 10 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 10 A, di/dt = 100 A/μs		87	139	ns
Q_{rr}	Reverse Recovery Charge			165	264	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 45 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 541 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 19 A, V_{DD} = 150 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 60 A.
4. Pulse Id please refer to Fig.11 SOA curve for detail.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

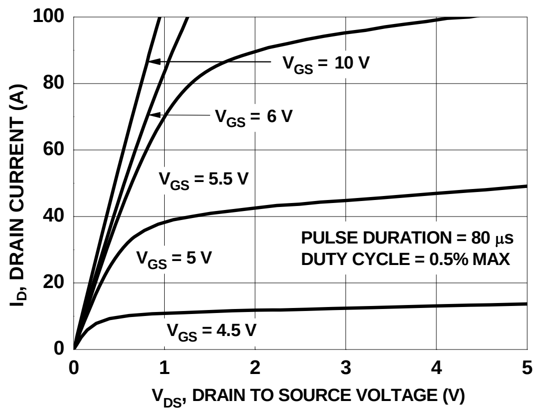


Figure 1. On-Region Characteristics

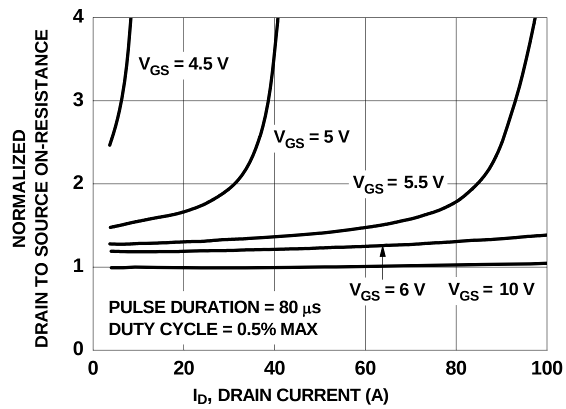


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

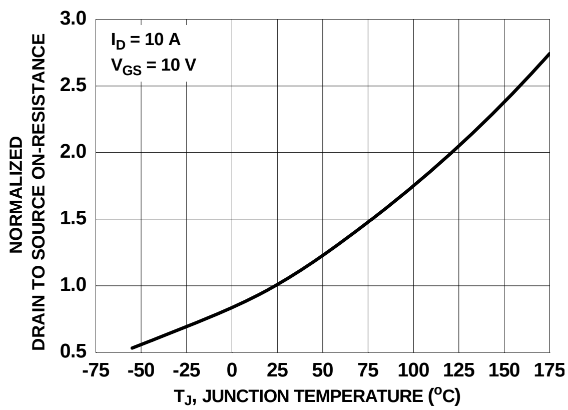


Figure 3. Normalized On-Resistance vs Junction Temperature

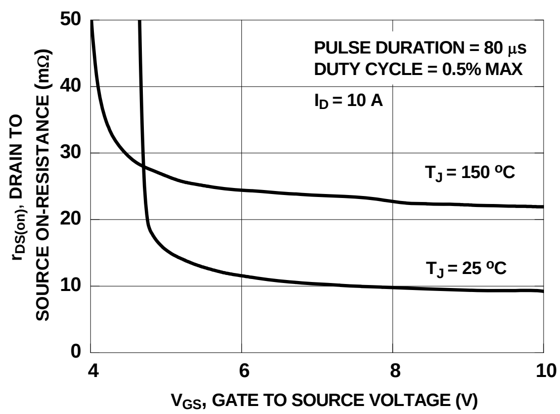


Figure 4. On-Resistance vs Gate to Source Voltage

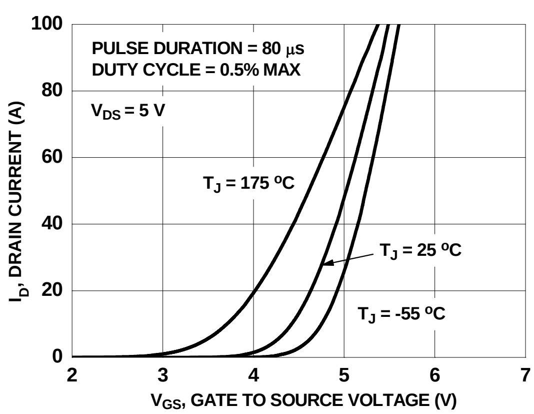


Figure 5. Transfer Characteristics

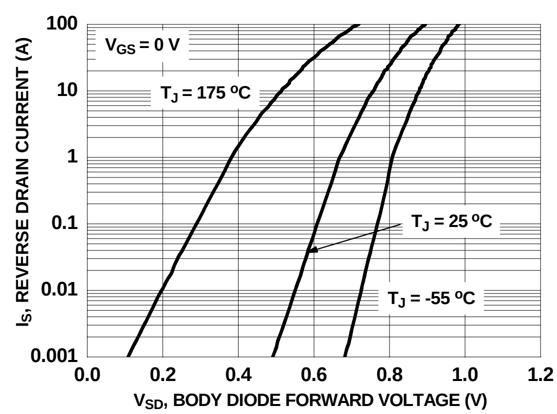


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

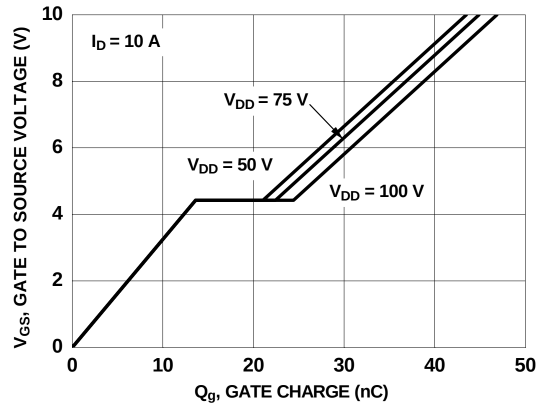


Figure 7. Gate Charge Characteristics

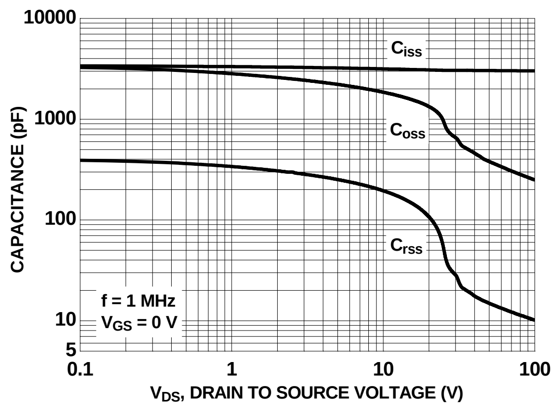


Figure 8. Capacitance vs Drain to Source Voltage

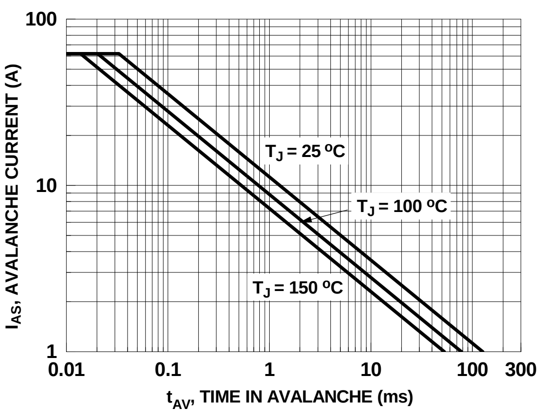


Figure 9. Unclamped Inductive Switching Capability

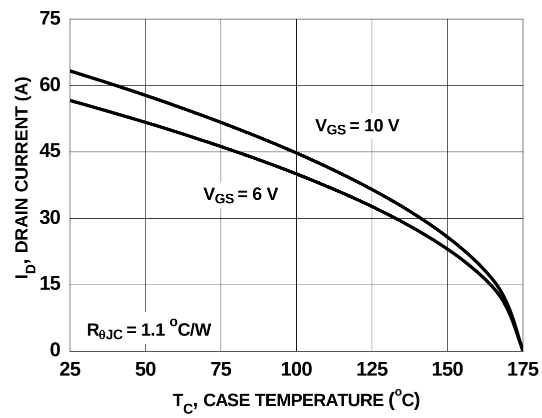


Figure 10. Maximum Continuous Drain Current vs Case Temperature

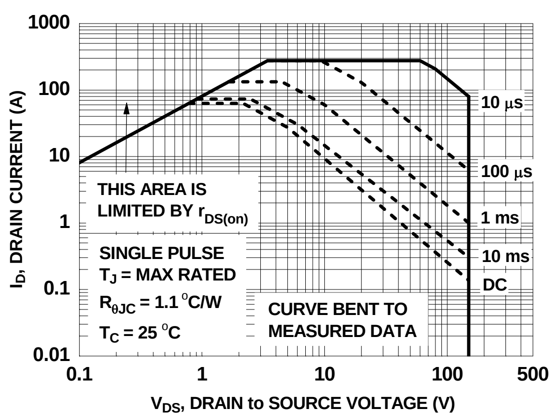


Figure 11. Forward Bias Safe Operating Area

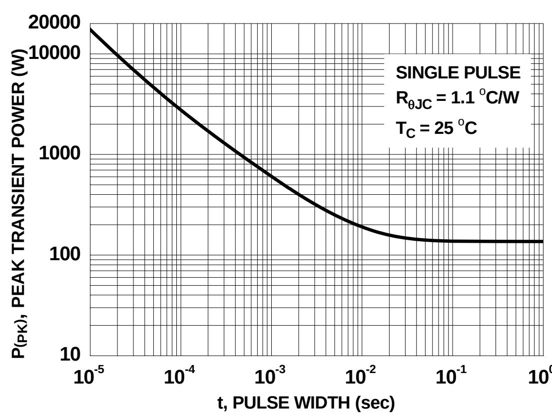


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

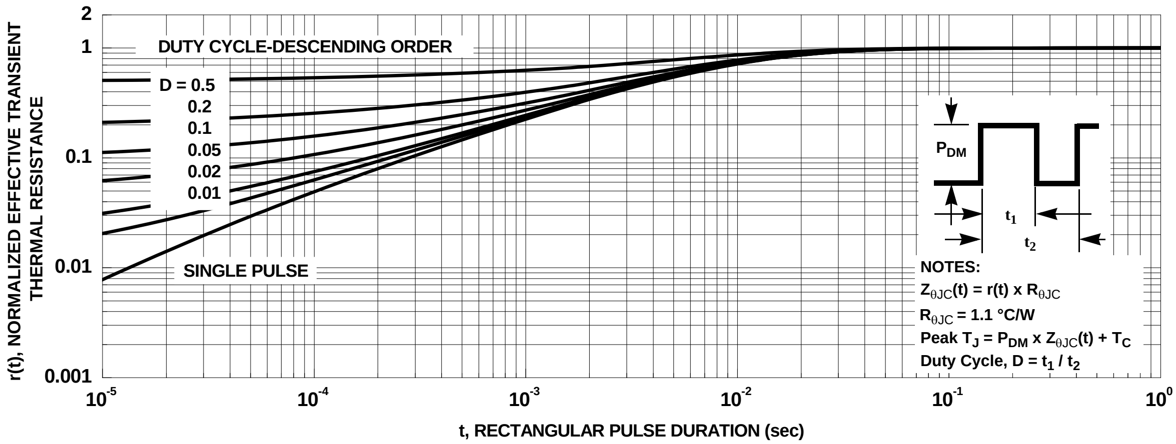
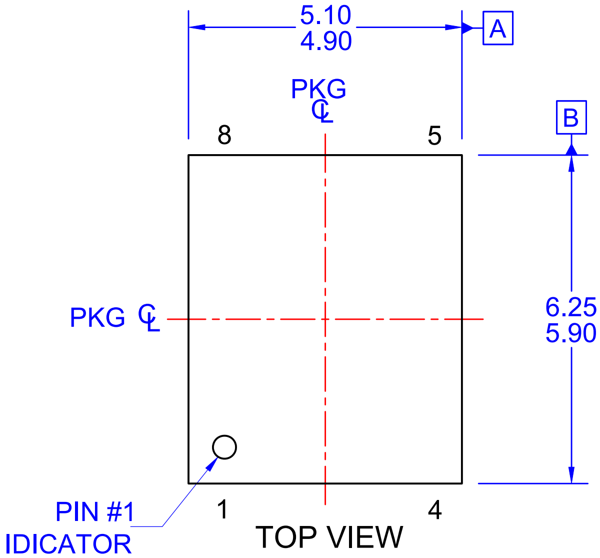
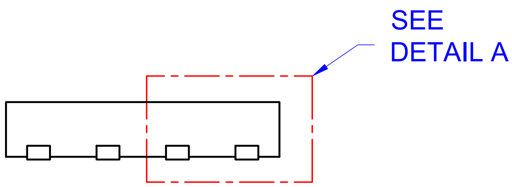


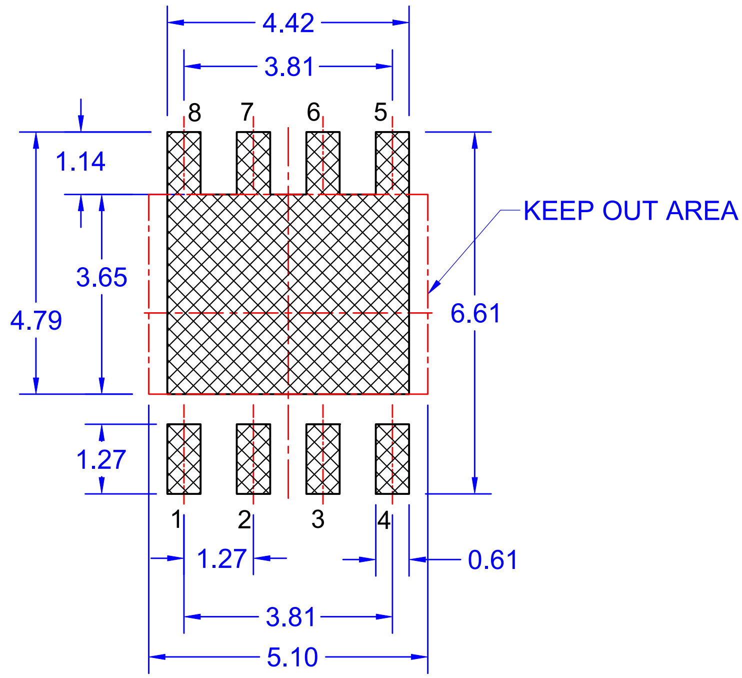
Figure 13. Transient Thermal Response Curve



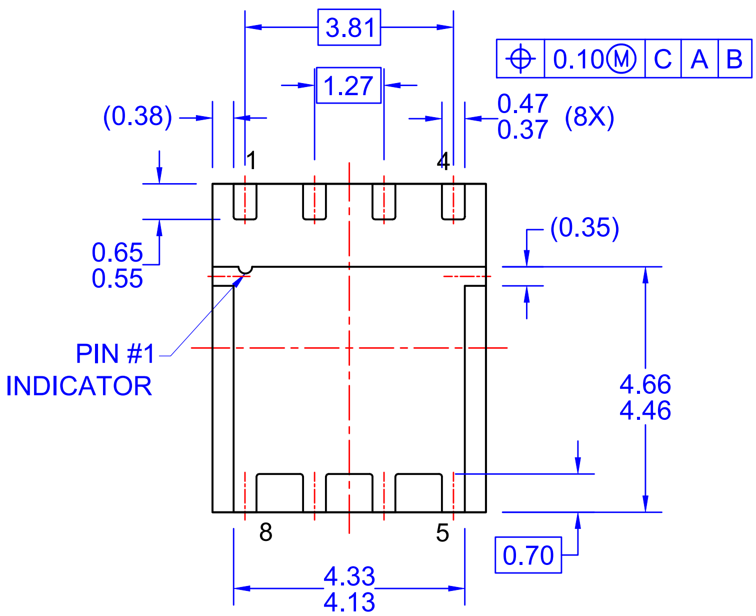
TOP VIEW



SIDE VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW

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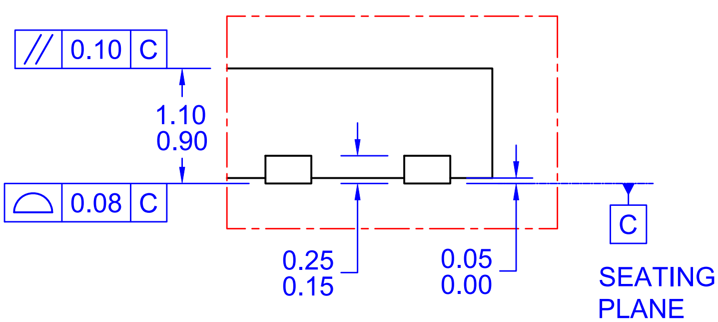
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F) DRAWING FILE NAME: PQFN08JREV3.



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