

DUAL CHANNEL 3A 20V MONOLITHIC SYNCHRONOUS STEP-DOWN REGULATOR

DESCRIPTION

Demonstration circuit DC1896 is a dual output regulator consisting of two constant-frequency step-down converters, based on the LTC3633A-3 monolithic dual channel synchronous buck regulator. The DC1896 has an input voltage range of 3.6V to 20V, with each regulator capable of delivering up to 3A of output current. The DC1896 can operate in either Burst Mode™ or forced continuous mode. In shutdown, the DC1896 can run off of less than 15 uA total. The DC1896 is a very efficient circuit: up to

90%. The DC1896 uses the 28 Pin QFN LTC3633AEFE-3 package, which has an exposed pad on the bottom-side of the IC for better thermal performance. These features, plus a programmable operating frequency range from 500 kHz to 4 MHz (2 MHz switching frequency with the RT pin connected to INTVcc), make the DC1896 demo board an ideal circuit for use industrial or distributed power applications. **Design files for this circuit are available at www.linear.com/demo.**

QUICK START PROCEDURE

The DC1896 is easy to set up to evaluate the performance of the LTC3633A-3. For a proper measurement equipment configuration, set up the circuit according to the diagram in Figure 1.

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals. See the proper scope probe technique in figure 2.

Please follow the procedure outlined below for proper operation.

1. Connect the input power supply to the Vin1/Vin2 and GND terminals (Vin1 and Vin2 are separate nodes.). Connect the loads between the Vout and GND terminals. Refer to figure 1 for the proper measurement equipment setup.

Before proceeding to operation, insert jumper shunts XJP1 and XJP2 into the OFF positions of headers JP1 and JP2, shunt XJP11 into the ON position (180°out-of-phase) of PHASE header JP11, shunts XJP3 and XJP4 into the

soft-start (SS) positions of headers JP3 and JP4, shunt XJP8 into the forced continuous mode (FCM) position of MODE header JP8, shunt XJP14 into the 1 MHz position of the frequency (FREQ) header JP14, shunts XJP12 and XJP13 into the external (EXT) compensation positions of headers JP12 and JP13, and shunt XJP6 into the Vout1 voltage options of choice of header JP6: 1.5V, 1.8V, or 2.5V, and a shunt into the Vout2 voltage option of choice: 2.5V (header JP15), 3.3V (header JP5), or 5V (header JP7).

2. Apply 5.5V at Vins 1 & 2. Measure both Vouts; they should read 0V. If desired, one can measure the shutdown supply current at this point. The supply current will be less than 15 uA in shutdown.

3. Turn on Vout1 and Vout2 by shifting shunts XJP1 and XJP2 from the OFF positions to the ON positions. Both output voltages should be within a tolerance of +/- 2%.

4. Vary the input voltages from 5.8V (the min. Vin is dependent on Vout) to 20V, and the load currents from 0 to 3A. Both output voltages should be within +/- 3% tolerance.

5. Set the load current of both outputs to 3A and the input voltages to 20V, and then measure each output ripple voltage (refer to figure 2 for proper measurement technique); they should each measure less than 30 mVAC. Also, observe the voltage waveform at either switch node (pins 23 & 24 for reg.1 and 13 & 14 for reg.2) of each regulator. The switching frequencies should be between 800 kHz and 1.2 MHz ($T = 1.25 \mu\text{s}$ and $0.833 \mu\text{s}$). To attain 2 MHz operation, change the shunt position on header JP14. In all cases, both switch node waveforms should be rectangular in shape, and 180° out-of-phase with each other. Change the shunt position on header JP11 to set the switch waveforms in phase with respect to each other. To operate the ckt.s in Burst Mode™, change the shunt in header JP8 to the Burst Mode™ position. When finished, insert shunts XJP1 and XJP2 to the OFF position(s) and disconnect the power.

6. Regulators 1 (VIN1) and 2 (VIN2) are completely separated from each other; thus, they can be powered from different individual input supplies, as can the signal input supply. Of course, all the voltage requirements still must be met: 1.5V to 20V for the PVin pins and 3.6V to 20V for the SVin pin.

Warning - If the power for the demo board is carried in long leads, the input voltage at the part could “ring”, which could affect the operation of the circuit or even exceed the maximum voltage rating of the IC. To eliminate the ringing, a small tantalum capacitor (for instance, AVX part # TPSY226M035R0200) is inserted on the pads between the input power and return terminals on the bottom of the demo board. The (greater) ESR of the tantalum capacitor will dampen the (possible) ringing voltage caused by the long input leads. On a normal, typical PCB, with short traces, this capacitor is not needed.

Table 1. Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITIONS	VALUE
Minimum Input Voltages		3.6V
Maximum Input Voltages		20V
Run	RUN Pin = GND	Shutdown
	RUN Pin = VIN	Operating
Output Voltage V _{OUT1} Regulation	VIN1 = 3.6V to 20V, I _{OUT1} = 0A to 3A	1.5V ±3% (1.455V - 1.545V)
		1.8V ±3% (1.746V - 1.854V)
		2.5V ±3% (2.425V - 2.575V)
Typical Output Ripple V _{OUT1}	VIN1 = 12V, I _{OUT1} = 3A (20 MHz BW)	< 30mV _{p-p}
Output Voltage V _{OUT2} Regulation	VIN2 = 3.6V to 20V, I _{OUT2} = 0A to 3A	2.5V ±3% (2.425V - 2.575V)
		3.3V ±3% (3.201V - 3.399V)
		5V ±3% (4.85V - 5.15V)
Typical Output Ripple V _{OUT2}	VIN2 = 12V, I _{OUT2} = 3A (20 MHz BW)	< 30mV _{p-p}
Nominal Switching Frequencies	RT Pin connected to 32k	1 MHz
	RT Pin = INTV _{CC}	2 MHz
Burst Mode™ Operation Output Current Thresholds	Channel 1: Vin = 12V, Vout1 = 1.8V, Fsw = 1 MHz	I _{out1} < 1.5A
	Channel 2: Vin = 12V, Vout2 = 3.3V, Fsw = 1 MHz	I _{out2} < 1.25A
	Channel 1: Vin = 12V, Vout1 = 1.8V, Fsw = 2 MHz	I _{out1} < 1A
	Channel 2: Vin = 12V, Vout2 = 3.3V, Fsw = 2 MHz	I _{out2} < 0.75 A
Phase	Phase Pin = INTV _{CC}	Out-of-Phase
	Phase Pin = GND	In Phase
INTV _{CC}		3.3V ±6%

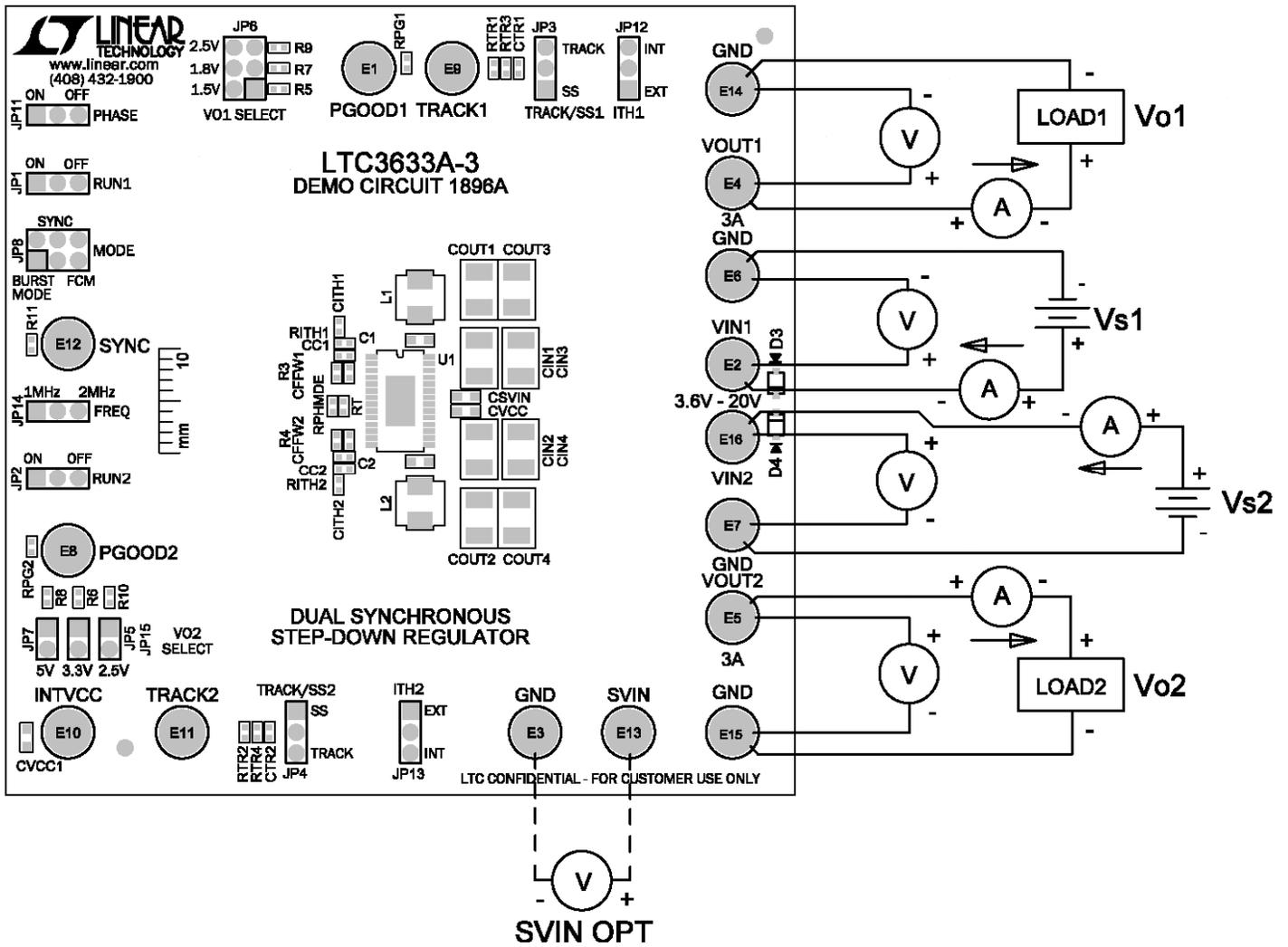


Figure 1. Proper Measurement Equipment Setup

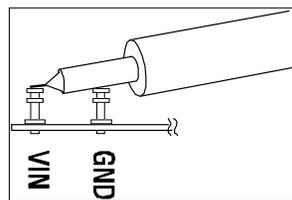


Figure 2. Measuring Input or Output Ripple

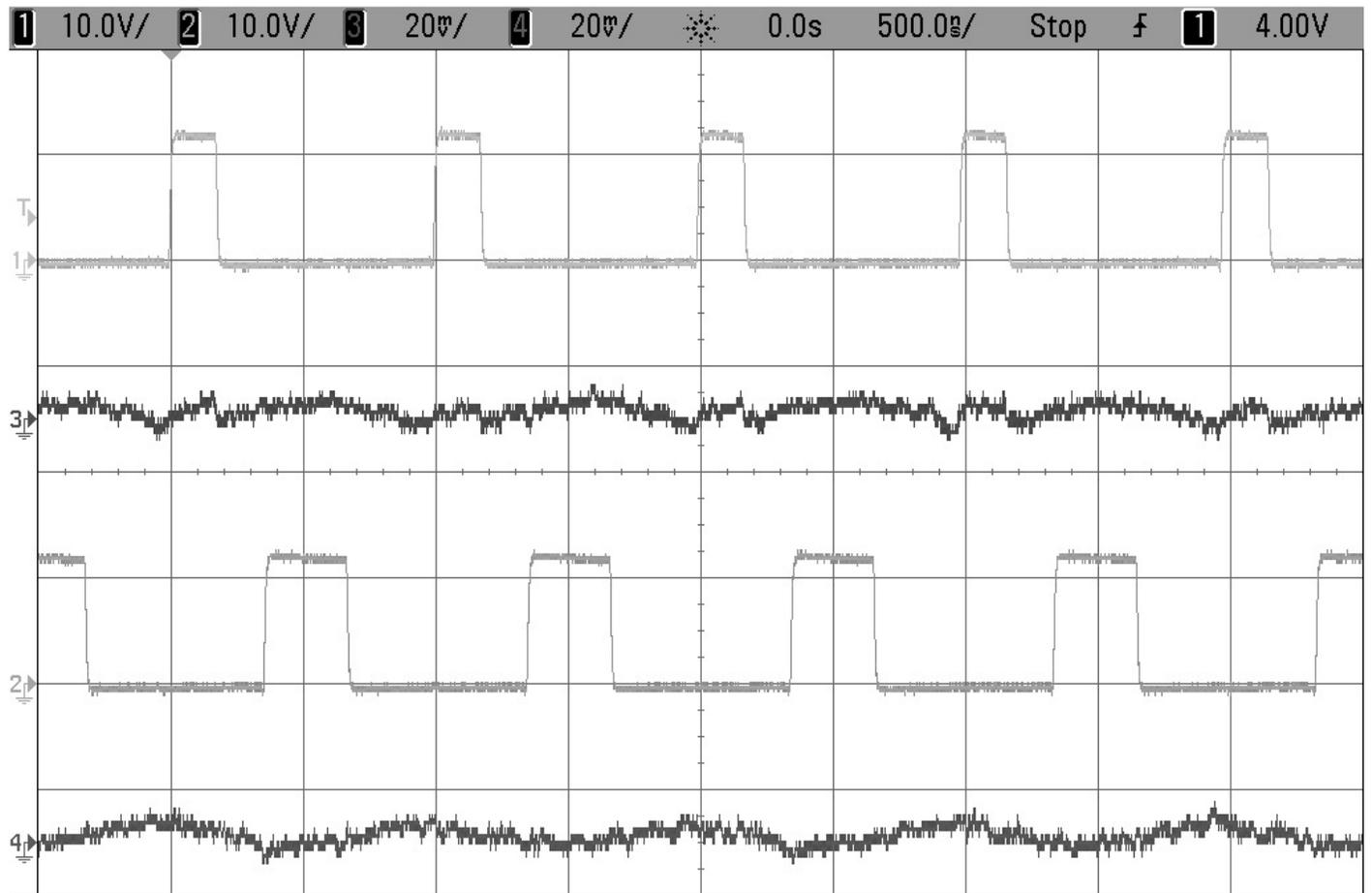


Figure 3. LTC3633A-3 DC1896 Switch Operation

$V_{IN1\&2} = 12V$, $V_{OUT1} = 1.8V @ I_{OUT1} = 3A$, $V_{OUT2} = 3.3V @ I_{OUT2} = 3A$

Forced Continuous Mode $F_{SW} = 1\text{ MHz}$

External Compensation: $R_{ithx} = 13k$, $C_{ithx} = 220\text{ pF}$

Trace 1: V_{SW1} (10V/div)

Trace 3: V_{OUT1} AC Voltage (20mV/div AC)

Trace 2: V_{SW2} (10V/div)

Trace 4: V_{OUT2} AC Voltage (20mV/div AC)

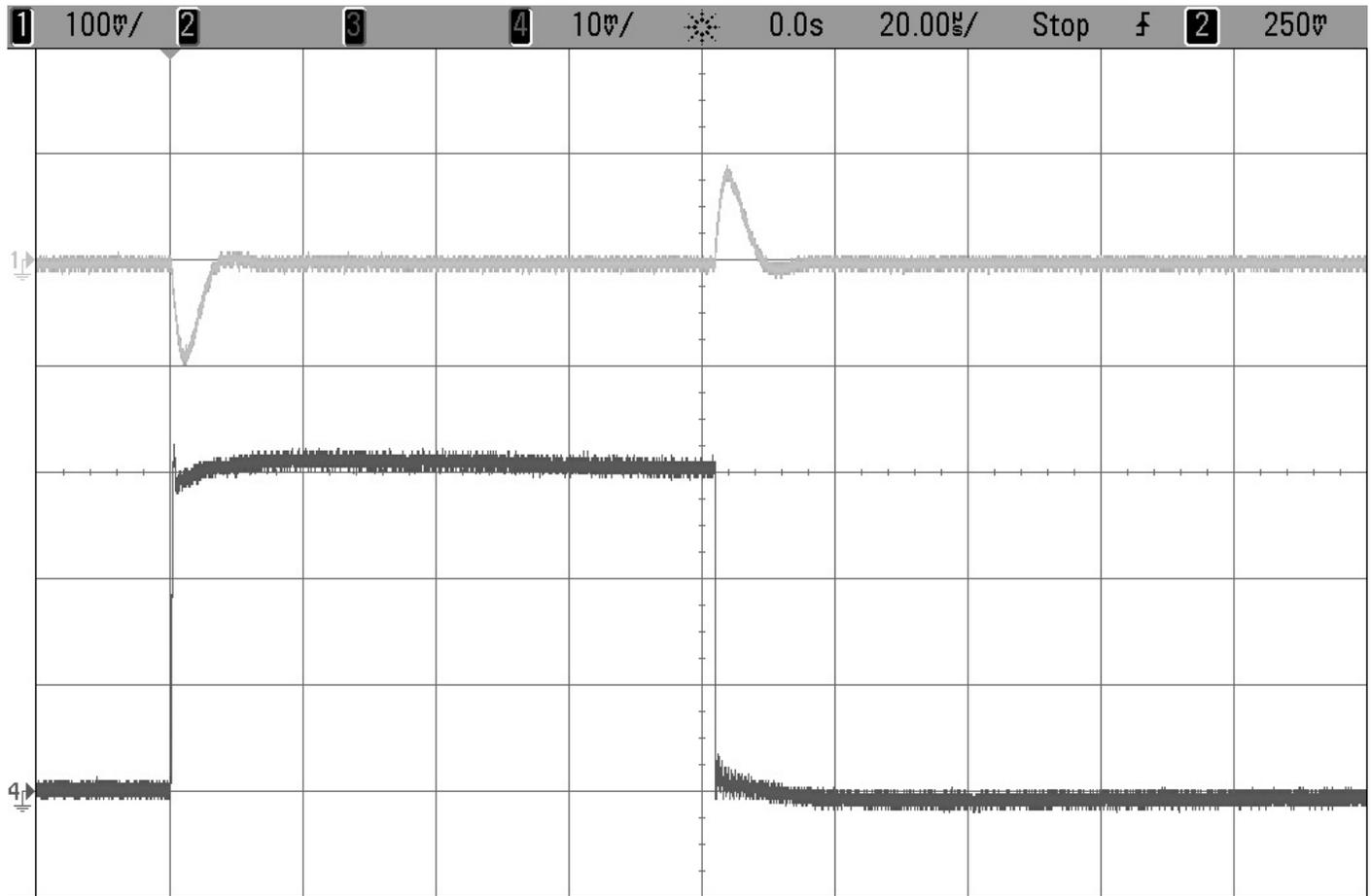


Figure 4. V_{OUT1} Load Step Response

$V_{IN1} = 12V$, $V_{OUT1} = 1.8V$, 3A Load Step (0A \leftrightarrow 3A)

Forced Continuous Mode $F_{SW} = 1\text{ MHz}$

External Compensation: $R_{ith1} = 13k$, $C_{ith1} = 220\text{ pF}$

Trace 1: Output Voltage (100mV/div AC)

Trace 4: Output Current (1A/div)

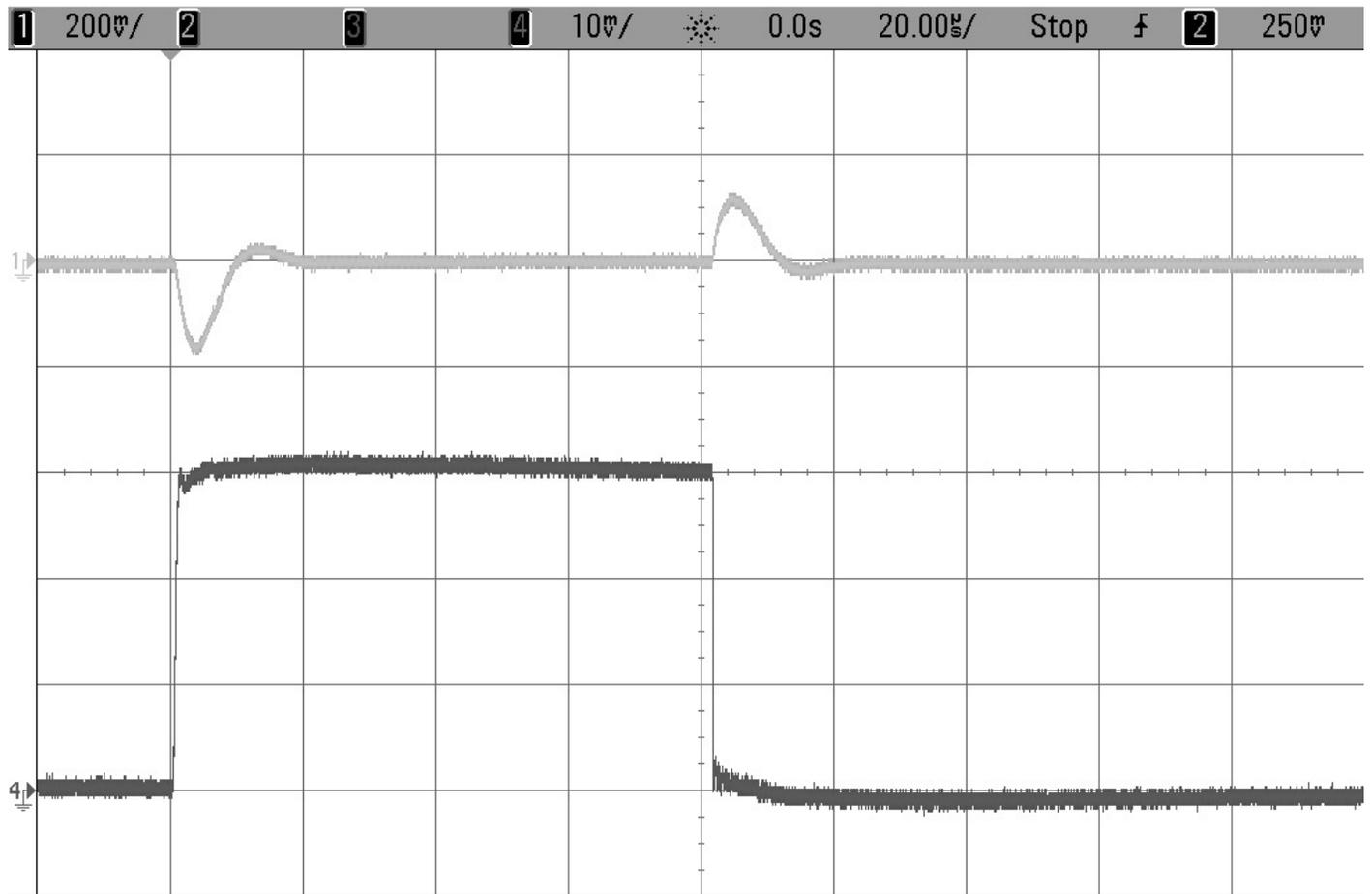


Figure 5. V_{OUT2} Load Step Response

$V_{IN2} = 12V$, $V_{OUT2} = 3.3V$, 3A Load Step (0A \leftrightarrow 3A)

Forced Continuous Mode $F_{SW} = 1\text{ MHz}$

External Compensation: $R_{ith2} = 13k$, $C_{ith2} = 220\text{ pF}$

Trace 1: Output Voltage (200mV/div AC)

Trace 4: Output Current (1A/div)

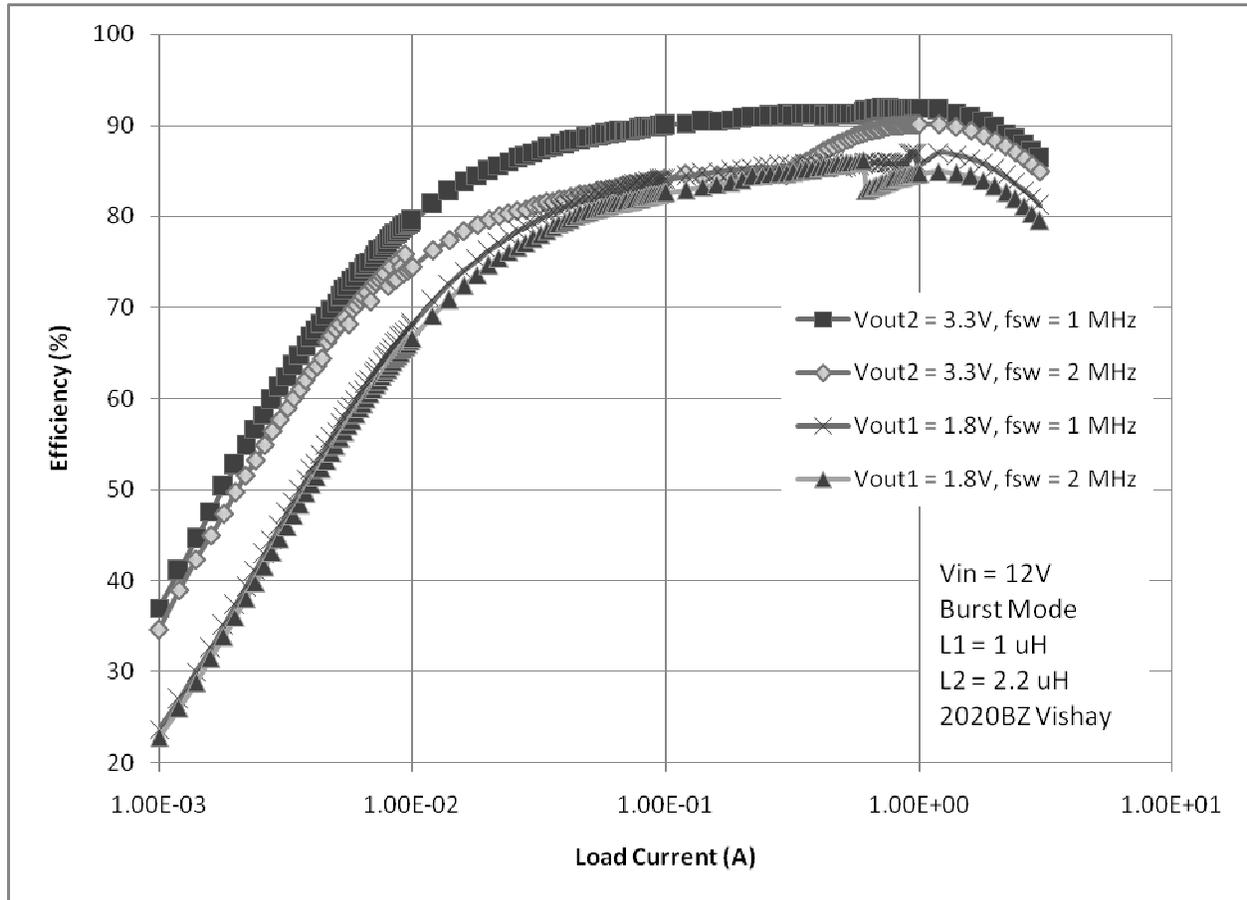
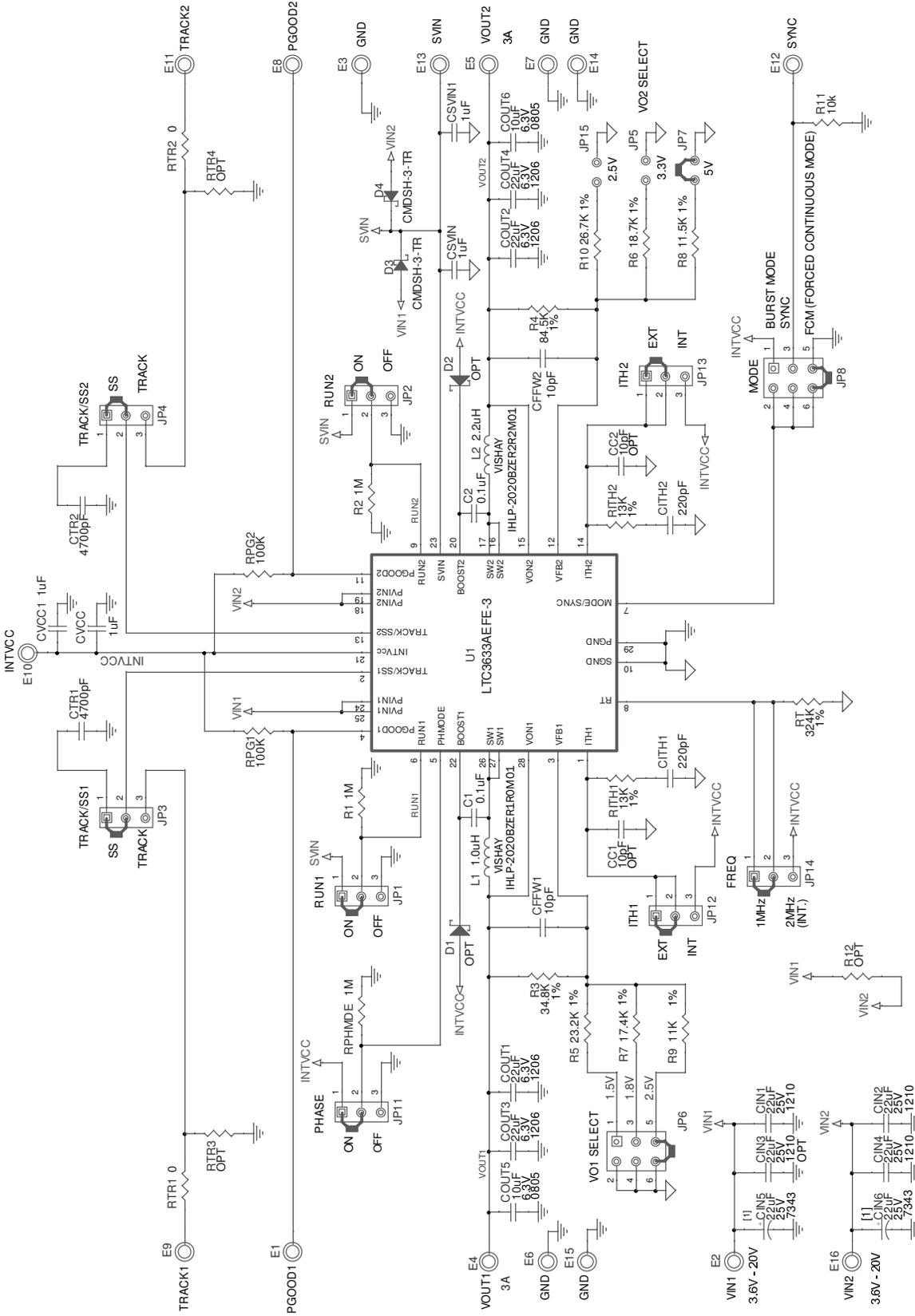


Figure 6. LTC3633A-3 DC1896 Efficiency



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TITLE: SCHEMATIC DUAL SYNCHRONOUS STEP-DOWN REGULATOR IC NO. LTC3633AEFE-3 DEMO CIRCUIT 1896A		PCB DES. JMI APP ENG. TOM G.	REV. 1 SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED,
 [1] CIN5 AND CIN6 ARE INSERTED ON DC1896A TO DAMPEN THE (POSSIBLE) RINGING VOLTAGE DUE TO THE USE OF LONG INPUT LEADS ON A NORMAL, TYPICAL PCB, WITH SHORT TRACES.
 CIN5 AND CIN6 ARE NOT NEEDED.