

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## General Description

The MAX8550A integrates a synchronous-buck PWM controller to generate  $V_{DDQ}$ , a sourcing and sinking LDO linear regulator to generate  $V_{TT}$ , and a 10mA reference output buffer to generate  $V_{TTR}$ . The buck controller drives two external n-channel MOSFETs to generate output voltages down to 0.7V from a 2V to 28V input with output currents up to 15A. The LDO can sink or source up to 1.5A continuous and 3A peak current. Both the LDO output and the 10mA reference buffer output can be made to track the  $V_{REFIN}$  voltage. These features make the MAX8550A ideally suited for DDR memory applications in desktops, notebooks, and graphic cards.

The PWM controller in the MAX8550A utilizes Maxim's proprietary Quick-PWM™ architecture with programmable switching frequencies of up to 600kHz. This control scheme handles wide input/output voltage ratios with ease and provides 100ns response to load transients while maintaining high efficiency and a relatively constant switching frequency. The MAX8550A offers fully programmable UVP/OVP and skip-mode options ideal in portable applications. Skip mode allows for improved efficiency at lighter loads.

The  $V_{TT}$  and  $V_{TTR}$  outputs track to within 1% of  $V_{REFIN} / 2$ . The high bandwidth of this LDO regulator allows excellent transient response without the need for bulk capacitors, thus reducing cost and size.

The buck controller and LDO regulators are provided with independent current limits. Adjustable lossless foldback current limit for the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low-side MOSFET. Additionally, overvoltage and undervoltage protection mechanisms are built in. Once the overcurrent condition is removed, the regulator is allowed to enter soft-start again. This helps minimize power dissipation during a short-circuit condition. The MAX8550A allows flexible sequencing and standby power management using the SHDN and STBY inputs, which support all DDRs' operating states.

The MAX8550A is available in a small 5mm × 5mm, 28-pin thin QFN package.

## Applications

- DDR I and DDR II Memory Power Supplies
- Desktop Computers
- Notebooks and Desknotes
- Graphic Cards
- Game Consoles
- RAID
- Networking

## Features

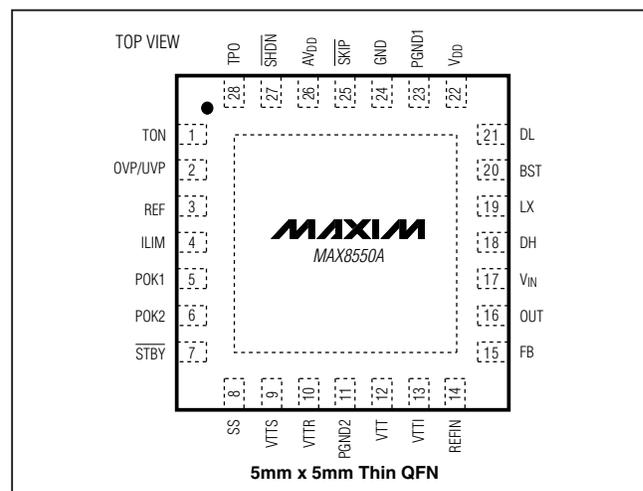
### Buck Controller

- ◆ Quick-PWM with 100ns Load-Step Response
- ◆ Up to 95% Efficiency
- ◆ 2V to 28V Input Voltage Range
- ◆ 1.8V/2.5V Fixed or 0.7V to 5.5V Adjustable Output
- ◆ Up to 600kHz Selectable Switching Frequency
- ◆ Programmable Current Limit with Foldback Capability
- ◆ 1.7ms Digital Soft-Start
- ◆ Independent Shutdown and Standby Controls
- ◆ Overvoltage/Undervoltage-Protection Option
- ◆ Power-Good Window Comparator LDO Section
- ◆ Fully Integrated  $V_{TT}$  and  $V_{TTR}$  Capability
- ◆  $V_{TT}$  Has  $\pm 3A$  Sourcing/Sinking Capability
- ◆  $V_{TT}$  and  $V_{TTR}$  Outputs Track  $V_{REFIN} / 2$
- ◆ All-Ceramic Output-Capacitor Designs
- ◆ 1.0V to 2.8V Input Voltage Range
- ◆ Power-Good Window Comparator

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8550AETI	-40°C to +85°C	28 TQFN 5mm × 5mm

## Pin Configuration



Typical Operating Circuit appears at end of data sheet.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

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## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$ to GND	-0.3V to +30V	$V_{TTS}$ to GND	-0.3V to ( $AV_{DD}$ + 0.3V)
$V_{DD}$ , $AV_{DD}$ , $V_{TTI}$ to GND	-0.3V to +6V	PGND1, PGND2, TP0 to GND	-0.3V to +0.3V
$\overline{SHDN}$ , REFIN to GND	-0.3V to +6V	REF Short Circuit to GND	Continuous
SS, POK1, POK2, SKIP, ILIM, FB to GND	-0.3V to +6V	Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
$\overline{STBY}$ , TON, REF, UVP/OVP to GND	-0.3V to ( $AV_{DD}$ + 0.3V)	28-Pin 5mm x 5mm TQFN (derate 35.7mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$ )	2.86W
OUT, VTTR to GND	-0.3V to ( $AV_{DD}$ + 0.3V)	Operating Temperature Range	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
DL to PGND1	-0.3V to ( $V_{DD}$ + 0.3V)	Junction Temperature	+150 $^\circ\text{C}$
DH to LX	-0.3V to ( $V_{BST}$ + 0.3V)	Storage Temperature Range	-65 $^\circ\text{C}$ to +165 $^\circ\text{C}$
LX to BST	-6V to +0.3V	Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$
LX to GND	-2V to +30V		
VTT to GND	-0.3V to ( $V_{TTI}$ + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = +15\text{V}$ ,  $V_{DD} = AV_{DD} = V_{\overline{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5\text{V}$ ,  $V_{OUT} = V_{REFIN} = V_{TTI} = 2.5\text{V}$ , UVP/OVP = TP0 = FB =  $\overline{SKIP}$  = GND, PGND1 = PGND2 = LX = GND, TON = OPEN,  $V_{TTS} = V_{TT}$ ,  $T_A = -40^\circ\text{C}$  to +85 $^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>MAIN PWM CONTROLLER</b>							
Input Voltage Range	$V_{IN}$		2		28	V	
	$V_{DD}$ , $AV_{DD}$		4.5		5.5		
Output Adjust Range	$V_{OUT}$		0.7		5.5	V	
Output Voltage Accuracy (Note 2)		FB = OUT	0.693	0.7	0.707	V	
		FB = GND	2.47	2.5	2.53		
		FB = $V_{DD}$	1.78	1.8	1.82		
Soft-Start Ramp Time	$t_{SS}$	Rising edge of $\overline{SHDN}$ to full current limit		1.7		ms	
On-Time	$t_{ON}$	$V_{IN} = 15\text{V}$ , $V_{OUT} = 1.5\text{V}$ (Note 3)	TON = GND (600kHz)	170	194	219	ns
			TON = REF (450kHz)	213	243	273	
			TON = OPEN (300kHz)	316	352	389	
			TON = $AV_{DD}$ (200kHz)	461	516	571	
Minimum Off-Time	$t_{OFF\_MIN}$	(Note 3)	200	300	450	ns	
$V_{IN}$ Quiescent Supply Current	$I_{IN}$			25	40	$\mu\text{A}$	
$V_{IN}$ Shutdown Supply Current		$\overline{SHDN} = \text{GND}$		1	5	$\mu\text{A}$	
$AV_{DD}$ Quiescent Supply Current	$I_{AVDD}$	All on (PWM, VTT, and VTTR on)		2.5	5	mA	
		$\overline{STBY} = \text{GND}$ (only VTTR and PWM on)		1	2		
$AV_{DD} + V_{DD}$ Shutdown Supply Current		$\overline{SHDN} = \text{GND}$		2	10	$\mu\text{A}$	
$AV_{DD}$ Undervoltage-Lockout Threshold		Rising edge of $V_{IN}$	4.05	4.25	4.40	V	
		Hysteresis		50		mV	
$V_{DD}$ Quiescent Supply Current	$I_{VDD}$	Set $V_{FB} = 0.8\text{V}$		1	5	$\mu\text{A}$	

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = +15V$ ,  $V_{DD} = AV_{DD} = V_{\overline{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V$ ,  $V_{OUT} = V_{REFIN} = V_{VTT1} = 2.5V$ ,  $UVP/OVP = TP0 = FB = \overline{SKIP} = GND$ ,  $PGND1 = PGND2 = LX = GND$ ,  $TON = OPEN$ ,  $V_{VTT5} = V_{VTT}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>REFERENCE</b>						
Reference Voltage	$V_{REF}$	$AV_{DD} = 4.5V$ to $5.5V$ ; $I_{REF} = 0$	1.98	2	2.02	V
Reference Load Regulation		$I_{REF} = 0$ to $50\mu A$			0.01	V
REF Undervoltage Lockout		$V_{REF}$ rising		1.93		V
		Hysteresis		300		mV
<b>FAULT DETECTION</b>						
OVP Trip Threshold (Referred to Nominal $V_{OUT}$ )		$UVP/OVP = AV_{DD}$ (Note 4)	112	116	120	%
UVP Trip Threshold (Referred to Nominal $V_{OUT}$ )			65	70	75	%
POK1 Trip Threshold (Referred to Nominal $V_{OUT}$ )		Lower level, falling edge, 1% hysteresis	87	90	93	%
		Upper level, rising edge, 1% hysteresis	107	110	113	
POK2 Trip Threshold (Referred to Nominal $V_{VTT5}$ and $V_{VTT1}$ )		Lower level, falling edge, 1% hysteresis	87.5	90	92.5	%
		Upper level, rising edge, 1% hysteresis	107.5	110	112.5	
POK2 Disable Threshold (Measured at $REFIN$ )		$V_{REFIN}$ rising (hysteresis = $75mV$ typ)	0.7		0.9	V
UVP Blanking Time		From rising edge of $\overline{SHDN}$	10	20	40	ms
OVP, UVP, POK_ Propagation Delay				10		$\mu s$
POK_ Output Low Voltage		$I_{SINK} = 4mA$			0.3	V
POK_ Leakage Current		$V_{POK_} = 5.5V$ , $V_{FB} = 0.8V$ , $V_{VTT5} = 1.3V$			1	$\mu A$
ILIM Adjustment Range	$V_{ILIM}$		0.25		2.00	V
ILIM Input Leakage Current					0.1	$\mu A$
Current-Limit Threshold (Fixed) PGND1 to LX			45	50	55	mV
Current-Limit Threshold (Adjustable) PGND1 to LX		$V_{ILIM} = 2V$	170	200	235	mV
Current-Limit Threshold (Fixed, Negative Direction) PGND1 to LX		$\overline{SKIP} = AV_{DD}$	-75	-60	-45	mV
Current-Limit Threshold (Adjustable, Negative Direction) PGND1 to LX		$\overline{SKIP} = AV_{DD}$ , $V_{ILIM} = 2V$		-250		mV
Zero-Crossing Detection Threshold PGND1 to LX				3		mV
Thermal-Shutdown Threshold				+160		$^{\circ}C$
Thermal-Shutdown Hysteresis				15		$^{\circ}C$

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = +15V$ ,  $V_{DD} = AV_{DD} = V_{SHDN} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V$ ,  $V_{OUT} = V_{REFIN} = V_{VTTI} = 2.5V$ ,  $UVP/OVP = TP0 = FB = \overline{SKIP} = GND$ ,  $PGND1 = PGND2 = LX = GND$ ,  $TON = OPEN$ ,  $V_{VTTs} = V_{VTT}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>MOSFET DRIVERS</b>						
DH Gate-Driver On-Resistance		$V_{BST} - V_{LX} = 5V$		1	4	$\Omega$
DL Gate-Driver On-Resistance in High State				1	4	$\Omega$
DL Gate-Driver On-Resistance in Low State				0.5	3	$\Omega$
Dead Time (Additional to Adaptive Delay)		DH falling to DL rising		30		ns
		DL falling to DH rising		30		
<b>INPUTS AND OUTPUTS</b>						
Logic Input Threshold (SHDN, STBY, SKIP)		Rising edge	1.20	1.7	2.20	V
		Hysteresis		225		mV
Logic Input Current (SHDN, STBY, SKIP)			-1		+1	$\mu A$
Dual-Mode™ Input Logic Levels (FB)		Low (2.5V output)			0.05	V
		High (1.8V output)	2.1			
Input Bias Current (FB)			-0.1		+0.1	$\mu A$
Four-Level Input Logic Levels (TON, OVP/UVP)		High	$AV_{DD} - 0.4$			V
		Floating	3.15		3.85	
		REF	1.65		2.35	
		Low			0.5	
Logic Input Current (TON, OVP/UVP)			-3		+3	$\mu A$
OUT Input Resistance		FB = GND	90	175	350	k $\Omega$
		FB = $AV_{DD}$	70	135	270	
		FB adjustable mode	400	800	1600	
OUT Discharge-Mode On-Resistance				10	25	$\Omega$
DL Turn-On Level During Discharge Mode (Measured at OUT)			0.01	0.1	0.20	V

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = +15V$ ,  $V_{DD} = AV_{DD} = \overline{V_{SHDN}} = \overline{STBY} = V_{BST} = V_{ILIM} = 5V$ ,  $V_{OUT} = V_{REFIN} = V_{VTTI} = 2.5V$ ,  $UVP/OVP = TP0 = FB = \overline{SKIP} = GND$ ,  $PGND1 = PGND2 = LX = GND$ ,  $TON = OPEN$ ,  $V_{VTTS} = V_{VTT}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LINEAR REGULATORS (VTTR AND VTT)</b>						
VTTI Input Voltage Range	$V_{VTTI}$		1		2.8	V
VTTI Supply Current	$I_{VTTI}$	$I_{VTT} = I_{VTTR} = 0$		<0.1	1	mA
VTTI Shutdown Current		$\overline{SHDN} = GND$			10	$\mu A$
REFIN Input Impedance		$V_{REFIN} = 2.5V$	12	20	30	k $\Omega$
REFIN Range	$V_{REFIN}$		1		2.8	V
VTT, VTTR UVLO Threshold (Measured at OUT)			0.01	0.1	0.20	V
Soft-Start Charge Current	$I_{SS}$	$V_{SS} = 0$		4		$\mu A$
VTT Internal MOSFET High-Side On-Resistance		$I_{VTT} = -100mA$ , $V_{VTTI} = 1.5V$ , $AV_{DD} = 4.5V$			0.3	$\Omega$
VTT Internal MOSFET Low-Side On-Resistance		$I_{VTT} = 100mA$ , $AV_{DD} = 4.5V$			0.3	$\Omega$
VTT Output Accuracy (Referred to $V_{REFIN} / 2$ )		$V_{REFIN} = 1.5V$ or $2.5V$ , $I_{VTT} = 1mA$	-1		+1	%
VTT Load Regulation		$V_{REFIN} = 2.5V$ , $I_{VTT} = 0$ to $\pm 1.5A$		1		%
		$V_{REFIN} = 1.5V$ , $I_{VTT} = 0$ to $\pm 1A$		1		
VTT Current Limit		$V_{TT} = 0$ or $V_{TTI}$	$\pm 3$	$\pm 5$	$\pm 6.5$	A
VTTS Input Current	$I_{VTTS}$	$V_{VTTS} = 1.5V$ , VTT open		0.1	1	$\mu A$
VTTR Output Error (Referred to $V_{REFIN} / 2$ )		$V_{REFIN} = 1.5V$ or $2.5V$ , $I_{VTTR} = 0$	-1		+1	%
VTTR Current Limit		$V_{VTTR} = 0$ or $V_{VTTI}$	$\pm 18$	$\pm 32$	$\pm 50$	mA

**Note 1:** Specifications to  $-40^{\circ}C$  are guaranteed by design, not production tested.

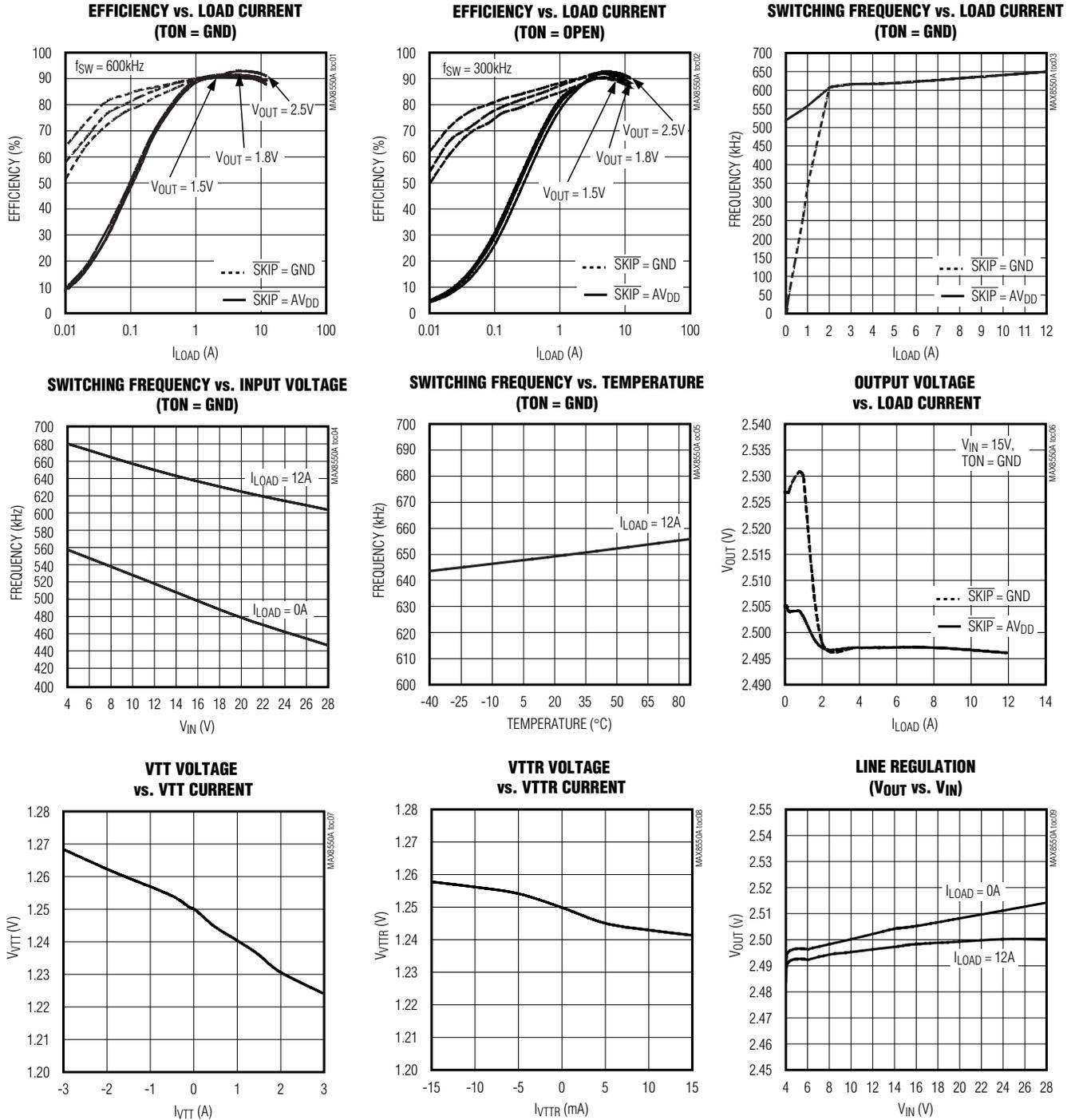
**Note 2:** When the inductor is in continuous conduction, the output voltage has a DC regulation level higher than the error-comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage has a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

**Note 3:** On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with  $LX = GND$ ,  $V_{BST} = 5V$ , and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Typical Operating Characteristics

( $V_{IN} = 12V$ ,  $V_{OUT} = 2.5V$ ,  $T_{ON} = GND$ ,  $SKIP = AV_{DD}$ , circuit of Figure 8,  $T_A = +25^\circ C$ , unless otherwise noted.)

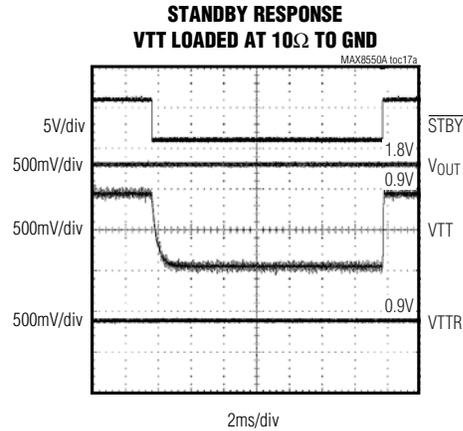
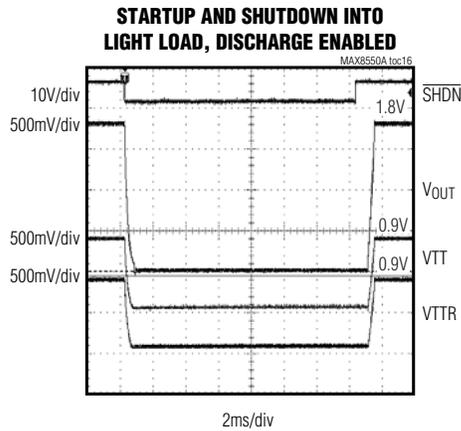
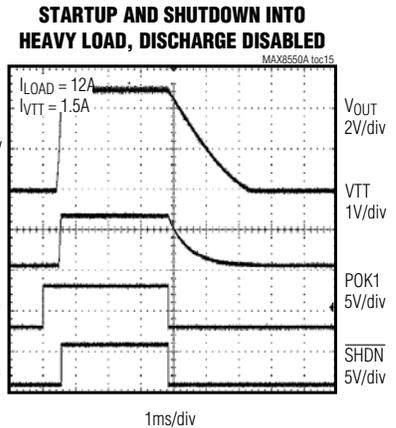
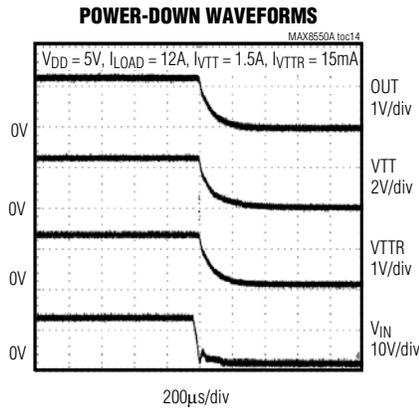
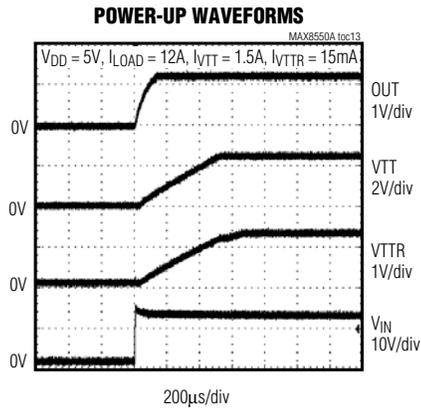
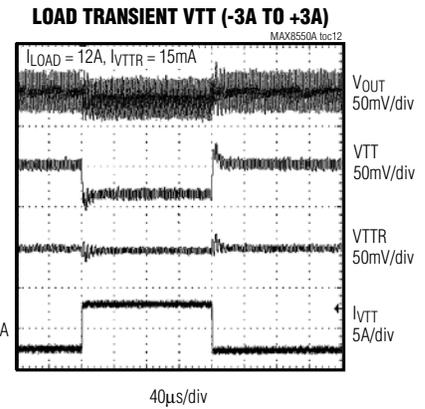
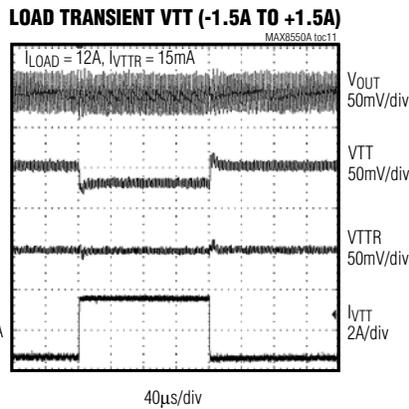
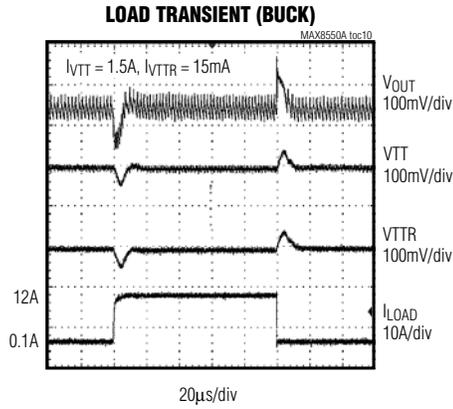


# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Typical Operating Characteristics (continued)

( $V_{IN} = 12V$ ,  $V_{OUT} = 2.5V$ ,  $T_{ON} = GND$ ,  $SKIP = AV_{DD}$ , circuit of Figure 8,  $T_A = +25^\circ C$ , unless otherwise noted.)

**MAX8550A**

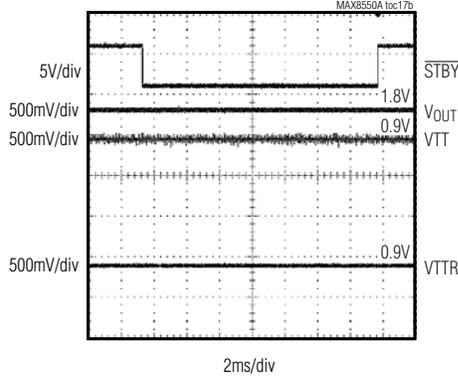


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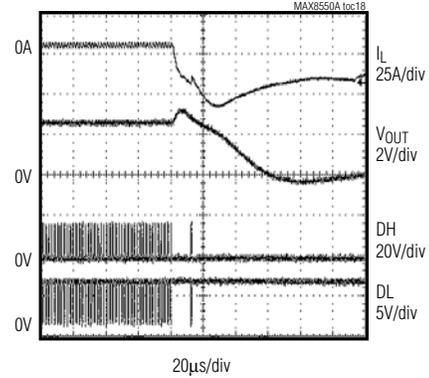
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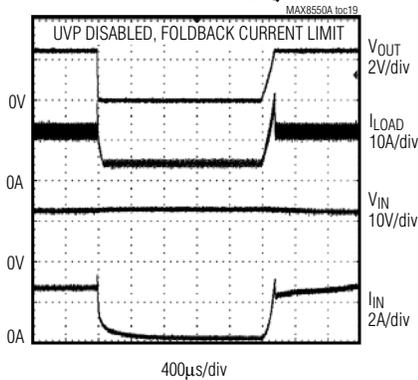
**STANDBY RESPONSE, VTT AT NO LOAD**



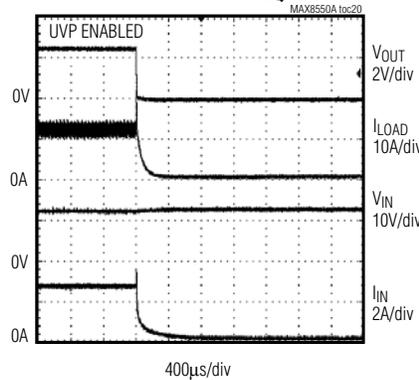
**OVERVOLTAGE AND TURN-OFF OF BUCK OUTPUT**



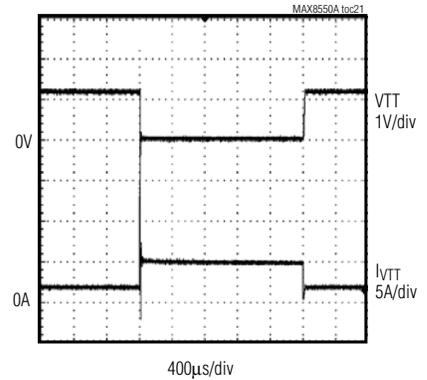
**SHORT CIRCUIT AND RECOVERY OF VDDQ**



**SHORT CIRCUIT AND RECOVERY OF VDDQ**



**SHORT CIRCUIT OF VTT**



# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Pin Description

**MAX8550A**

PIN	NAME	FUNCTION
1	TON	On-Time Selection-Control Input. This four-level logic input sets the nominal DH on-time. Connect to GND, REF, AV <sub>DD</sub> , or leave TON unconnected to select the following nominal switching frequencies: TON = AV <sub>DD</sub> (200kHz) TON = OPEN (300kHz) TON = REF (450kHz) TON = GND (600kHz)
2	OVP/ UVP	Overvoltage/Undervoltage-Protection Control Input. This four-level logic input enables or disables the overvoltage and/or undervoltage protection. The overvoltage limit is 116% of the nominal output voltage. The undervoltage limit is 70% of the nominal output voltage. Discharge mode is enabled when OVP is also enabled. Connect the OVP/UVP pin to the following pins for the desired function: OVP/UVP = AV <sub>DD</sub> (Enable OVP and discharge mode, enable UVP.) OVP/UVP = OPEN (Enable OVP and discharge mode, disable UVP.) OVP/UVP = REF (Disable OVP and discharge mode, enable UVP.) OVP/UVP = GND (Disable OVP and discharge mode, disable UVP.)
3	REF	+2.0V Reference Voltage Output. Bypass to GND with a 0.1μF (min) capacitor. REF can supply 50μA for external loads. Can be used for setting voltage for ILIM. REF turns off when $\overline{\text{SHDN}}$ is low and $\text{OUT} < 0.1\text{V}$ .
4	ILIM	Valley Current-Limit Threshold Adjustment for Buck Regulator. The current-limit threshold across PGND and LX is 0.1 times the voltage at ILIM. Connect ILIM to a resistive divider, typically from REF to GND, to set the current-limit threshold between 25mV and 200mV. This corresponds to a 0.25V to 2V range at ILIM. Connect ILIM to AV <sub>DD</sub> to select the 50mV default current-limit threshold. See the <i>Setting the Current Limit</i> section.
5	POK1	Buck Power-Good Open-Drain Output. POK1 is low when the buck output voltage is more than 10% above or below the normal regulation point or during soft-start. POK1 is high impedance when the output is in regulation and the soft-start circuit has terminated. POK1 is low in shutdown.
6	POK2	LDO Power-Good Open-Drain Output. In normal mode, POK2 is low when either VTTR or VTTS is more than 10% above or below the normal regulation point, which is typically $\text{REFIN} / 2$ . In standby mode, POK2 responds only to the VTTR input. POK2 is low in shutdown, and when $\text{VREFIN}$ is less than 0.8V.
7	$\overline{\text{STBY}}$	Standby. Connect to GND for low-quiescent mode where the VTT output is open circuit. POK2 takes input from only VTTR in this mode. PWM output can be on or off, depending on the state of SHDN.
8	SS	Soft-Start Control for VTT. Connect a capacitor (C9 in the <i>Typical Applications Circuit</i> ) from SS to ground (see the <i>Soft-Start Capacitor Selection</i> section). Leave SS open to disable soft-start. SS discharges to ground when VTT is off. See the <i>POR, UVLO, and Soft-Start</i> section.
9	VTTS	Sensing Pin for Termination Supply Output. Normally connected to VTT pin to allow accurate regulation to half the REFIN voltage. Connected to a resistive divider from VTT to GND to regulate VTT to higher than half the REFIN voltage.
10	VTTR	Termination Reference Voltage. VTTR tracks $\text{VREFIN} / 2$ .

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## Pin Description (continued)

PIN	NAME	FUNCTION
11	PGND2	Power Ground for VTT and VTTR. Connect PGND2 externally to the underside of the exposed pad.
12	VTT	Termination Power-Supply Output. Connect VTT to VTTS to regulate to $V_{REFIN} / 2$ .
13	VTTI	Power-Supply Input Voltage for VTT and VTTR. Normally connected to the output of the buck regulator for DDR application.
14	REFIN	External Reference Input. This is used to regulate the VTT and VTTR outputs to $V_{REFIN} / 2$ .
15	FB	Feedback Input for Buck Output. Connect to $AV_{DD}$ for a +1.8V fixed output or to GND for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB to a resistive divider from the output voltage. FB regulates to +0.7V.
16	OUT	Output-Voltage Sense Connection. Connect to the positive terminal of the buck output filter capacitor. OUT senses the output voltage to determine the on-time for the high-side switching MOSFET (Q1 in the <i>Typical Applications Circuit</i> ). OUT also serves as the buck output's feedback input in fixed-output modes. When discharge mode is enabled by OVP/UVLP, the output capacitor is discharged through an internal $10\Omega$ resistor connected between OUT and GND. OUT also acts as the input to the VTT and VTTR UVLO detector.
17	$V_{IN}$	Input-Voltage Sense Connection. Connect to input power source. $V_{IN}$ is used only to set the PWM's on-time one-shot timer. IN voltage range is from 2V to 28V.
18	DH	High-Side Gate-Driver Output. Swings from LX to BST. DH is low when in shutdown or UVLO.
19	LX	External Inductor Connection. Connect LX to the input side of the inductor. LX is used for both current limit and the return supply of the DH driver.
20	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to the <i>Typical Applications Circuit</i> (Figure 8). See the <i>Boost-Supply Diode and Capacitor Selection</i> section.
21	DL	Synchronous-Rectifier Gate-Driver Output. Swings from PGND to $V_{DD}$ .
22	$V_{DD}$	Supply Input for the DL Gate Drive. Connect to the +4.5V to +5.5V system supply voltage. Bypass to PGND1 with a $1\mu\text{F}$ (min) ceramic capacitor.
23	PGND1	Power Ground for Buck Controller. Connect PGND1 externally to the underside of the exposed pad.
24	GND	Analog Ground for Both Buck and LDO. Connect GND externally to the underside of the exposed pad.
25	$\overline{\text{SKIP}}$	Pulse-Skipping Control Input. Connect to $AV_{DD}$ for low-noise, forced-PWM mode. Connect to GND to enable pulse-skipping operation.
26	$AV_{DD}$	Analog Supply Input for Both Buck and LDO. Connect to the +4.5V to +5.5V system supply voltage with a series $10\Omega$ resistor. Bypass to GND with a $1\mu\text{F}$ or greater ceramic capacitor.
27	$\overline{\text{SHDN}}$	Shutdown Control Input. Use to control buck output. A rising edge on $\overline{\text{SHDN}}$ clears the overvoltage- and undervoltage-protection fault latches (see Tables 2 and 3). Connect to $AV_{DD}$ for normal operation.
28	TP0	This is a test pin. Must connect to GND externally.

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

MAX8550A

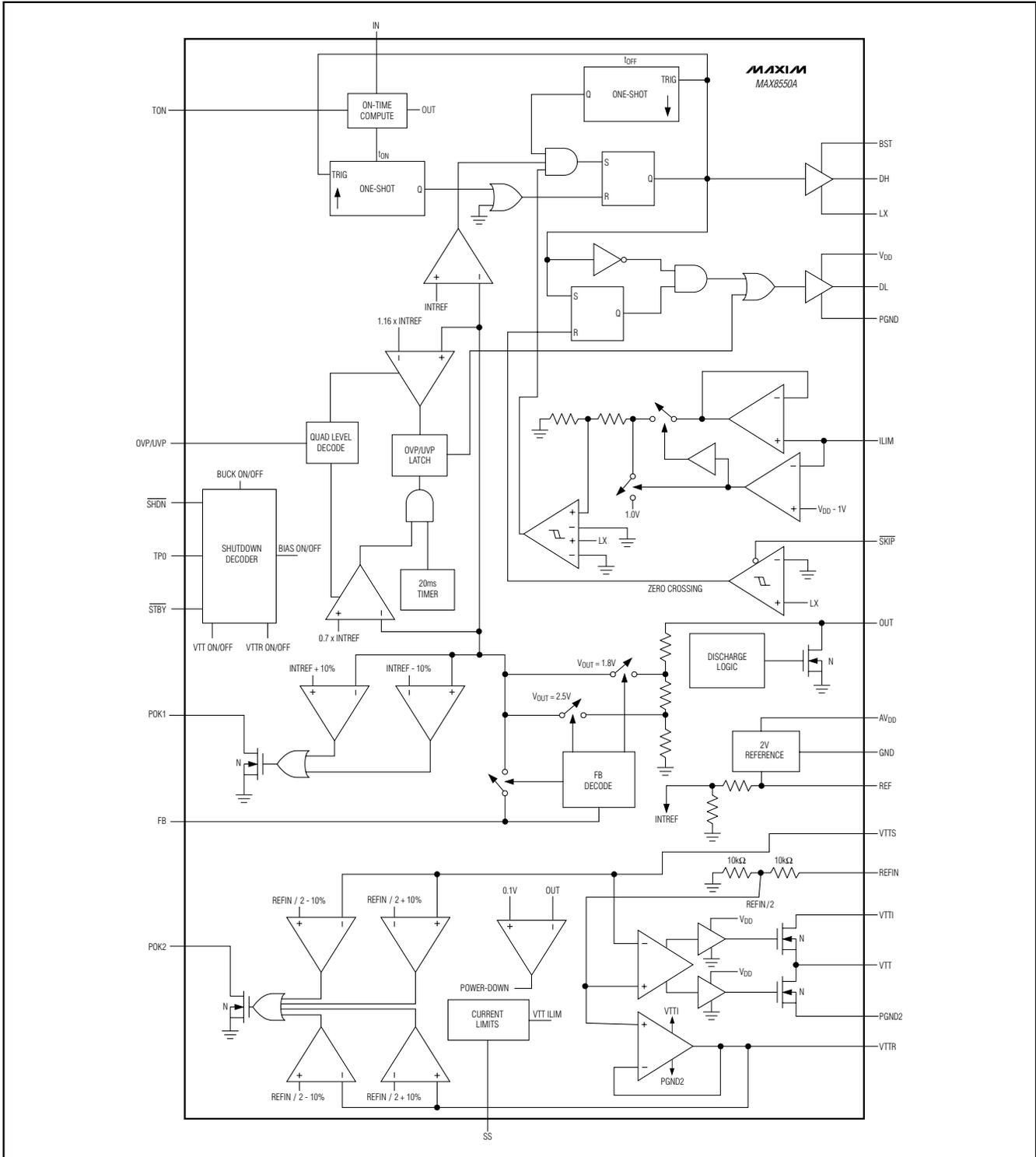


Figure 1. Functional Diagram

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Detailed Description

The MAX8550A combines a synchronous-buck PWM controller, an LDO linear regulator, and a 10mA reference output buffer. The buck controller drives two external n-channel MOSFETs to deliver load currents up to 12A and generate voltages down to 0.7V from a +2V to +28V input. The LDO linear regulator can sink and source up to 1.5A continuous and 3A peak current with relatively fast response. These features make the MAX8550/MAX8551 ideally suited for DDR memory applications.

The MAX8550A buck regulator is equipped with a fixed switching frequency of up to 600kHz using Maxim's proprietary constant on-time Quick-PWM architecture. This control scheme handles wide input/output voltage ratios with ease, and provides 100ns "instant-on" response to load transients, while maintaining high efficiency with relatively constant switching frequency.

The buck controller, LDO, and a reference output buffer are provided with independent current limits. Lossless foldback current limit in the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low-side FET. The ILIM input is used to adjust this current limit. Overvoltage protection, if selected, is achieved by latching the low-side synchronous FET on and the high-side FET off when the output voltage is over 116% of its set output. It also features an optional undervoltage protection by latching the MOSFET drivers to the OFF state during an overcurrent condition, when the output voltage is lower than 70% of the regulated output. This helps minimize power dissipation during a short-circuit condition.

The current limit in the LDO and buffered reference output buffer is  $\pm 5A$  and  $\pm 32mA$ , respectively, and neither have the over- or undervoltage protection. When the current limit in either output is reached, the output no longer regulates the voltage, but regulates the current to the value of the current limit.

### +5V Bias Supply ( $V_{DD}$ and $AV_{DD}$ )

The MAX8550A requires an external +5V bias supply in addition to the input voltage ( $V_{IN}$ ). Keeping the bias supply external to the IC improves the efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and the gate drivers. If stand-alone capability is needed, then the +5V supply can be generated with an external linear regulator such as the MAX1615.  $V_{DD}$ ,  $AV_{DD}$ , and  $I_N$  can be connected together if the input source is a fixed +4.5V to +5.5V supply.

$V_{DD}$  is the supply input for the buck regulator's MOSFET drivers, and  $AV_{DD}$  supplies the power for the rest of

the IC. The current from the  $AV_{DD}$  and  $V_{DD}$  power supply must supply the current for the IC and the gate drive for the MOSFETs. This maximum current can be estimated as:

$$I_{BIAS} = I_{VDD} + I_{AVDD} + f_{SW} \times (Q_{G1} + Q_{G2})$$

where  $I_{VDD} + I_{AVDD}$  are the quiescent supply currents into  $V_{DD}$  and  $AV_{DD}$ ,  $Q_{G1}$  and  $Q_{G2}$  are the total gate charges of MOSFETs Q1 and Q2 (at  $V_{GS} = 5V$ ) in the *Typical Applications Circuit*, and  $f_{SW}$  is the switching frequency.

### Free-Running Constant-On-Time PWM

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward (Figure 1). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to the output voltage. Another one-shot sets a minimum off-time of 300ns (typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

### On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to input and output voltages. The high-side switch on-time is inversely proportional to the input voltage ( $V_{IN}$ ) and is proportional to the output voltage:

$$t_{ON} = K \times \frac{(V_{OUT} + I_{LOAD} \times R_{DS(ON)Q2})}{V_{IN}}$$

where K (the switching period) is set by the TON input connection (Table 1) and  $R_{DS(ON)Q2}$  is the on-resistance of the synchronous rectifier (Q2) in the *Typical Applications Circuit* (Figure 8). This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold:

- 1) The frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band.
- 2) The inductor ripple-current operating point remains relatively constant, resulting in an easy design methodology and predictable output voltage ripple.

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* table (approximately  $\pm 12.5\%$  at 600kHz and 450kHz, and  $\pm 10\%$  at 200kHz and 300kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range. For example, the 600kHz setting typically runs approximately 10% slower with inputs much greater than 5V due to the very short on-times required.

The constant on-time translates only roughly to a constant switching frequency. The on-times guaranteed in the *Electrical Characteristics* table are influenced by resistive losses and by switching delays in the high-side MOSFET. Resistive losses, which include the inductor, both MOSFETs, the output capacitor's ESR, and any PC board copper losses in the output and ground, tend to raise the switching frequency as the load increases. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times are added to the effective on-time. The dead time occurs only in PWM mode ( $\overline{\text{SKIP}} = V_{\text{DD}}$ ) and during dynamic output-voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{\text{SW}} = \frac{V_{\text{OUT}} + V_{\text{DROP1}}}{t_{\text{ON}}(V_{\text{IN}} + V_{\text{DROP2}})}$$

where  $V_{\text{DROP1}}$  is the sum of the parasitic voltage drops in the inductor discharge path, including the synchronous rectifier, the inductor, and any PC board resistances;  $V_{\text{DROP2}}$  is the sum of the resistances in the charging path, including the high-side switch (Q1 in the *Typical Applications Circuit*), the inductor, and any PC board resistances, and  $t_{\text{ON}}$  is the one-shot on-time (see the *On-Time One-Shot (TON)* section).

## Automatic Pulse-Skipping Mode (SKIP = GND)

In skip mode ( $\overline{\text{SKIP}} = \text{GND}$ ), an inherent automatic switchover to PFM takes place at light loads (Figure 2). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the synchronous-rectifier MOSFET (Q2 in the *Typical Applications Circuit*, Figure 8). Once  $V_{\text{PGND}} - V_{\text{LX}}$  drops below 5% of the current-limit threshold (2.5mV

for the default 50mV current-limit threshold), the comparator forces DL low (Figure 1). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which PFM/PWM crossover occurs,  $I_{\text{LOAD(SKIP)}}$ , is equal to half the peak-to-peak ripple current, which is a function of the inductor value (Figure 2). This threshold is relatively constant, with only a minor dependence on the input voltage ( $V_{\text{IN}}$ ):

$$I_{\text{LOAD(SKIP)}} = \left( \frac{V_{\text{OUT}} \times K}{2L} \right) \left( \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}} \right)$$

where K is the on-time scale factor (see Table 1). For example, in the *Typical Applications Circuit* of Figure 8 ( $K = 1.7\mu\text{s}$ ,  $V_{\text{OUT}} = 2.5\text{V}$ ,  $V_{\text{IN}} = 12\text{V}$ , and  $L = 1\mu\text{H}$ ), the pulse-skipping switchover occurs at:

$$\left( \frac{2.5\text{V} \times 1.7\mu\text{s}}{2 \times 1\mu\text{H}} \right) \left( \frac{12\text{V} - 2.5\text{V}}{12\text{V}} \right) = 1.68\text{A}$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used. The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resis-

**Table 1. Approximate K-Factor Errors**

TON SETTING	TYPICAL K-FACTOR ( $\mu\text{s}$ )	K-FACTOR ERROR (%)	MINIMUM $V_{\text{IN}}$ AT $V_{\text{OUT}} = 2.5\text{V}$ ( $h = 1.5$ ; SEE THE DROPOUT PERFORMANCE SECTION)
200 (TON = AV <sub>DD</sub> )	5.0	$\pm 10$	3.15
300 (TON = OPEN)	3.3	$\pm 10$	3.47
450 (TON = REF)	2.2	$\pm 12.5$	4.13
600 (TON = GND)	1.7	$\pm 12.5$	5.61

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tance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input-voltage levels.

DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX8550A regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ( $\overline{\text{SKIP}} = \text{GND}$  and  $I_{\text{LOAD}} < I_{\text{LOAD}}(\overline{\text{SKIP}})$ ), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

## Forced-PWM Mode ( $\overline{\text{SKIP}} = \text{AVDD}$ )

The low-noise forced-PWM mode ( $\overline{\text{SKIP}} = \text{AVDD}$ ) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while  $DH$  maintains a duty factor of  $V_{\text{OUT}} / V_{\text{IN}}$ . Forced-PWM mode keeps the switching frequency fairly constant. However, forced-PWM operation comes at a cost where the no-load  $V_{\text{DD}}$  bias current remains between 2mA and 20mA due to the external MOSFET's gate charge and switching frequency. Forced-PWM mode is most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output-voltage adjustment.

## Current-Limit Buck Regulator (ILIM)

### Valley Current Limit

The current-limit circuit for the buck regulator portion of the MAX8550A employs a unique "valley" current-sensing algorithm that senses the voltage drop across  $LX$  and  $PGND1$  and uses the on-resistance of the rectifying MOSFET ( $Q2$  in the *Typical Applications Circuit*, Figure 8) as the current-sensing element. If the magnitude of the current-sense signal is above the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle (Figure 4). With valley current-limit sensing, the actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor current ripple. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and input voltage. When combined with the undervoltage-protec-

tion circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX8550A also implements a negative current limit to prevent excessive reverse inductor currents when the buck regulator output is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when  $V_{\text{ILIM}}$  is adjusted. The current-limit threshold is adjusted with an external resistor-divider at  $ILIM$ . A  $2\mu\text{A}$  to  $20\mu\text{A}$  divider current is recommended for accuracy and noise immunity.

The current-limit threshold adjustment range is from 25mV to 200mV. In the adjustable mode, the current-limit threshold voltage (from  $PGND1$  to  $LX$ ) is precisely 1/10th the voltage seen at  $ILIM$ . The threshold defaults to 50mV when  $ILIM$  is connected to  $AV_{\text{DD}}$ . The logic threshold for switchover to the 50mV default value is approximately  $AV_{\text{DD}} - 1V$ .

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen between  $LX$  and  $GND$ .

## POR, UVLO, and Soft-Start

Internal power-on reset (POR) occurs when  $AV_{\text{DD}}$  rises above approximately 2V, resetting the fault latch and the soft-start counter, powering up the reference, and preparing the buck regulator for operation. Until  $AV_{\text{DD}}$  reaches 4.25V (typ),  $AV_{\text{DD}}$  undervoltage-lockout

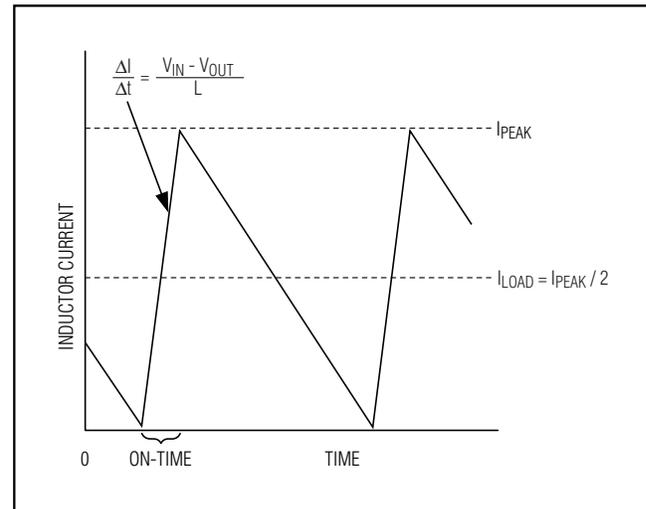


Figure 2. Pulse-Skipping/Discontinuous Crossover Point

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**MAX8550A**

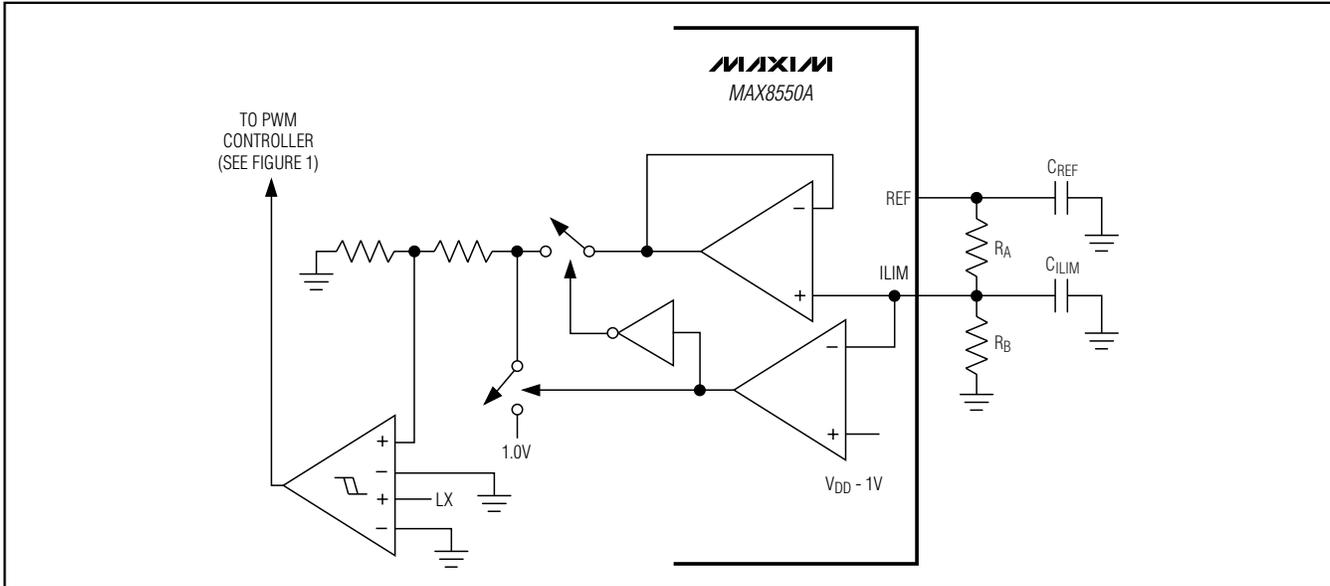


Figure 3. Adjustable Current-Limit Threshold

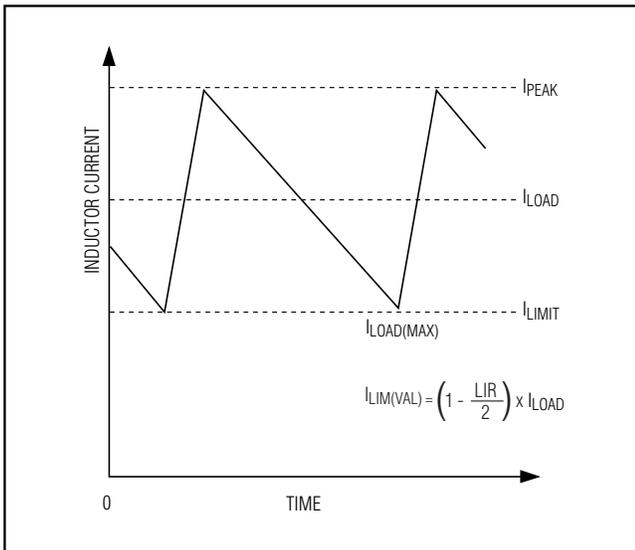


Figure 4. Valley Current-Limit Threshold

(UVLO) circuitry inhibits switching. The controller inhibits switching by pulling DH low and holding DL low when OVP and shutdown discharge are disabled (OVP/UVP = REF or GND) or forcing DL high when OVP and shutdown discharge are enabled (OVP/UVP = AVDD or OPEN). See Table 3 for a detailed truth table for OVP/UVP and shutdown settings. When AVDD rises above 4.25V, the controller activates the buck regulator and initializes the internal soft-start.

The buck regulator's internal soft-start allows a gradual increase of the current-limit level during startup to reduce the input surge currents. The MAX8550A divides the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach regulation within 425µs, soft-start enters the second phase, and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached, after 1.7ms, or when the output reaches the nominal regulation voltage, whichever occurs first. Adding a capacitor in parallel with the external ILIM resistors creates a continuously adjustable analog soft-start function for the buck regulator's output.

Soft-start in the LDO section can be realized by connecting a capacitor between the SS pin and ground. When VTT is turned off or placed in standby mode, or during thermal shutdown of the LDOs, the SS capacitor is discharged. When VTT is turned on or when the thermal limit is removed, an internal 4µA (typ) current charges the SS capacitor. The resulting ramp voltage on SS linearly increases the current-limit comparator threshold to the VTT output, until full current limit is attained when SS reaches approximately 1.6V. This lowering of the current limit during startup limits the initial inrush current peaks, particularly when driving capacitors. Choose the value of the SS cap appropriately to set the soft-start time window. Leave SS floating to disable the soft-start feature.

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## Power-OK (POK1)

POK1 is an open-drain output for a window comparator that continuously monitors  $V_{OUT}$ . POK1 is actively held low when  $\overline{SHDN}$  is low and during the buck regulator output's soft-start. After the digital soft-start terminates, POK1 becomes high impedance as long as the output voltage is within  $\pm 10\%$  of the nominal regulation voltage set by FB. When  $V_{OUT}$  drops 10% below or rises 10% above the nominal regulation voltage, the MAX8550A pulls POK1 low. Any fault condition forces POK1 low until the fault latch is cleared by toggling  $\overline{SHDN}$  or cycling  $AV_{DD}$  power below 1V. For logic-level output voltages, connect an external pullup resistor between POK1 and  $AV_{DD}$ . A 100k $\Omega$  resistor works well in most applications. Note that the POK1 window detector is completely independent of the overvoltage- and undervoltage-protection fault detectors and the state of VTTS and VTTR.

## $\overline{SHDN}$ and Output Discharge

The  $\overline{SHDN}$  input corresponds to the buck regulator and places the buck regulator's portion of the IC in a low-power mode (see the *Electrical Characteristics* table).  $\overline{SHDN}$  is also used to reset a fault signal such as an overvoltage or undervoltage fault.

When output discharge is enabled, (OVP/UVP =  $AV_{DD}$  or open) and  $\overline{SHDN}$  is pulled low, or if UVP is enabled (OVP/UVP =  $AV_{DD}$ ) and  $V_{OUT}$  falls to 70% of its regulation set point, the MAX8550A discharges the buck regulator output (through the OUT input) through an internal 10 $\Omega$  switch to ground. While the output is discharging, DL is forced low and the PWM controller is disabled but the reference remains active to provide an accurate threshold. Once the output voltage drops below 0.1V, the MAX8550A shuts down the reference and pulls DL high, effectively clamping the buck output and LX to ground.

When output discharge is disabled (OVP/UVP = REF or GND), the controller does not actively discharge the buck output and the DL driver remains low. Under these conditions, the buck output discharge rate is determined

by the load current and its output capacitance. The buck regulator detects and latches the discharge-mode state set by the OVP/UVP setting on startup.

When OUT is discharging, both VTT and VTTR outputs will remain alive and continue to track REF<sub>IN</sub> until OUT drops to 0.1V.

## $\overline{STBY}$

The  $\overline{STBY}$  input is an active-low input that is used to shut down only the VTT output. When  $\overline{STBY}$  is low, VTT is high impedance.

## Power-OK (POK2)

POK2 is the open-drain output for a window comparator that continuously monitors the VTTS input and VTTR output. POK2 is pulled low when REF<sub>IN</sub> is less than 0.8V. POK2 is high impedance as long as the output voltage is within  $\pm 10\%$  of the nominal regulation voltage as set by REF<sub>IN</sub>. When  $V_{VTTS}$  or  $V_{VTTR}$  rises 10% above or 10% below its nominal regulation voltage, the MAX8550A pulls POK2 low. For logic-level output voltages, connect an external pullup resistor between POK2 and  $AV_{DD}$ . A 100k $\Omega$  resistor works well in most applications.

## Current Limit (LDO for VTT and VTTR Buffer)

The VTT output is a linear regulator that regulates the input (VTTI) to half the  $V_{REFIN}$  voltage. The feedback point for VTT is at the VTTS input (Figure 1). VTT is capable of sinking and sourcing at least 1.5A of continuous current and 3A peak current. The current limit for VTT and VTTR is typically  $\pm 5A$  and  $\pm 32mA$ , respectively. When the current limit for either output is reached, the outputs regulate the current, not the voltage.

## Fault Protection

The MAX8550A provides overvoltage/undervoltage fault protection in the buck controller. Select OVP/UVP to enable and disable fault protection as shown in Table 3. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions.

**Table 2. Shutdown and Standby Control Logic**

$\overline{SHDN}$	$\overline{STBY}$	BUCK OUTPUT ( $V_{DDQ}$ )	VTT	VTTR
$AV_{DD}^*$	$AV_{DD}^*$	ON	ON	ON
$AV_{DD}^{**}$	GND <sup>**</sup>	ON	OFF (high impedance)	ON
GND <sup>***</sup>	X	OFF	OFF (tracking 1/2 REF <sub>IN</sub> )	OFF (tracking 1/2 REF <sub>IN</sub> )

\*For DDR application, this is referred as S0 state, where all outputs are on.

\*\*For DDR application, this is referred as S3 state, where  $V_{DDQ}$  and VTTR are kept on, but VTT is turned off (high impedance).

\*\*\*For DDR application, this is referred as S4/S5 states, where all outputs are off. Discharge mode should be selected (OVP/UVP =  $AV_{DD}$  or OPEN, see Table 3) to discharge the outputs.

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## Overvoltage Protection (OVP)

When the output voltage rises above 116% of the nominal regulation voltage and OVP is enabled (OVP/UVP = AV<sub>DD</sub> or open), the OVP circuit sets the fault latch, shuts down the PWM controller, and immediately pulls DH low and forces DL high. This turns on the synchronous-rectifier MOSFET (Q2 in the *Typical Applications Circuit* of Figure 8) with a 100% duty cycle, rapidly discharging the output capacitor and clamping the output to ground. Note that immediately latching DL high can cause the output voltage to go slightly negative due to energy stored in the output LC circuit at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. Toggle  $\overline{\text{SHDN}}$  or cycle AV<sub>DD</sub> below 1V to clear the fault latch and restart the controller. OVP is disabled when OVP/UVP is connected to REF or GND (see Table 3). OVP only applies to the buck output. The VTT and VTTR outputs do not have overvoltage protection.

## Undervoltage Protection (UVP)

When the output voltage drops below 70% of its regulation voltage while UVP is enabled, the controller sets the fault latch and begins the discharge mode (see the *Shutdown and Output Discharge* section). When the output voltage drops to 0.1V, the synchronous rectifier (Q2 in the *Typical Applications Circuit*) turns on and clamps the buck output to GND. UVP is ignored for at least 10ms (min) after startup or after a rising edge on  $\overline{\text{SHDN}}$ . Toggle  $\overline{\text{SHDN}}$  or cycle AV<sub>DD</sub> power below 1V to clear the fault latch and restart the controller. UVP is disabled when OVP/UVP is left open or connected to GND (see Table 3). UVP only applies to the buck output. The VTT and VTTR outputs do not have undervoltage protection.

## Thermal Fault Protection

The MAX8550A features two thermal-fault-protection circuits. One monitors the buck-regulator portion of the IC and the other monitors the linear regulator (VTT) and the reference buffer output (VTTR). When the junction temperature of the buck-regulator portion of the MAX8550A rises above +160°C, a thermal sensor activates the fault latch, pulls POK1 low, and shuts down the buck-controller output using discharge mode regardless of the OVP/UVP setting. Toggle  $\overline{\text{SHDN}}$  or cycle AV<sub>DD</sub> below 1V to reactivate the controller after the junction temperature cools by 15°C. If the VTT and VTTR regulator portion of the IC has its die temperature rise above +160°C, then VTT and VTTR shut off, go high impedance, and restart after the die portion of the IC cools by 15°C. Both thermal faults are independent. For example, if the VTT output is overloaded to the point that it triggers its thermal fault, the buck regulator continues to function.

## Design Procedure

Firmly establish the input voltage range (V<sub>IN</sub>) and maximum load current (I<sub>LOAD</sub>) in the buck regulator before choosing a switching frequency and inductor operating point (ripple current ratio or LIR). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- Input Voltage Range. The maximum value (V<sub>IN(MAX)</sub>) must accommodate the worst-case voltage. The minimum value (V<sub>IN(MIN)</sub>) must account for the lowest voltage after drops due to connectors and fuses. If there is a choice, lower input voltages result in better efficiency.

**Table 3. OVP/UVP Fault Protection**

OVP/UVP	DISCHARGE	UVP PROTECTION	OVP PROTECTION
AV <sub>DD</sub>	Yes. DL forced high when $\overline{\text{SHDN}}$ is low and OUT < 0.1V.	Enabled	Enabled
OPEN	Yes. DL forced high when $\overline{\text{SHDN}}$ is low and OUT < 0.1V.	Disabled	Enabled
REF	No. DL forced low when $\overline{\text{SHDN}}$ is low.	Enabled	Disabled
GND	No. DL forced low when $\overline{\text{SHDN}}$ is low.	Disabled	Disabled



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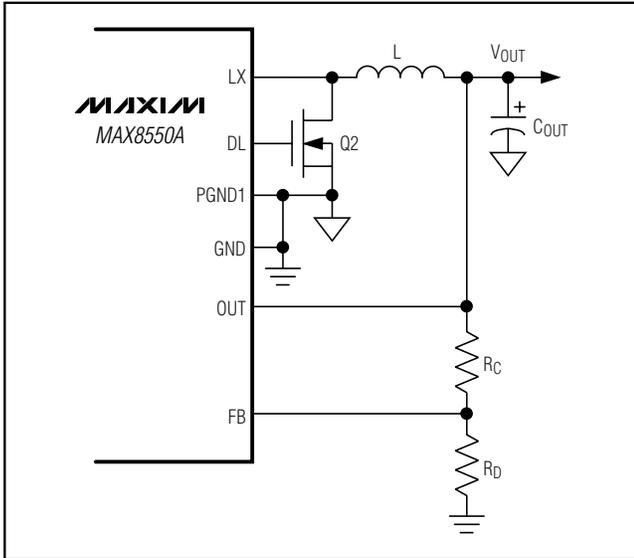


Figure 6. Setting V<sub>OUT</sub> with a Resistive Voltage-Divider

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at frequencies up to 200kHz. The core must be large enough not to saturate at the peak inductor current (I<sub>PEAK</sub>):

$$I_{PEAK} = I_{LOAD(MAX)} \left( 1 + \frac{LIR}{2} \right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0μH, 1.5μH, 2.2μH, 3.3μH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

### Input Capacitor Selection (Buck)

The input capacitor must meet the ripple current requirement (I<sub>RMS</sub>) imposed by the switching currents:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

I<sub>RMS</sub> has a maximum value of I<sub>LOAD</sub> / 2 when V<sub>IN</sub> = 2 × V<sub>OUT</sub>. For most applications, nontantalum capacitors (ceramic, aluminum, POS, or OSCON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX8550A is operated as the second stage of a two-stage power conversion sys-

tem, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

### Output Capacitor Selection (Buck)

The output filter capacitor must have low enough equivalent series resistance (R<sub>ESR</sub>) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications in which the output is subject to violent load transients, the output capacitor's size depends on how much R<sub>ESR</sub> is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much R<sub>ESR</sub> is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller is approximately equal to the total inductor ripple current multiplied by the output capacitor's R<sub>ESR</sub>. Therefore, the maximum R<sub>ESR</sub> required to meet ripple specifications is:

$$R_{ESR} \leq \frac{V_{RIPPLE}}{I_{LOAD(MAX)} \times LIR}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OSCONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V<sub>SAG</sub> and V<sub>SOAR</sub> from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V<sub>SAG</sub> and V<sub>SOAR</sub> equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability (see the *Stability Requirements* section).

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Stability Requirements

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{\text{ESR}} \leq \frac{f_{\text{SW}}}{\pi}$$

where:

$$f_{\text{ESR}} = \frac{1}{2\pi \times R_{\text{ESR}} \times C_{\text{OUT}}}$$

If  $C_{\text{OUT}}$  consists of multiple same-value capacitors, as in the *Typical Applications Circuit* of Figure 8, the  $f_{\text{ESR}}$  remains the same as that of a single capacitor.

For a typical 600kHz application, the ESR zero frequency must be well below 190kHz, preferably below 100kHz. Two 150 $\mu\text{F}/4\text{V}$  Sanyo POS capacitors are used to provide 12m $\Omega$  (max) of  $R_{\text{ESR}}$ . This results in a zero at 42kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired.

Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped but can cause the output voltage to rise above or fall below the tolerance limits. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

## VTT Output Capacitor Selection (LDO)

A minimum value of 60 $\mu\text{F}$  is needed to stabilize the VTT output for load currents up to  $\pm 1.5\text{A}$ . This value of capacitance limits the regulator's unity-gain bandwidth frequency to about 700kHz (typ) to allow adequate phase margin for stability. To keep the capacitor acting as a capacitor within the regulator's bandwidth, it is important that ceramic caps with low ESR and ESL be used.

Since the gain bandwidth is also determined by the transconductance of the output FETs, which increases with load current, the output capacitor needs to be greater than 60 $\mu\text{F}$  if the load current exceeds 1.5A, but can be smaller than 60 $\mu\text{F}$  if the maximum load current is less than 1.5A. As a rule, choose the minimum capacitance and maximum ESR for the output capacitor using the following:

$$C_{\text{OUT\_MIN}} = 60\mu\text{F} \times \sqrt{\frac{I_{\text{LOAD}}}{1.5\text{A}}}$$

$$R_{\text{ESR\_MAX}} = 5\text{m}\Omega \times \sqrt{\frac{1.5\text{A}}{I_{\text{LOAD}}}}$$

$R_{\text{ESR}}$  value is measured at the unity-gain-bandwidth frequency given by approximately:

$$f_{\text{GBW}} = \frac{40}{C_{\text{OUT}}} \times \sqrt{\frac{I_{\text{LOAD}}}{1.5\text{A}}}$$

Once these conditions for stability are met, additional capacitors, including those of electrolytic and tantalum types, can be connected in parallel to the ceramic capacitor (if desired) to further suppress noise or voltage ripple at the output.

## VTTR Output Capacitor Selection (LDO)

The VTTR buffer is a scaled-down version of the VTT regulator, with much smaller output transconductance. Its compensation cap can therefore be smaller, and its ESR larger, than what is required for its larger counterpart. For typical applications requiring load current up to  $\pm 15\text{mA}$ , a ceramic cap with a minimum value of 1 $\mu\text{F}$  is recommended ( $R_{\text{ESR}} < 0.3\Omega$ ). Connect this cap between VTTR and the analog ground plane.

## VTTI Input Capacitor Selection (LDO)

Both the VTT and VTTR output stages are powered from the same VTTI input. Their output voltages are referenced to the same REFIN input. The value of the VTTI bypass capacitor is chosen to limit the amount of ripple/noise at VTTI, or the amount of voltage dip during a load transient. Typically VTTI is connected to the output of the buck regulator, which already has a large bulk

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

capacitor. Nevertheless, a ceramic capacitor of at least 10µF must be used and must be added and placed as close as possible to the VTTI pin. This value must be increased with larger load current, or if the trace from the VTTI pin to the power source is long and has significant impedance. Furthermore, to prevent undesirable VTTI bounce from coupling back to the REFIN input and possibly causing instability in the loop, the REFIN pin should ideally tap its signal from a separate low-impedance DC source rather than directly from the VTTI input. If the latter is unavoidable, increase the amount of bypass capacitance at the VTTI input and add additional bypass at the REFIN pin.

## MOSFET Selection (Buck)

The MAX8550A drives external, logic-level, n-channel MOSFETs as the circuit-switch elements. The key selection parameters:

**On-resistance (R<sub>DS(ON)</sub>):** the lower, the better.

**Maximum drain-to-source voltage (V<sub>DSS</sub>):** should be at least 20% higher than input supply rail at the high-side MOSFET's drain.

**Gate charges (Q<sub>G</sub>, Q<sub>GD</sub>, Q<sub>GS</sub>):** the lower the better.

Choose MOSFETs with rated R<sub>DS(ON)</sub> at V<sub>GS</sub> = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has a conduction loss equal to its switching loss at nominal input voltage and maximum output current (see below). For the low-side MOSFET, make sure that it does not spuriously turn on because of dV/dt caused by the high-side MOSFET turning on, as this results in shoot-through current degrading efficiency. MOSFETs with a lower Q<sub>GD</sub> to Q<sub>GS</sub> ratio have higher immunity to dV/dt.

For proper thermal-management design, calculate the power dissipation at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage. For the low-side MOSFET, the worst case is at V<sub>IN(MAX)</sub>. For the high-side MOSFET, the worst case could be at either V<sub>IN(MIN)</sub> or V<sub>IN(MAX)</sub>. The high-side MOSFET and low-side MOSFET have different loss components due to the circuit operation. The low-side MOSFET operates as a zero-voltage switch; therefore, major losses are:

- The channel-conduction loss (P<sub>LSCC</sub>)
- The body-diode conduction loss (P<sub>LSDC</sub>)
- The gate-drive loss (P<sub>LSDR</sub>):

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use R<sub>DS(ON)</sub> at T<sub>J(MAX)</sub>:

$$P_{LSDC} = 2I_{LOAD} \times V_F \times t_{DT} \times f_{SW}$$

where V<sub>F</sub> is the body-diode forward-voltage drop, t<sub>DT</sub> is the dead time (≈30ns), and f<sub>SW</sub> is the switching frequency. Because of the zero-voltage switch operation, the low-side MOSFET gate-drive loss occurs as a result of charging and discharging the input capacitance, (C<sub>ISS</sub>). This loss is distributed among the average DL gate-driver's pullup and pulldown resistance, R<sub>DL</sub> (≈1Ω), and the internal gate resistance (R<sub>GATE</sub>) of the MOSFET (≈2Ω). The drive power dissipated is given by:

$$P_{LSDR} = C_{ISS} \times V_{GS}^2 \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DL}}$$

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses:

- The channel-conduction loss (P<sub>HSCC</sub>)
- The VI overlapping switching loss (P<sub>HSSW</sub>)
- The drive loss (P<sub>HSDR</sub>)

(The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current):

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use R<sub>DS(ON)</sub> at T<sub>J(MAX)</sub>:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_{SW} \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$$

where I<sub>GATE</sub> is the average DH-driver output current determined by:

$$I_{GATE(ON)} = \frac{2.5V}{R_{DH} + R_{GATE}}$$

where R<sub>DH</sub> is the high-side MOSFET driver's on-resistance (1Ω typ) and R<sub>GATE</sub> is the internal gate resistance of the MOSFET (≈2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{DH}}$$

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where  $V_{GS} = V_{DD} = 5V$ . In addition to the losses above, allow about 20% more for additional losses because of MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET that is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipations. To reduce EMI caused by switching noise, add a 0.1 $\mu$ F ceramic capacitor from the high-side switch drain to the low-side switch source, or add resistors in series with DH and DL to slow down the switching transitions. Adding series resistors increases the power dissipation of the MOSFET, so ensure that this does not overheat the MOSFET.

## MOSFET Snubber Circuit (Buck)

Fast switching transitions cause ringing because of a resonating circuit formed by the parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, an optional series RC snubber circuit is added across each switch. Below is a simple procedure for selecting the value of the series RC of the snubber circuit:

- 1) Connect a scope probe to measure  $V_{LX}$  to PGND1, and observe the ringing frequency,  $f_R$ .
- 2) Estimate the circuit parasitic capacitance ( $C_{PAR}$ ) at LX by first finding a capacitor value, which, when connected from LX to PGND1, reduces the ringing frequency by half.  $C_{PAR}$  can then be calculated as 1/3rd the value of the capacitor value found.
- 3) Estimate the circuit parasitic inductance ( $L_{PAR}$ ) from the equation:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}}$$

- 4) Calculate the resistor for critical dampening ( $R_{SNUB}$ ) from the equation:  $R_{SNUB} = 2\pi \times f_R \times L_{PAR}$ . Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.
- 5) The capacitor ( $C_{SNUB}$ ) should be at least 2 to 4 times the value of  $C_{PAR}$  to be effective.

The power loss of the snubber circuit ( $P_{RSNUB}$ ) is dissipated in the resistor and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times V_{IN}^2 \times f_{SW}$$

where  $V_{IN}$  is the input voltage and  $f_{SW}$  is the switching frequency. Choose an  $R_{SNUB}$  power rating that meets the specific application's derating rule for the power dissipation calculated.

## Setting the Current Limit (Buck)

The current-sense method used in the MAX8550/MAX8551 makes use of the on-resistance ( $R_{DS(ON)}$ ) of the low-side MOSFET (Q2 in the *Typical Applications Circuit*). When calculating the current limit, use the worst-case maximum value for  $R_{DS(ON)}$  from the MOSFET data sheet, and add some margin for the rise in  $R_{DS(ON)}$  with temperature. A good general rule is to allow 0.5% additional resistance for each 1°C of temperature rise.

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at  $I_{LOAD(MAX)}$  minus half the ripple current; therefore:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left( \frac{I_{LOAD(MAX)} \times LIR}{2} \right)$$

where  $I_{LIM(VAL)}$  equals the minimum valley current-limit threshold voltage divided by the on-resistance of Q2 ( $R_{DS(ON)Q2}$ ). For the 50mV default setting, connect ILIM to AVDD. In adjustable mode, the valley current-limit threshold is precisely 1/10th\* the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND with ILIM connected to the center tap. The external 250mV to 2V adjustment range corresponds to a 25mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10 $\mu$ A to prevent significant inaccuracy in the valley current-limit tolerance.

## Foldback Current Limit

Alternately, foldback current limit can be implemented if the UVP latch option is not available. Foldback current limit reduces the power dissipation of external components so they can withstand indefinite overload and short circuit, with automatic recovery after the overload or short circuit is removed. To implement foldback current limit, connect a resistor from  $V_{OUT}$  to ILIM ( $R_6$  in Figure 7 and the *Typical Applications Circuit*), in addition to the resistor-divider network ( $R_4$  and  $R_5$ )

\*In the negative direction, the adjustable current limit is typically -1/8th the voltage seen at ILIM.

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used for setting the adjustable current limit as shown in Figure 7.

The following is a procedure for calculating the value of R4, R5, and R6:

- 1) Calculate the voltage,  $V_{ILIM(NOM)}$ , required at  $I_{LIM}$  when the output voltage is at nominal:

$$V_{ILIM(NOM)} = 10 \times I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right) \times R_{DS(ON)Q2}$$

- 2) Pick a percentage of foldback, PFB, from 15% to 40%.
- 3) Calculate the voltage,  $V_{ILIM(OV)}$ , when the output is shorted (OV):

$$V_{ILIM(OV)} = P_{FB} \times V_{ILIM(NOM)}$$

- 4) The value for R4 can be calculated as:

$$R4 = \frac{2V - V_{ILIM(OV)}}{10\mu A}$$

- 5) The parallel combination of R5 and R6, denoted R56, is calculated as:

$$R56 = \left(\frac{2V}{10\mu A}\right) - R4$$

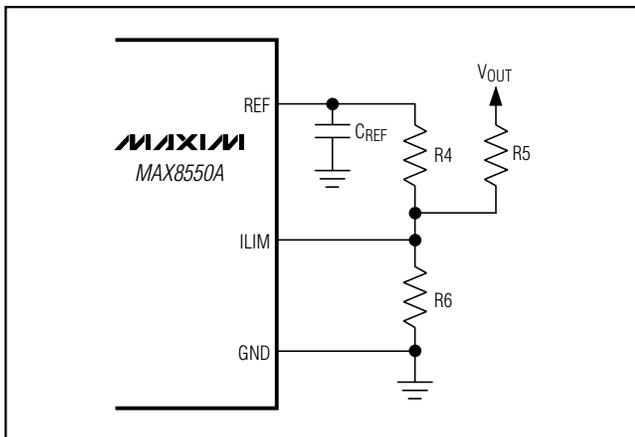


Figure 7. Foldback Current Limit

- 6) Then R6 can be calculated as:

$$R6 = \frac{V_{OUT} \times R4 \times R56}{\left[ \left( V_{OUT} - (V_{ILIM(NOM)} - V_{ILIM(OV)}) \right) \times R4 - \left( (V_{ILIM(NOM)} - V_{ILIM(OV)}) \times R56 \right) \right]}$$

- 7) Then R5 is calculated as:

$$R5 = \frac{R6 \times R56}{R6 - R56}$$

### Boost-Supply Diode and Capacitor Selection (Buck)

A low-current Schottky diode, such as the CMDSH-3 from Central Semiconductor, works well for most applications. Do not use large-power diodes, because higher junction capacitance can charge up the voltage at BST to the LX voltage and this exceeds the absolute maximum rating of 6V. The boost capacitor should be 0.1μF to 4.7μF, depending on the input and output voltages, external components, and PC board layout. The boost capacitance should be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET conduction time, which happens at maximum operating duty cycle (this occurs at minimum input voltage). In addition, ensure that the boost capacitor does not discharge to below the minimum gate-to-source voltage required to keep the high-side MOSFET fully enhanced for lowest on-resistance. This minimum gate-to-source voltage ( $V_{GS(MIN)}$ ) is determined by:

$$V_{GS(MIN)} = V_{DD} \times \frac{Q_G}{C_{BOOST}}$$

where  $V_{DD}$  is 5V,  $Q_G$  is the total gate charge of the high-side MOSFET, and  $C_{BOOST}$  is the boost-capacitor value where  $C_{BOOST}$  is C7 in the *Typical Applications Circuit* (Figure 8).

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

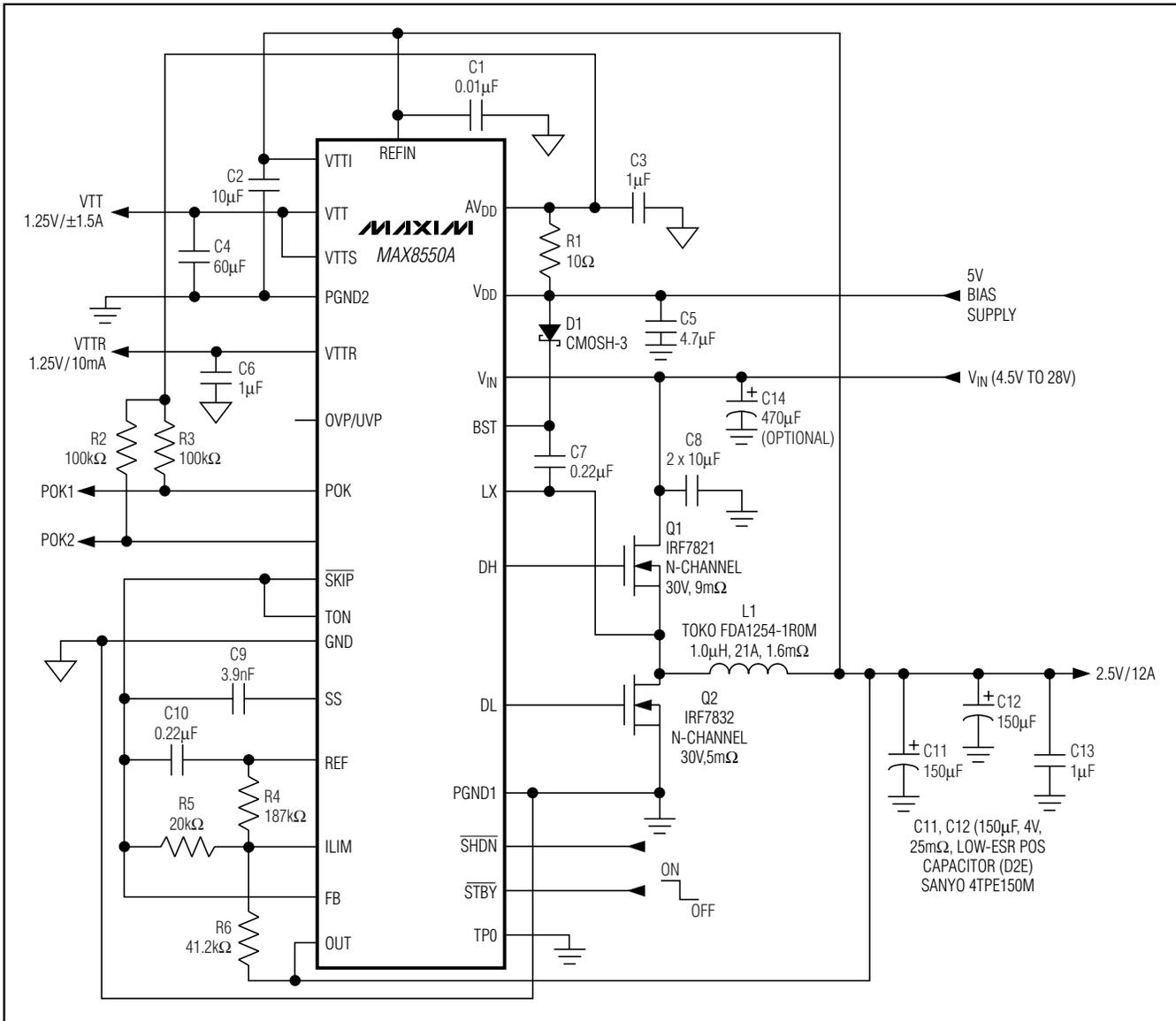


Figure 8. Typical Applications Circuit

### Transient Response (Buck)

The inductor ripple current also affects transient-response performance, especially at low  $V_{IN} - V_{OUT}$  differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{L \times \Delta I_{LOAD(MAX)}^2 \left[ \frac{V_{OUT} \times K}{V_{IN}} + t_{OFF(MIN)} \right]}{2C_{OUT} \times V_{OUT} \left[ \frac{(V_{IN} - V_{OUT}) \times K}{V_{IN}} + t_{OFF(MIN)} \right]}$$

where  $t_{OFF(MIN)}$  is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 1.

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The overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

## Applications Information

### Dropout Performance (Buck)

The output-voltage adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (see Table 1). Also, keep in mind that transient-response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the  $V_{SAG}$  equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time ( $\Delta I_{DOWN}$ ) as much as it ramps up during the on-time ( $\Delta I_{UP}$ ). The ratio  $h = \Delta I_{UP} / \Delta I_{DOWN}$  indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As  $h$  approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle, and  $V_{SAG}$  greatly increases, unless additional output capacitance is used.

A reasonable minimum value for  $h$  is 1.5, but adjusting this up or down allows trade-offs between  $V_{SAG}$ , output capacitance, and minimum operating voltage. For a given value of  $h$ , the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left[ \frac{V_{OUT} \times V_{DROPP1}}{1 - \left( \frac{h \times t_{OFF(MIN)}}{K} \right)} \right] + V_{DROPP2} - V_{DROPP1}$$

where  $V_{DROPP1}$  and  $V_{DROPP2}$  are the parasitic voltage drops in the discharge and charge paths (see the *On-Time One-Shot (TON)* section),  $t_{OFF(MIN)}$  is from the *Electrical Characteristics*, and  $K$  is taken from Table 1. The absolute minimum input voltage is calculated with  $h = 1$ .

If the calculated  $V_{IN(MIN)}$  is greater than the required minimum input voltage, then the operating frequency must be reduced or output capacitance added to obtain an acceptable  $V_{SAG}$ . If operation near dropout is anticipated, calculate  $V_{SAG}$  to be sure of adequate transient response.

A dropout design example follows:

- $V_{OUT} = 2.5V$
- $f_{SW} = 600kHz$
- $K = 1.7\mu s$
- $t_{OFF(MIN)} = 450ns$
- $V_{DROPP1} = V_{DROPP2} = 100mV$
- $h = 1.5$

$$V_{IN(MIN)} = \left[ \frac{2.5V + 0.1V}{1 - \left( \frac{1.5V \times 450ns}{1.7\mu s} \right)} \right] + 0.1V - 0.1V = 4.3V$$

### Voltage Positioning (Buck)

In applications where fast-load transients occur, the output voltage changes instantly by  $R_{ESR} \times C_{OUT} \times \Delta I_{LOAD}$ . Voltage positioning allows the use of fewer output capacitors for such applications, and maximizes the output-voltage AC and DC tolerance window in tight-tolerance applications.

Figure 9 shows the connection of OUT and FB in a voltage-positioned circuit. In nonvoltage-positioned circuits, the MAX8550A regulates at the output capacitor. In voltage-positioned circuits, the MAX8550A regulates on the inductor side of the voltage-positioning resistor.  $V_{OUT}$  is reduced to:

$$V_{OUT(VPS)} = V_{OUT(NO\_LOAD)} - R_{POS} \times I_{LOAD}$$

### PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using

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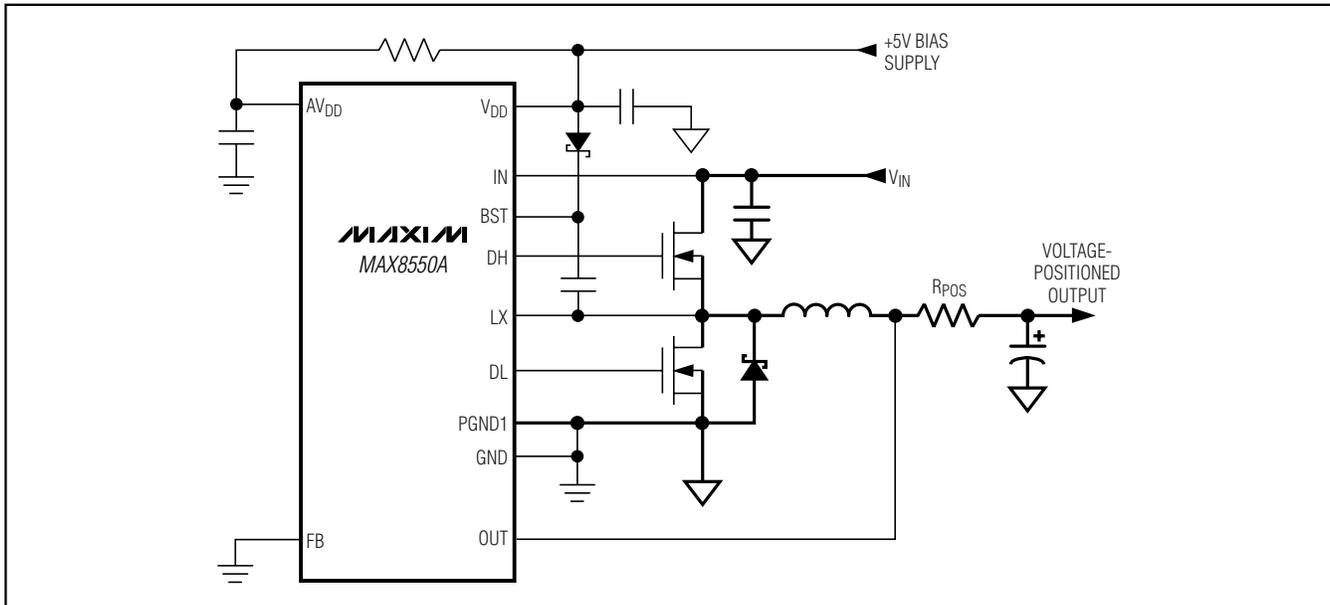


Figure 9. Voltage-Positioned Output

thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single  $m\Omega$  of excess trace resistance causes a measurable efficiency penalty.

- The LX and PGND1 connections to the low-side MOSFET for current sensing must be made using Kelvin-sense connections.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (REF, FB, and ILIM).
- Input ceramic capacitors must be placed as close as possible to the high-side MOSFET drain and the low-side MOSFET source. Position the MOSFETs so the impedance between the input capacitor terminals and the MOSFETs is as low as possible.

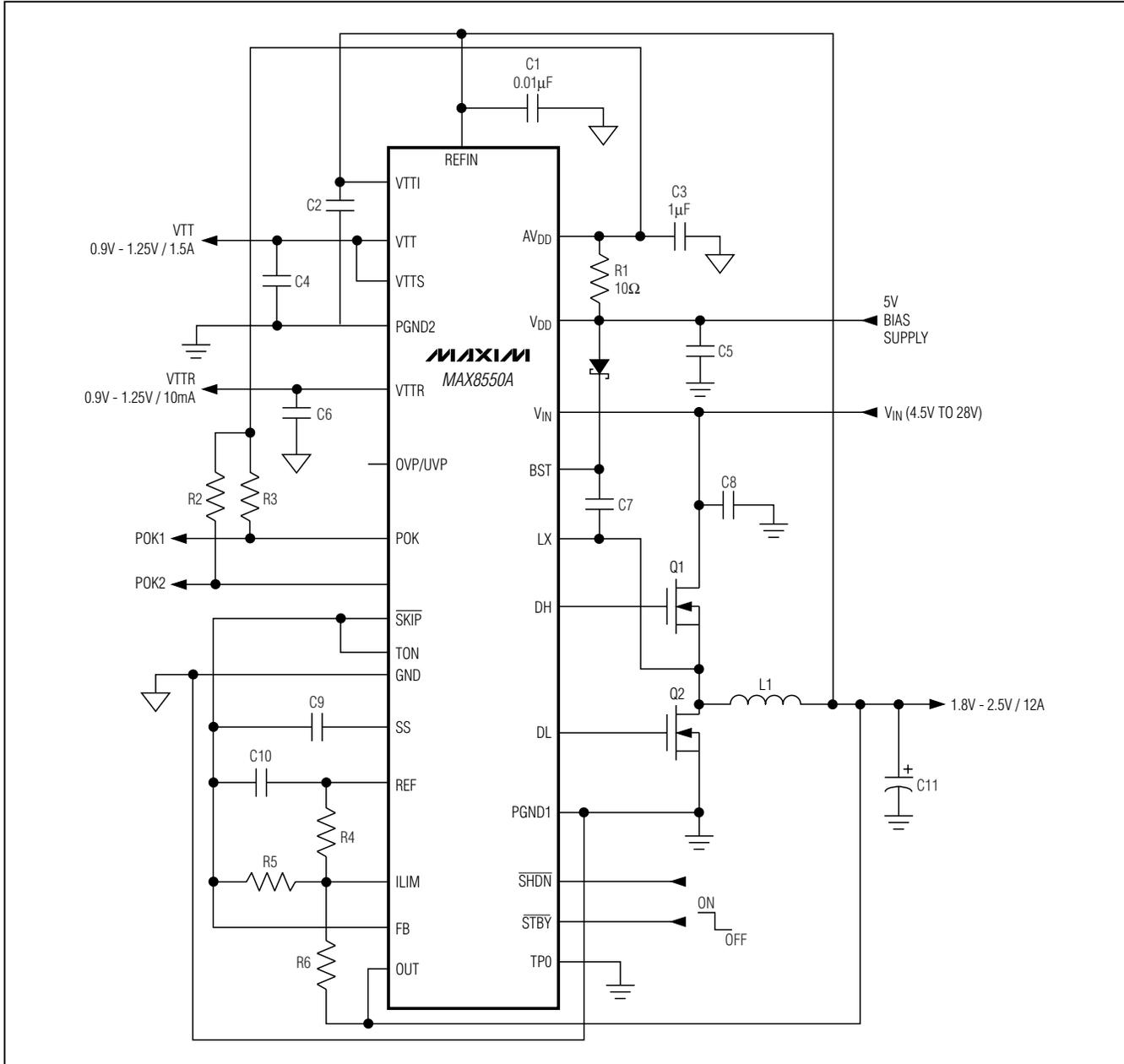
### Special Layout Considerations for LDO Section

The capacitor (or capacitors) at VTT should be placed as close to VTT and PGND2 (pins 12 and 11) as possible to minimize the series resistance/inductance of the trace. The PGND2 side of the capacitor must be short with a low-impedance path to the exposed pad underneath the IC. The exposed pad must be star-connected to GND (pin 24), PGND1 (pin 23), and PGND2 (pin 11). A narrower trace can be used to connect the output voltage on the VTT side of the capacitor back to VTTS (pin 9). However, keep this trace well away from potentially noisy signals such as PGND1 or PGND2. This prevents noise from being injected into the error amplifier's input. For best performance, the VTTI bypass capacitor must be placed as close to VTTI (pin 13) as possible. REFIN (pin 14) should be separately routed with a clean trace and adequately bypassed to GND. Refer to the MAX8550A evaluation kit data sheet for PC board guidelines.

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Typical Operating Circuit

**MAX8550A**



### Chip Information

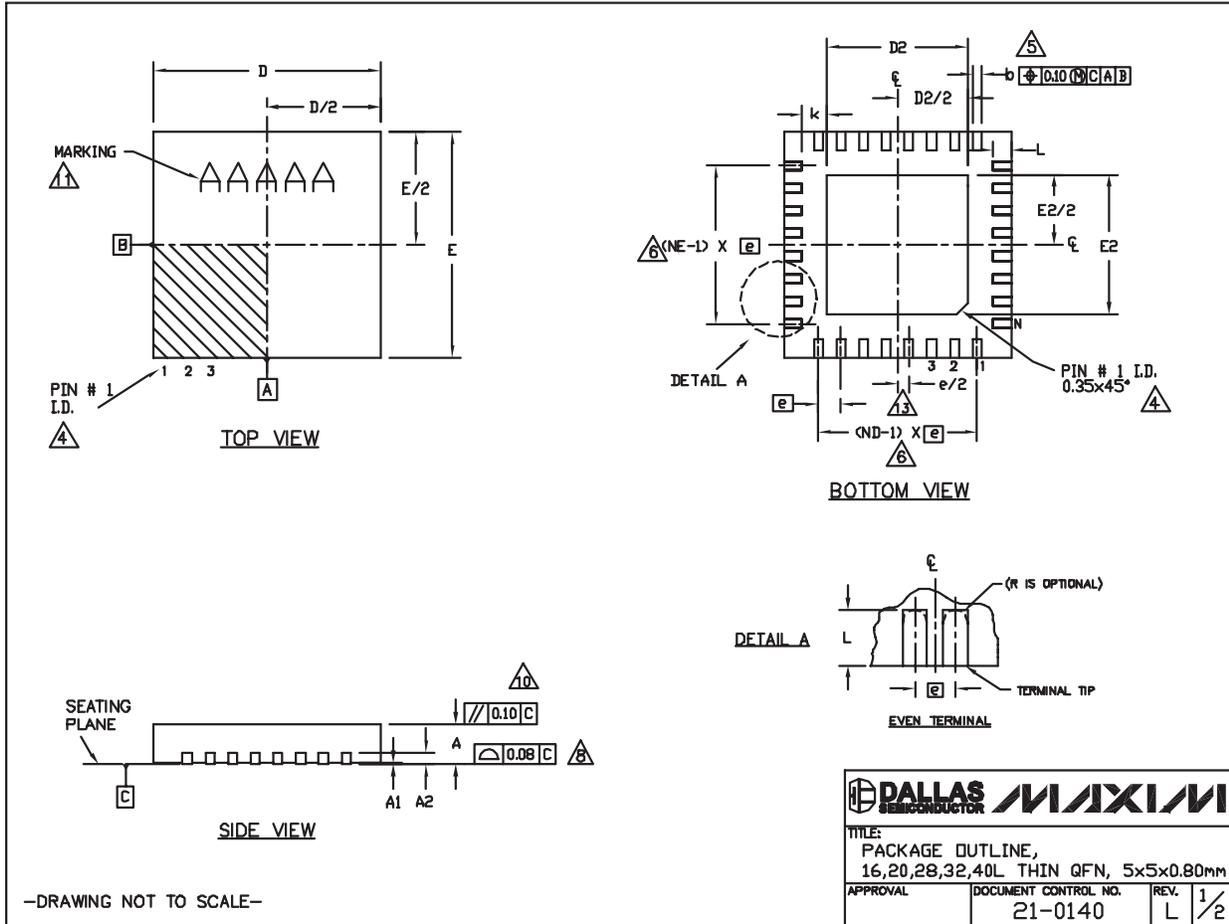
TRANSISTOR COUNT: 5100

PROCESS: BICMOS

# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# Integrated DDR Power-Supply Solution for Desktops, Notebooks, and Graphic Cards

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX8550A

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.												
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.														
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	VHBB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

**NOTES:**

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 93-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
- ALL DIMENSIONS APPLY TO BOTH LEADED AND PBFREE PARTS.

—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm	
APPROVAL	DOCUMENT CONTROL NO. 21-0140
REV.	L 2/2

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