



# PCA9646

## Buffered 4-channel 2-wire bus switch

Rev. 1 — 1 March 2011

Product data sheet

## 1. General description

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The PCA9646 is a monolithic CMOS integrated circuit for 2-wire bus buffering and switching in applications including I<sup>2</sup>C-bus, SMBus, PMBus, and other systems based on similar principles.

Each of the four outputs may be independently enabled in any combination as determined by the contents of the programmable control register. Each I/O is impedance isolated from all others, thus allowing a total of five branches of 2-wire bus with the maximum specified load (e.g.,  $5 \times 400$  pF for Fm+ I<sup>2</sup>C-bus at 1 MHz, or  $5 \times 4$  nF at lower frequencies) ([Ref. 1](#)). More than one PCA9646 may be used in series, providing a substantial fan-out capability.

As per the PCA9525 and PCA9605 simple bus buffers, the PCA9646 includes a unidirectional buffer for the clock signal, and a bidirectional buffer for the data signal. The direction of the clock signal may also be set by the contents of the programmable control register. Clock stretching and timing must always be under control of the master device.

The PCA9646 has excellent application to 2-wire bus address expansion and increasing of maximum load capacitance. Very large LED displays are a perfect example.

## 2. Features and benefits

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- Drop-in pin compatible with PCA9546A, etc.
- Each I/O is impedance isolated from all others allowing maximum capacitance on all branches
- 30 mA static sink capability on all ports
- Works with I<sup>2</sup>C-bus (Standard-mode, Fast-mode, and Fast-mode Plus (Fm+)), SMBus (standard and high power mode), and PMBus
- Fast switching times allow operation in excess of 1 MHz
- Allows driving of large loads (e.g.,  $5 \times 4$  nF)
- Hysteresis on I/O increases noise immunity
- Operating voltages from 2.7 V to 5.5 V
- Uncomplicated characteristics suitable for quick implementation in most common 2-wire bus applications

## 3. Applications

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- Large arrays of I<sup>2</sup>C-bus components, e.g., LED displays
- Power management systems
- Game consoles, computers, RAID systems

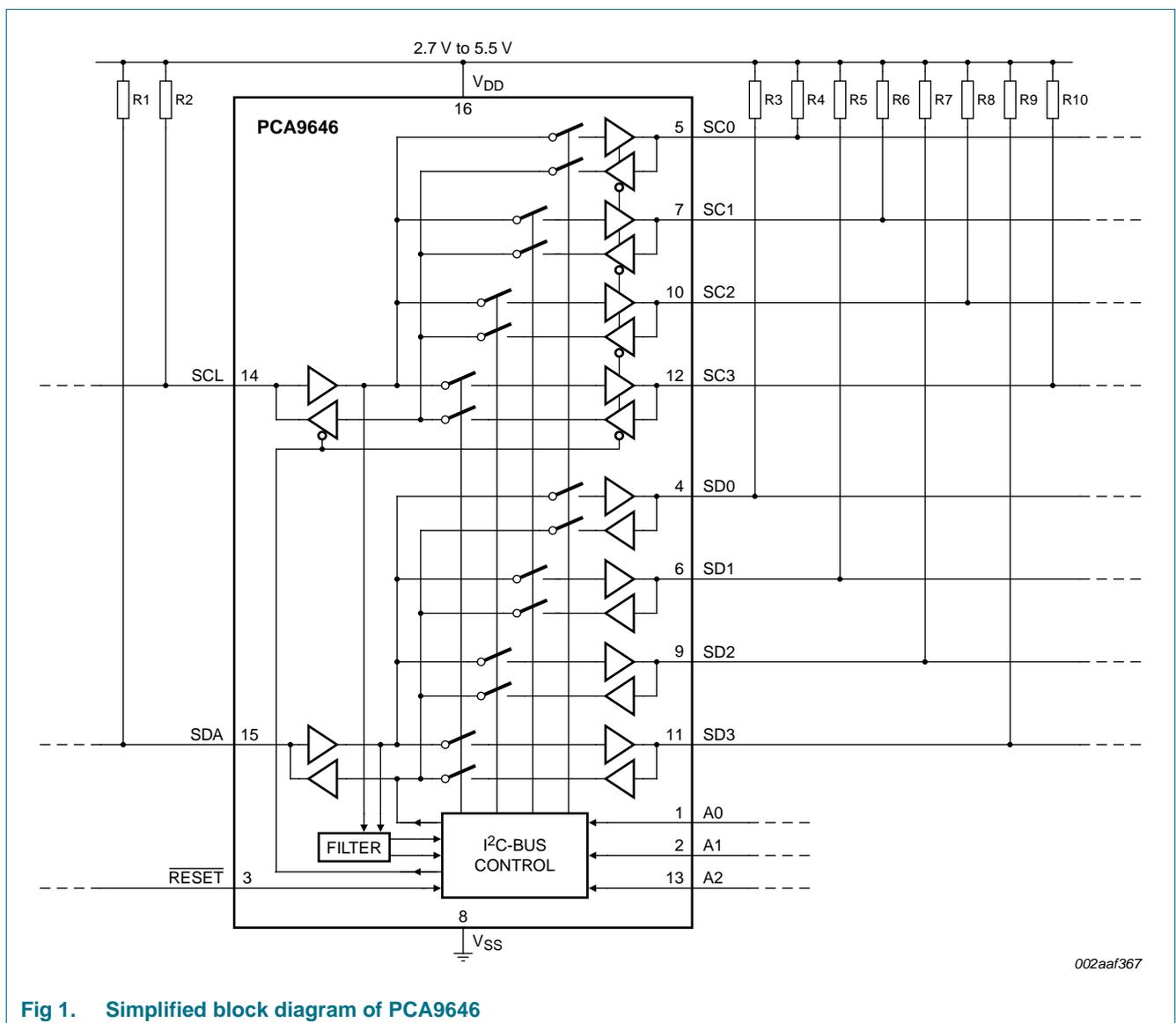


### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		Version
		Name	Description	
PCA9646D	PCA9646	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
PCA9646PW	PCA9646	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 5. Block diagram



002aaf367

Fig 1. Simplified block diagram of PCA9646

## 6. Pinning information

### 6.1 Pinning

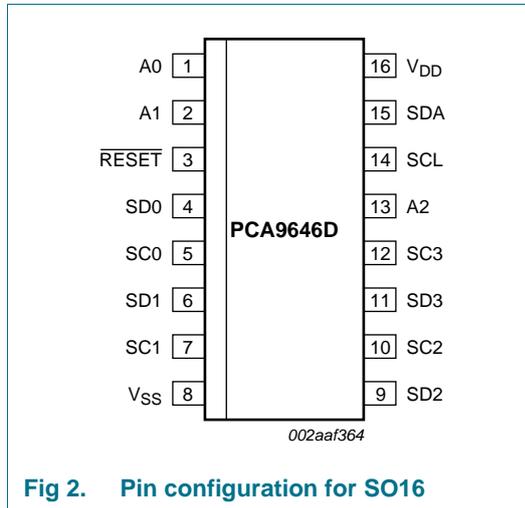


Fig 2. Pin configuration for SO16

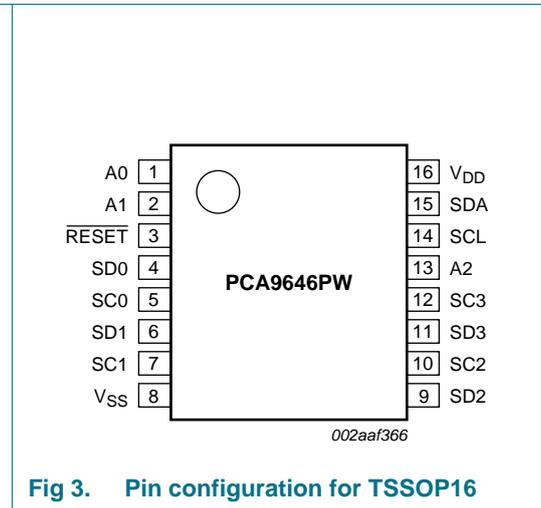


Fig 3. Pin configuration for TSSOP16

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
RESET	3	active LOW reset input
SD0	4	serial data 0
SC0	5	serial clock 0
SD1	6	serial data 1
SC1	7	serial clock 1
V <sub>SS</sub>	8	negative supply (ground)
SD2	9	serial data 2
SC2	10	serial clock 2
SD3	11	serial data 3
SC3	12	serial clock 3
A2	13	address input 2
SCL	14	serial clock line (normally input)
SDA	15	serial data line
V <sub>DD</sub>	16	positive supply

## 7. Functional description

Refer to [Figure 1 “Simplified block diagram of PCA9646”](#).

### 7.1 $V_{DD}$ , $V_{SS}$ — DC supply pins

The power supply voltage for the PCA9646 may be any voltage in the range 2.7 V to 5.5 V. The IC supply must be common with the supply for the bus. Hysteresis on the ports are a percentage of the IC's power supply, hence noise margin considerations should be taken into account when selecting an operating voltage.

### 7.2 SCL — clock signal input

The clock signal buffer is unidirectional, with this pin acting as the default input. However, the clock signal direction may be reversed by setting the MSB of the Control register HIGH. In normal I<sup>2</sup>C-bus operations the master device generates a unidirectional clock signal to the slave. For lowest cost the PCA9646 combines unidirectional buffering of the clock signal with a bidirectional buffer for the data signal. Clock stretching is therefore not supported and slave devices that may require clock stretching must be accommodated by the master adopting an appropriate clocking when communicating with them.

The buffer includes hysteresis to ensure clean switching signals are output, especially with slow rise times on high capacitively loaded buses.

### 7.3 SC0, SC1, SC2, SC3 — clock signal outputs

The clock signal from SCL is buffered through four independent buffers, and the signal is presented at the four SC0 to SC3 ports. Ports are open-drain type and require external pull-up resistors.

When the MSB of the control register is set HIGH, the port direction is reversed. The ANDed result of the selected SC0 to SC3 lines is then used to drive the open-drain output of the SCL pin.

### 7.4 SDA, SD0, SD1, SD2, SD3 — data signal inputs/outputs

The data signal buffers are bidirectional. The port (SDA, or any one of SD0 to SD3) which first falls LOW, will decide the direction of this buffer and 'lock out' signals coming from the opposite side. As the 'input' signal continues to fall, it will then drive the open-drain of the 'output' side LOW. Again, hysteresis is applied to the buffer to minimize the effects of noise. Ports are open-drain type and require external pull-up resistors.

At some points during the communication, the data direction will reverse—for example, when the slave transmits an acknowledge (ACK) or responds with its register contents. During these times, the controlling 'input' side will have to rise to  $V_{unlock}$  before it releases the 'lock', which then allows the 'output' side to gain control, and pull (what was) the 'input' side LOW again. This will cause a 'pulse' on the 'input' side, which can be quite long duration in high capacitance buses. However, this pulse will not interfere with the actual data transmission, as it should not occur during times of clock line transition (during normal I<sup>2</sup>C-bus and SMBus protocols), and thus data signal set-up time requirements are still met.

**7.5 RESET — reset IC to default state**

The active LOW  $\overline{\text{RESET}}$  input is used to disable the buffer, and reset it to its default state. The IC should only be disabled when the bus is idle to avoid truncation of commands which may confuse other devices on the bus.

The  $\overline{\text{RESET}}$  signal will clear the contents of the Control register, which has the effect of disabling all output lines SC[0:3] and SD[0:3]. It is the nature of the I<sup>2</sup>C-bus protocol that devices may become ‘stuck’. To help in the clearing of this condition, the PCA9646 can be reset, and each port brought on-line successively to find the component holding the bus LOW.

**7.6 Power-On Reset (POR)**

During power-on, the PCA9646 is internally held in the reset condition for a maximum of  $t_{rst} = 500$  ns. The default condition after reset is for the Control register to be erased (all zeros), resulting in all output channels being disabled.

**7.7 A0, A1, A2 — address lines**

The slave address of the PCA9646 is shown in Figure 4. The address pins (A2, A1, A0) must be driven to a HIGH or LOW level—they are not internally pulled to a default state.

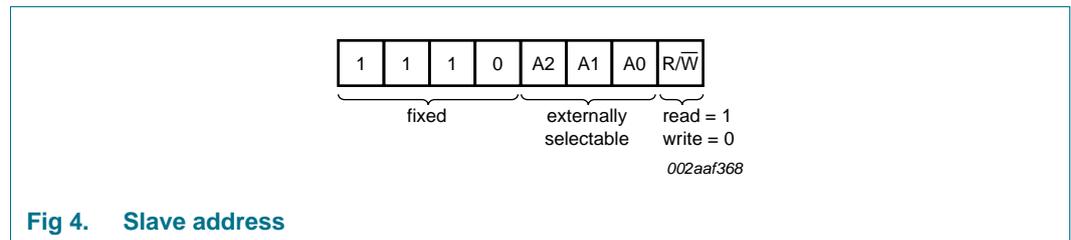


Fig 4. Slave address

The read/write bit must be set LOW to enable a write to the Control register, or HIGH to read from the Control register.

**7.8 Control register**

The Control register of the PCA9646 is shown in Figure 5. Each of the four output channels (SCn/SDn pairs) can be enabled independently, and the direction of the clock signal can be reversed.

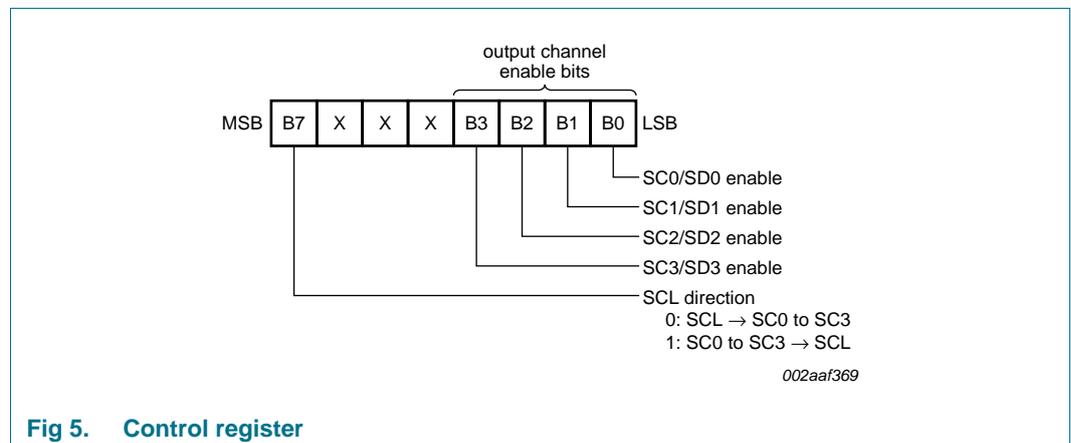


Fig 5. Control register

A LOW or 'zero' bit (B[3:0]) indicates that the respective channel (SC[3:0], SD[3:0]) is disabled. The default reset condition of the register is all zeros, all channels disabled, forward direction. A HIGH or 'one' bit indicates the respective channel is enabled.

Example: B3 = 1, B2 = 0, B1 = 1, B0 = 0 means channel 3 (SC3/SD3) and channel 1 (SC1/SD1) are enabled, and channel 2 (SC2/SD2) and channel 0 (SC0/SD0) are disabled.

As each channel is individually buffered, the loads on each are isolated, and therefore there is no special requirement to keep the sum of the collective capacitances below the maximum bus capacitance. Instead, each line may have up to the maximum bus capacitance and be enabled or disabled without affecting the performance of the other channels.

The Most Significant Bit (MSB) B7 is used to set the direction of the SCL (clock) signal. The default state is LOW (zero). In this state, the SCL port will act as the input, and the IC will supply a buffered signal to any of the four output channels (SC0 to SC3) which are enabled. When B7 is set HIGH (one), the clock signal direction is reversed. The ports SC0 to SC3 act as inputs, the ANDed combination of the selected signals is buffered and output on the SCL pin.

The PCA9646 is always addressable from the SCL/SDA side, regardless of the state of B7. Any device which can communicate data to the SCL/SDA pins, either by being directly attached to those pins or by transmitting through the PCA9646 (when B7 = 1), may address the device and change the control register's contents. The Control register is only updated upon receipt of the STOP condition.

## 8. Bus transaction

A typical I<sup>2</sup>C-bus write transaction to the PCA9646 is shown in [Figure 6](#). A typical read transaction is shown in [Figure 7](#).

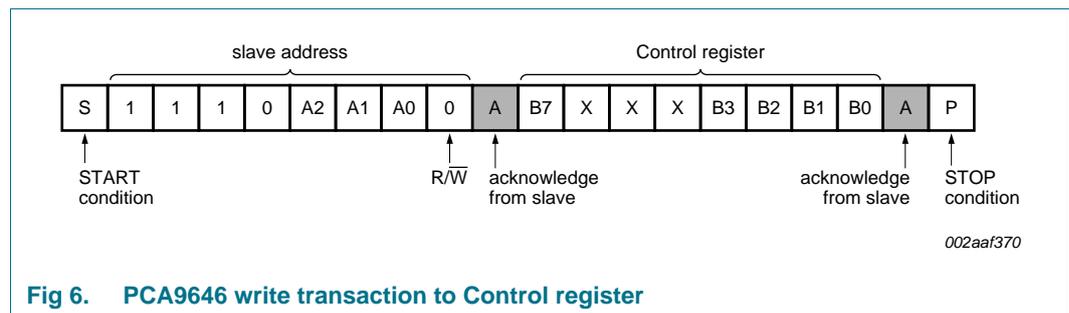


Fig 6. PCA9646 write transaction to Control register

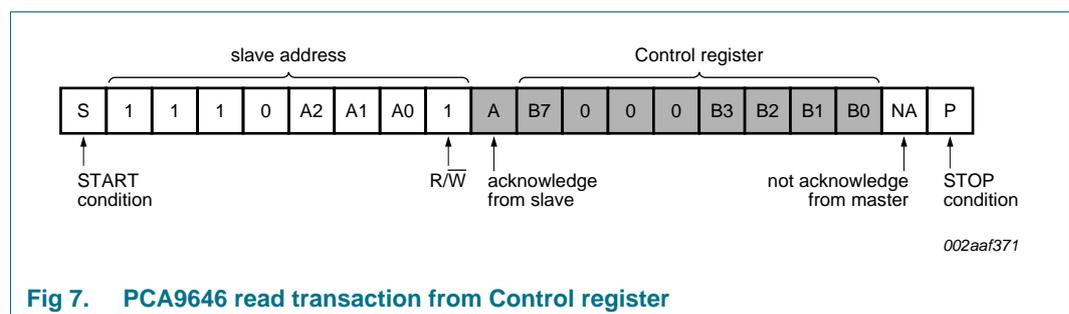


Fig 7. PCA9646 read transaction from Control register

## 9. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		[1] -0.3	+7	V
$V_{I/O}$	voltage on an input/output pin	pins SDx, SCx	[1] $V_{SS} - 0.5$	+7	V
$V_I$	input voltage	$\overline{RESET}$ pin	[1] $V_{SS} - 0.5$	$V_{DD} + 0.5$	V
		address pins A2, A1, A0	[1] $V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$I_I$	input current	pins other than SCx/SDx	-	20	mA
		all SCx and SDx	-	40	mA
$I_{SS}$	ground supply current		-	280	mA
$P_{tot}$	total power dissipation		-	300	mW
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	ambient temperature	operating	-40	+85	°C

[1] Voltages are specified with respect to pin 8 ( $V_{SS}$ ).

## 10. Characteristics

**Table 4. Characteristics**

$T_{amb} = -40$  °C to +85 °C; voltages are specified with respect to ground ( $V_{SS}$ );  $V_{DD} = 5.5$  V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power supply</b>						
$V_{DD}$	supply voltage	operating	2.7	-	5.5	V
$I_{DD}$	supply current	quiescent; $V_I$ ( $\overline{RESET}$ pin) = 0 V	-	-	1	μA
<b>I<sup>2</sup>C-bus ports (SCL, SDA, SC[3:0], SD[3:0])</b>						
$V_{I2C-bus}$	I <sup>2</sup> C-bus voltage	SDx, SCx	-	-	5.5	V
$V_{IL}$	LOW-level input voltage	$V_{DD} = 2.7$ V	[1] -	-	0.4	V
		$V_{DD} = 5.5$ V	[1] -	-	0.5	V
$V_{IH}$	HIGH-level input voltage	$V_{DD} = 2.7$ V	[1] 1.2	-	-	V
		$V_{DD} = 5.5$ V	[1] 2.0	-	-	V
$V_{I(hys)}$	hysteresis of input voltage	$V_{DD} = 2.7$ V	[1] 80	-	-	mV
		$V_{DD} = 5.5$ V	[1] 200	-	-	mV
$I_{LI}$	input leakage current	pin at $V_{DD}$ or $V_{SS}$	-1	-	+1	μA
$I_{O(sink)}$	output sink current	LOW-level; $V_{Sxx}$ input < $V_{IL}$	30	-	-	mA
$V_{OL}$	LOW-level output voltage	$I_{OL} = 30$ mA; $V_{DD} = 2.7$ V	-	260	450	mV
		$I_{OL} = 30$ mA; $V_{DD} = 5.5$ V	-	140	275	mV
<b>Pins SDA, SD0, SD1, SD2, SD3</b>						
$V_{lock}$	direction lock voltage	$V_{DD} = 2.7$ V	[1] -	-	1.3	V
		$V_{DD} = 5.5$ V	[1] -	-	3.0	V
$V_{unlock}$	direction unlock voltage	$V_{DD} = 2.7$ V	[1] 2.0	-	-	V
		$V_{DD} = 5.5$ V	[1] 4.8	-	-	V

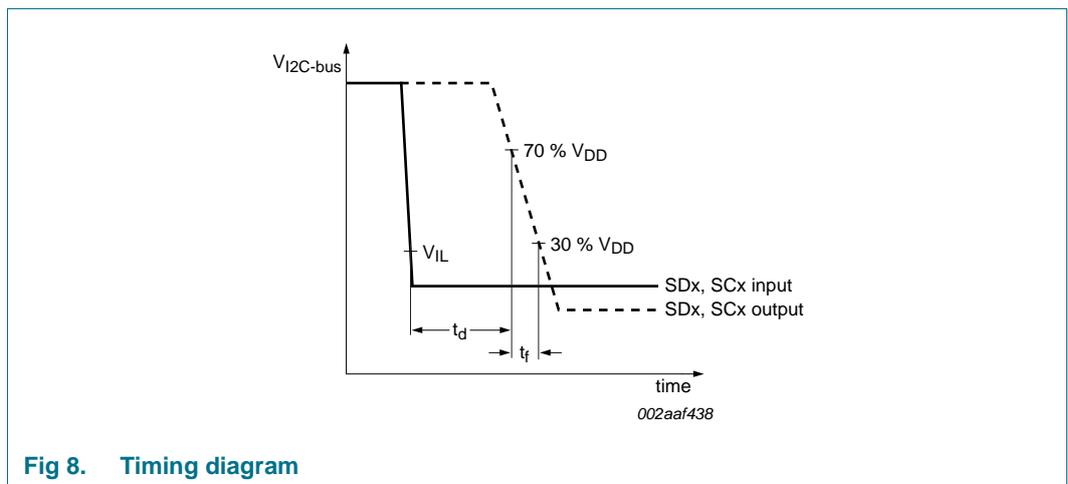
**Table 4. Characteristics ...continued**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ; voltages are specified with respect to ground ( $V_{SS}$ );  $V_{DD} = 5.5\text{ V}$  unless otherwise specified.

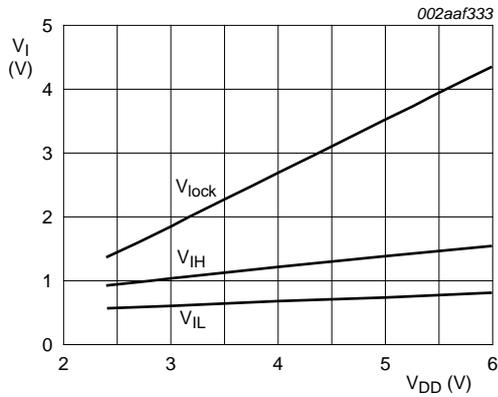
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>RESET</b>						
$V_{IH}$	HIGH-level input voltage	$V_{DD} = 2.7\text{ V}$	2.0	-	-	V
		$V_{DD} = 5.5\text{ V}$	4.8	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{DD} = 2.7\text{ V}$	-	-	650	mV
		$V_{DD} = 5.5\text{ V}$	-	-	900	mV
$V_{hys}$	hysteresis voltage	$V_{DD} = 2.7\text{ V}$	100	-	-	mV
		$V_{DD} = 5.5\text{ V}$	200	-	-	mV
$I_{LI}$	input leakage current	pin at $V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$t_{w(\text{rst})L}$	LOW-level reset time	$V_I < V_{IL}$	[2]	25	-	ns
$t_{rst}$	reset time	$\overline{\text{RESET}}$ pin; from $V_I > V_{IH}$	-	250	500	ns
$t_{POR}$	power-on reset pulse time	$\overline{\text{RESET}}$ pin; from $V_I > V_{IH}$	-	250	500	ns
<b>Address pins (A0, A1, A2)</b>						
$V_{IH}$	HIGH-level input voltage	$V_{DD} = 2.7\text{ V}$	1.7	-	-	V
		$V_{DD} = 5.5\text{ V}$	3.5	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{DD} = 2.7\text{ V}$	-	-	0.7	V
		$V_{DD} = 5.5\text{ V}$	-	-	1.5	V
$I_{LI}$	input leakage current	pin at $V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
<b>Timing characteristics (Figure 8)</b>						
$t_d$	delay time	$R_{PU} = 200\ \Omega$ ; $V_{DD} = 2.7\text{ V}$	-	100	-	ns
		$R_{PU} = 200\ \Omega$ ; $V_{DD} = 5.5\text{ V}$	-	70	-	ns
$t_f$	fall time	$R_{PU} = 200\ \Omega$	-	16	-	ns

[1] Supply voltage dependent; refer to graphs (Figure 9 through Figure 12) for typical trend.

[2] Guaranteed by design, not subject to test.



**Fig 8. Timing diagram**



$T_{amb} = 25\text{ °C}$

Fig 9. Typical input levels versus supply voltage

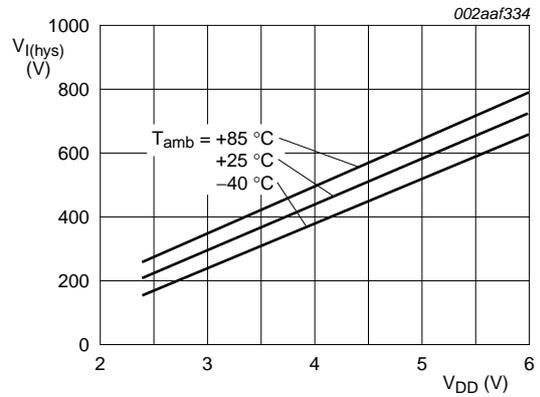
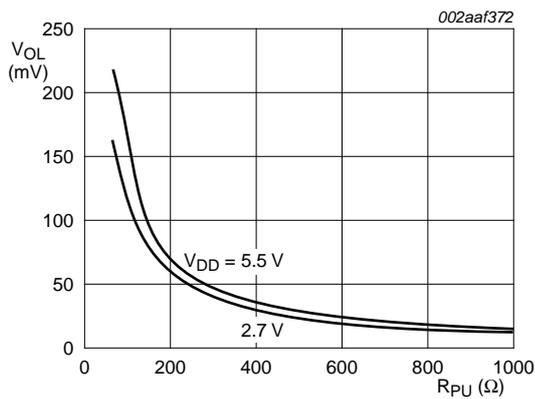
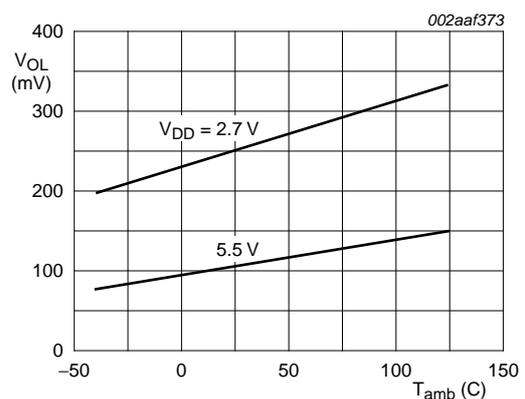


Fig 10. Typical  $V_{IH} - V_{IL}$  hysteresis versus supply voltage



$T_{amb} = 25\text{ °C}$

Fig 11. Typical LOW-level output voltage versus pull-up resistance



$I_{OL} = 30\text{ mA}$

Fig 12. Typical LOW-level output voltage versus ambient temperature

## 11. Application information

Figure 13 shows a typical data transfer through the PCA9646. The PCA9646 has excellent application to extending loads and expanding the address space of slave devices. Rise times are determined simply by the side of the buffer with the slowest RC time constant.

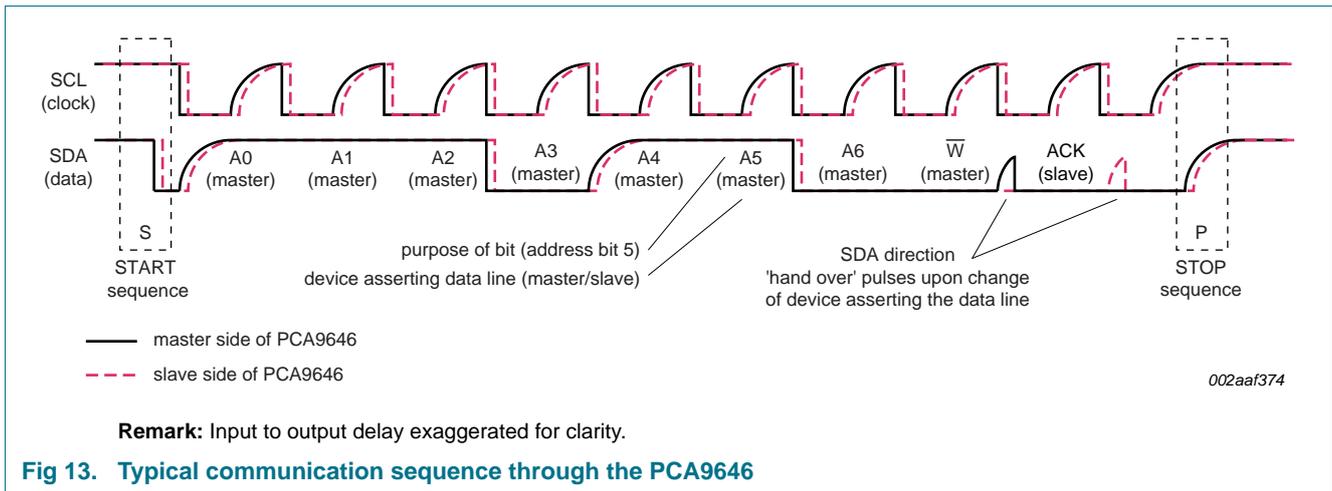


Fig 13. Typical communication sequence through the PCA9646

Figure 14 shows a typical application for the PCA9646. Each channel can support up to the maximum permissible capacitance load, thus the maximum loading of the system can be 5 times that which could be achieved without buffering.

The channel enable function can be used to interface buses of different operating frequencies. When certain bus sections are enabled, the system frequency may be limited by a bus section having a slave device specified only to 100 kHz. When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow the PCA9646 to run in excess of the 1 MHz maximum limit of the I<sup>2</sup>C-bus Fast-mode Plus (Fm+), or to run a huge 4 nF load at 100 kHz.

Figure 15 shows the PCA9646 used as a line driver. Four such lines (only one shown) can be run from the same device. The receiving end may then again be used as a 4-way bus switch, radiating out into another four lines.

Using the address pins, this entire structure may be repeated. Thus a total of eight PCA9646 'line drivers' may be connected to a single bus master (U1), allowing for 32 (8 × 4) long distance bus pairs to be driven from the one I<sup>2</sup>C-bus port.

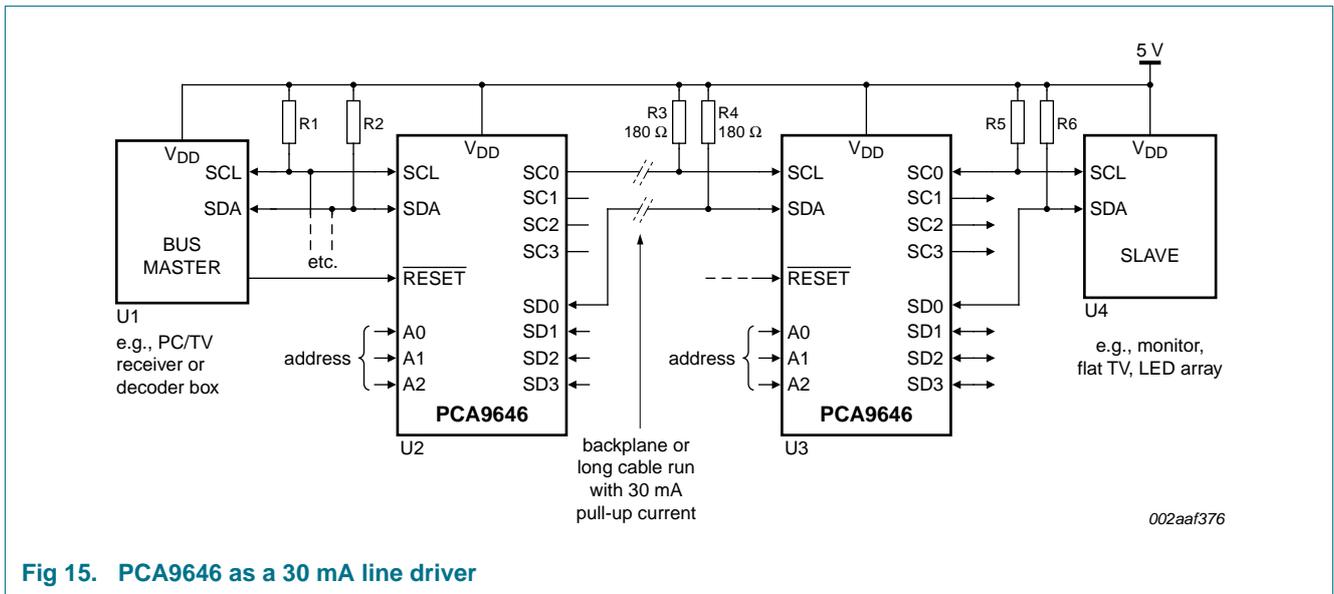
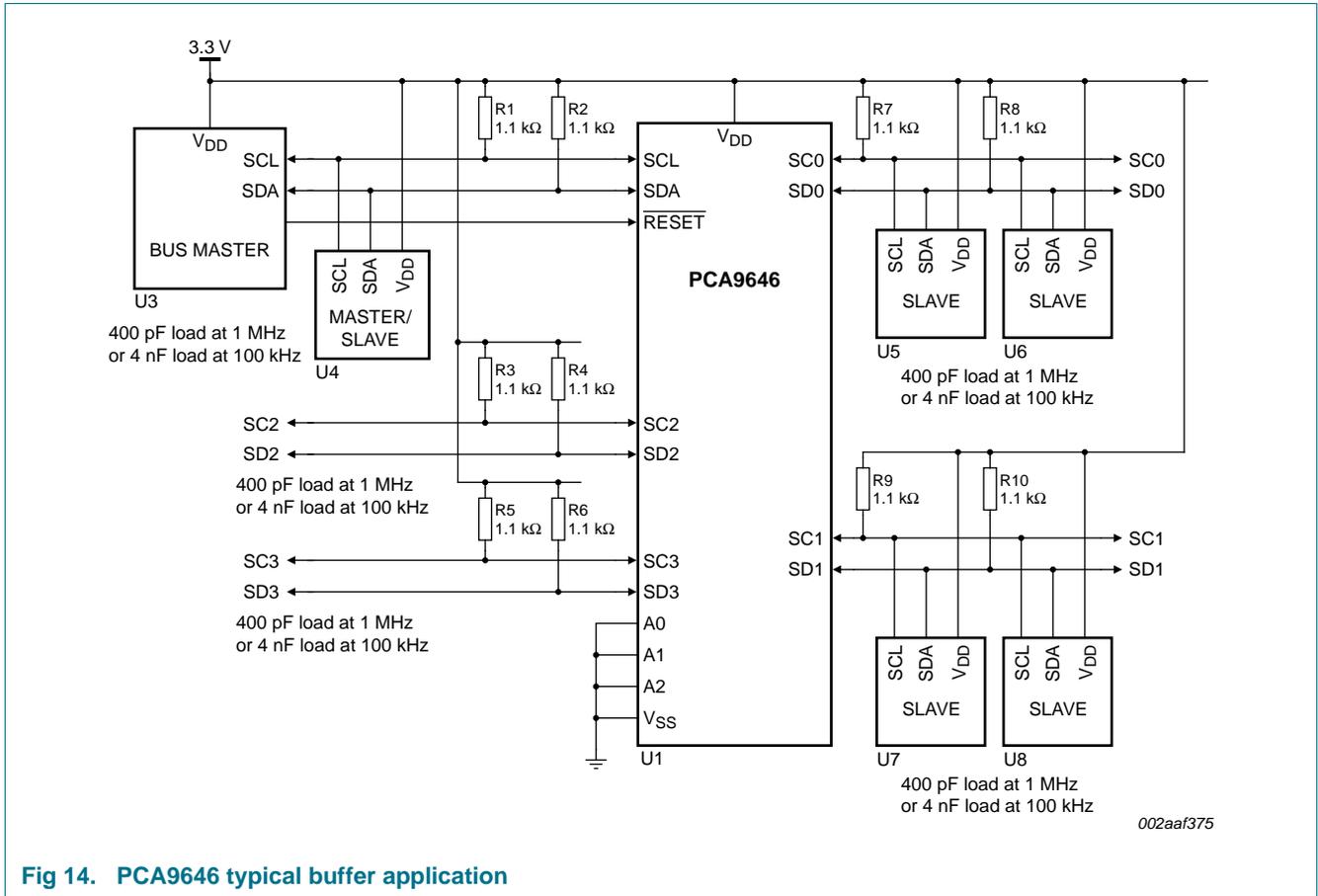
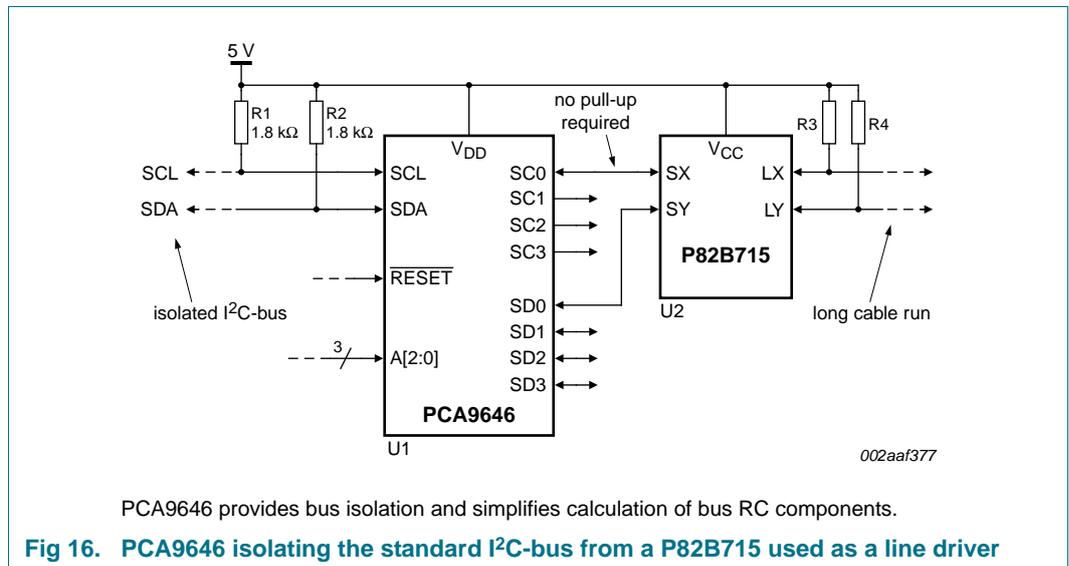
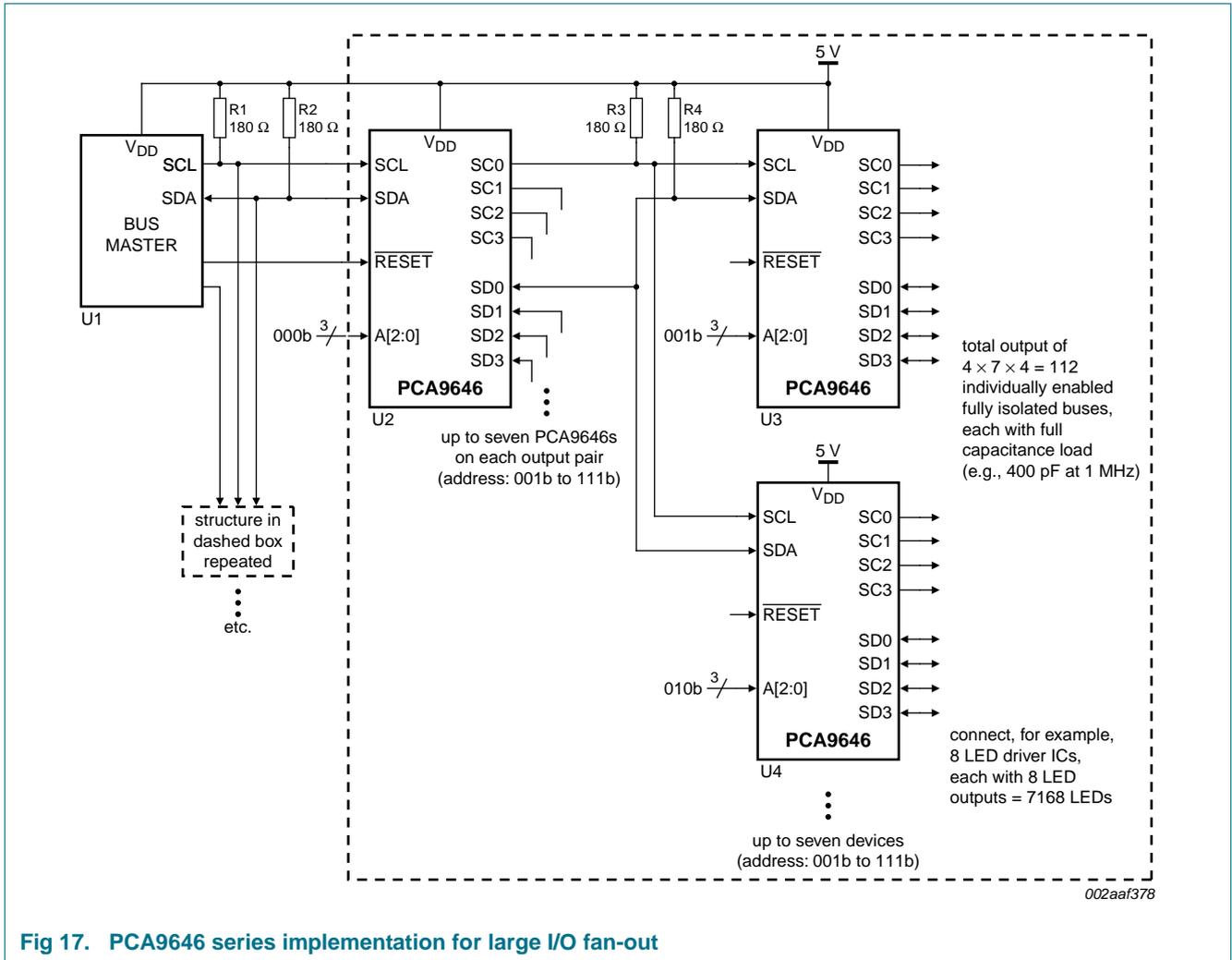


Figure 16 shows how PCA9646 can be used to combine or extend existing long cable systems using P82B715 I<sup>2</sup>C-bus extenders when they have reached their maximum capacitance limit. P82B715 alone provides a '10× impedance transformation' (Ref. 2) but no isolation of the loadings on either side. P82B715 systems have a finite capacitance limit and its system calculations can be relatively complex. The buffering action of PCA9646 simplifies calculations and allows the isolated bus rise time to meet the Fast-mode requirement even when that is not possible on the long cable section.

Of course it is possible to create a much larger system by connecting existing long P82B715 cable systems to each of the four channels and driving all of them from one isolated Master.



The PCA9646 may also be driven in series. [Figure 17](#) shows this configuration. In this scenario, each of the four outputs of the first device (U2) has six more PCA9646's connected to it. Each of those six devices has four outputs, thus giving  $4 \times 7 \times 4 = 112$  outputs. If the RESET pin on U2 was also driven from the master, it would be possible to reproduce this entire structure multiple times, giving a truly massive address space capability. Such a configuration may be applied to situations such as display drivers.



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

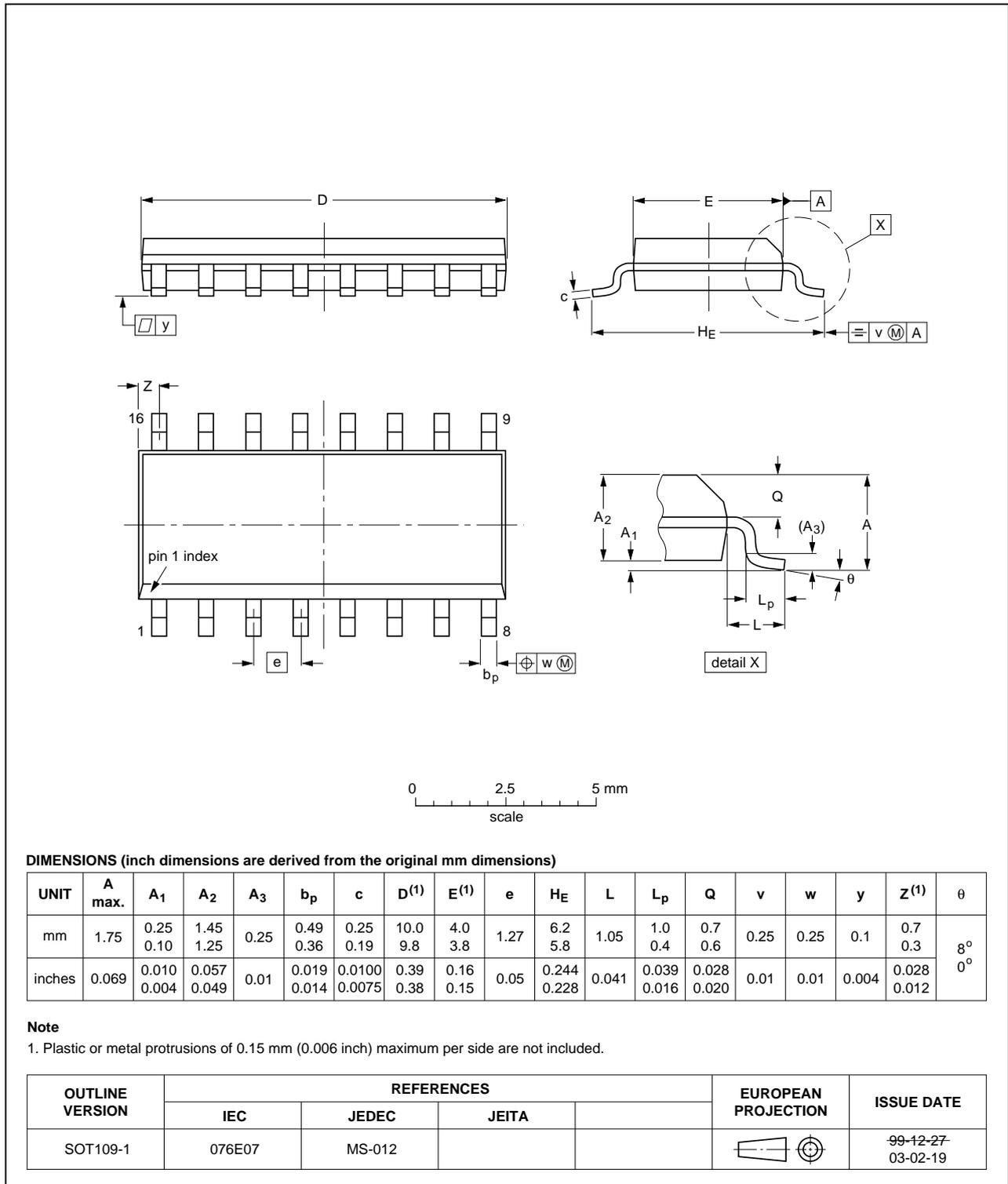


Fig 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

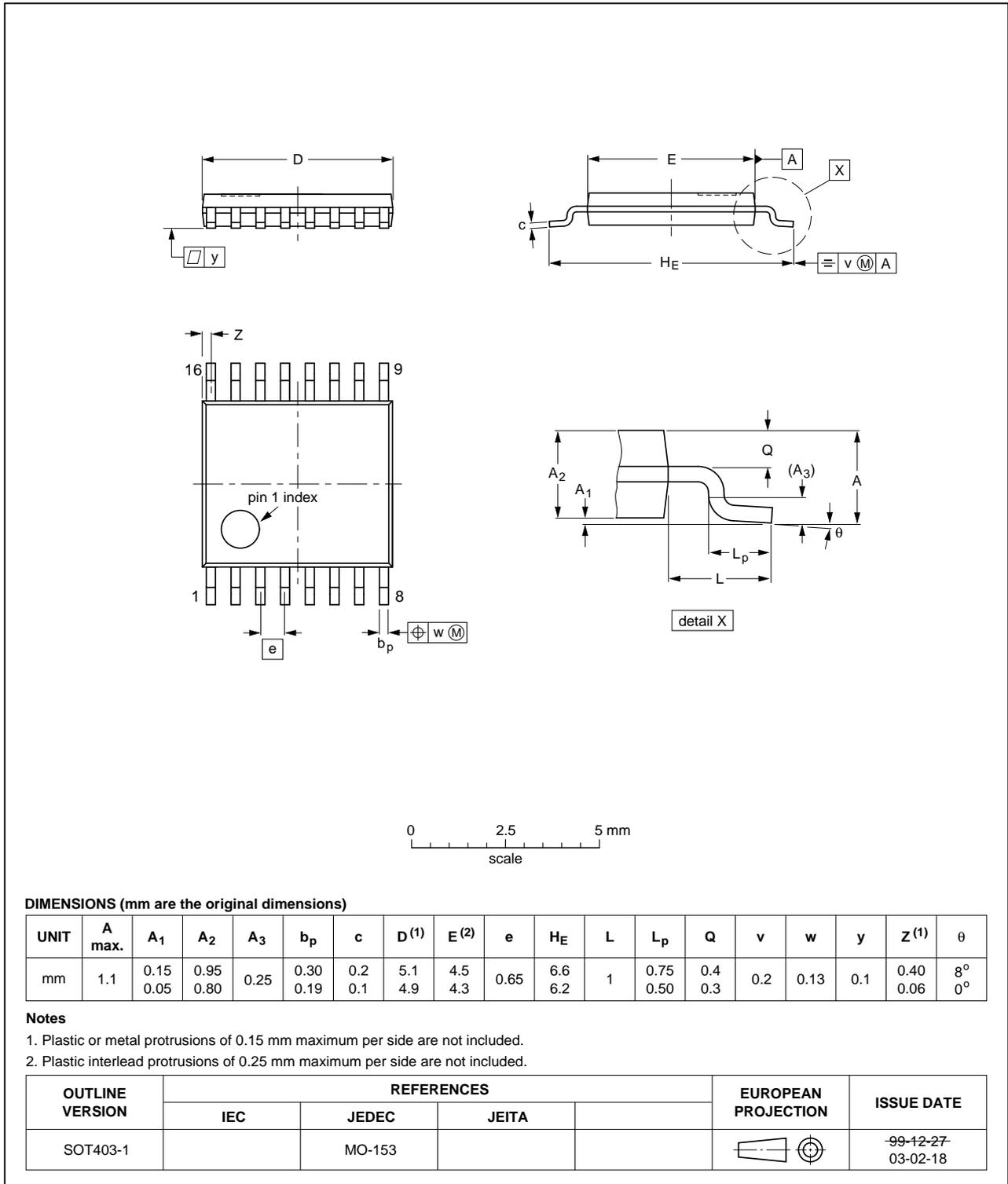


Fig 19. Package outline SOT403-1 (TSSOP16)

## 13. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#) and [6](#)

**Table 5. SnPb eutectic process (from J-STD-020C)**

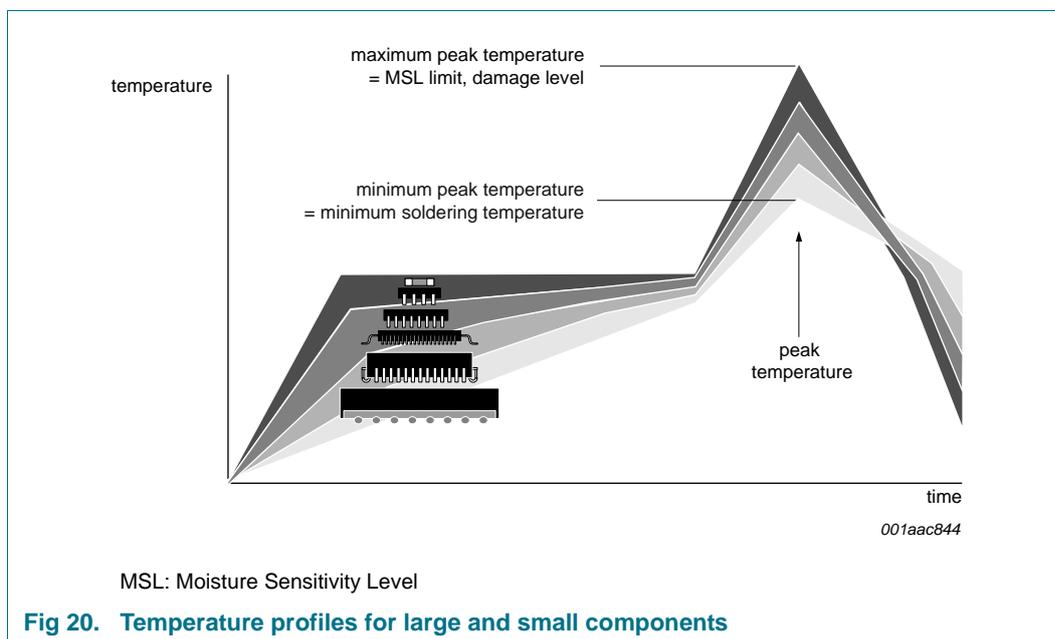
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 6. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 7. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
LED	Light-Emitting Diode
MSB	Most Significant Bit
PMBus	Power Management Bus
RAID	Redundant Array of Independent Discs
RC	Resistor-Capacitor network
SMBus	System Management Bus

## 16. References

- [1] **UM10204, “I<sup>2</sup>C-bus specification and user manual”** — NXP Semiconductors; [www.nxp.com/documents/user\\_manual/UM10204.pdf](http://www.nxp.com/documents/user_manual/UM10204.pdf)
- [2] **P82B715, I<sup>2</sup>C-bus extender** — NXP Semiconductors; Product data sheet; [www.nxp.com/documents/data\\_sheet/P82B715.pdf](http://www.nxp.com/documents/data_sheet/P82B715.pdf)

## 17. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9646 v.1	20110301	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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