

# PHD/PHU77NQ03T

N-channel TrenchMOS FET

Rev. 01 — 28 November 2006

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Fast switching
- Low thermal resistance

### 1.3 Applications

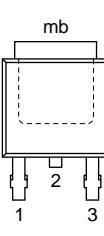
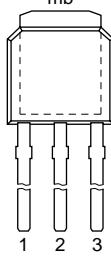
- DC-to-DC converters
- Computer motherboard

### 1.4 Quick reference data

- $V_{DS} \leq 25$  V
- $I_D \leq 75$  A
- $R_{DSon} \leq 9.5$  m $\Omega$
- $Q_{GD} = 3.2$  nC (typ)

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)	[1]	
3	source (S)		
mb	mounting base; connected to drain (D)		 SOT533 (IPAK)

[1] It is not possible to make a connection to pin 2 of the SOT428 package.

### 3. Ordering information

**Table 2. Ordering information**

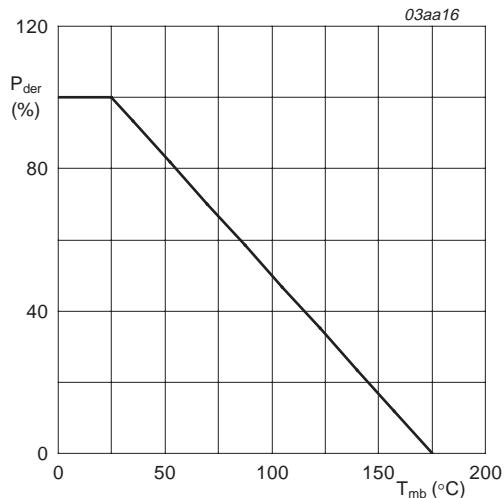
Type number	Package	Description	Version
Name			
PHD77NQ03T	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428
PHU77NQ03T	IPAK	plastic single-ended package; 3 leads (in-line)	SOT533

### 4. Limiting values

**Table 3. Limiting values**

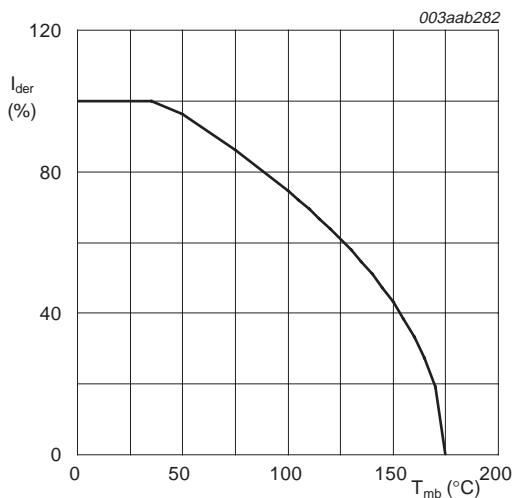
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$	-	25	V
$V_{DGR}$	drain-gate voltage (DC)	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}; R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{mb} = 25^{\circ}\text{C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	75	A
		$T_{mb} = 100^{\circ}\text{C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	55.9	A
$I_{DM}$	peak drain current	$T_{mb} = 25^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$ ; see <a href="#">Figure 1</a>	-	107	W
$T_{stg}$	storage temperature		-55	+175	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	+175	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25^{\circ}\text{C}$	-	75	A
$I_{SM}$	peak source current	$T_{mb} = 25^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 32\text{ A}$ ; $t_p = 0.17\text{ ms}$ ; $V_{DS} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25^{\circ}\text{C}$	-	100	mJ



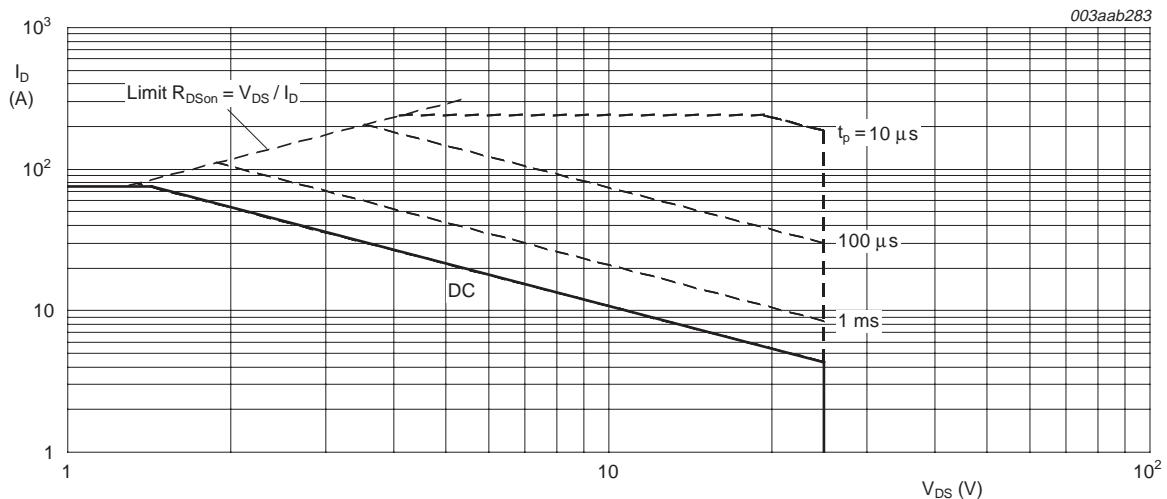
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}C)} \times 100 \%$$

**Fig 1.** Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}C)} \times 100 \%$$

**Fig 2.** Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

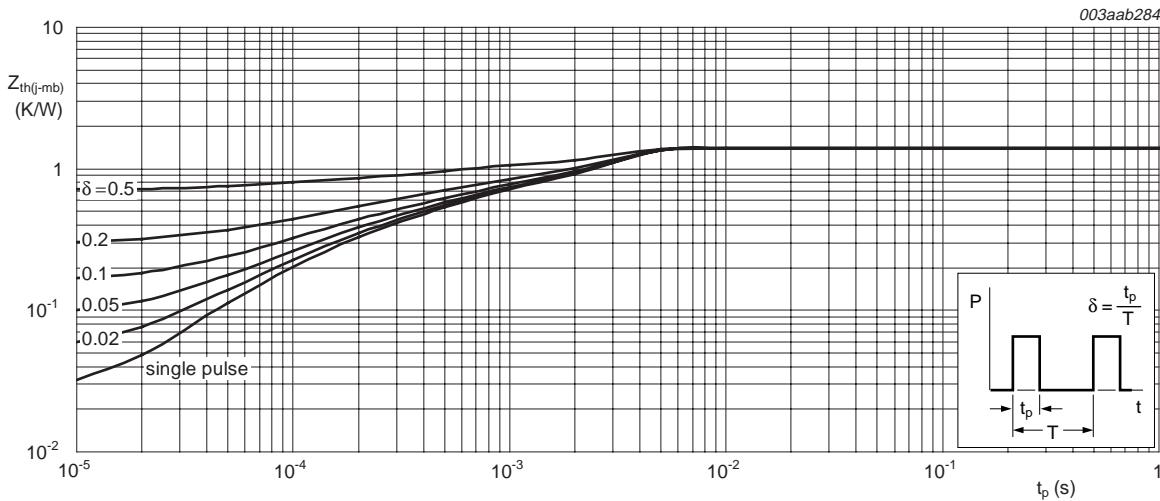
**Fig 3.** Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.4	K/W	
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient						
	SOT428	minimum footprint	[1]	-	75	-	K/W
		SOT404 minimum footprint	[1]	-	50	-	K/W
	SOT533	vertical in free air	-	70	-	K/W	

[1] Mounted on a printed-circuit board; vertical in still air.

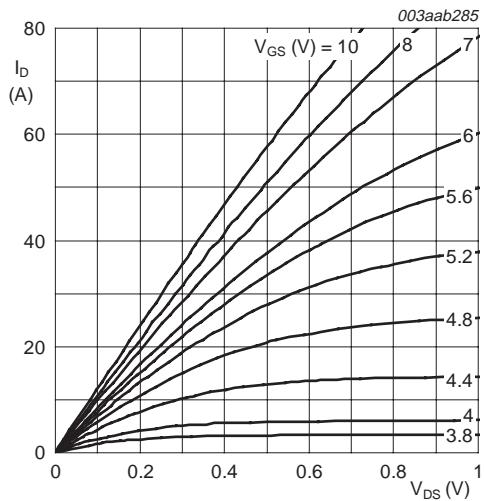


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

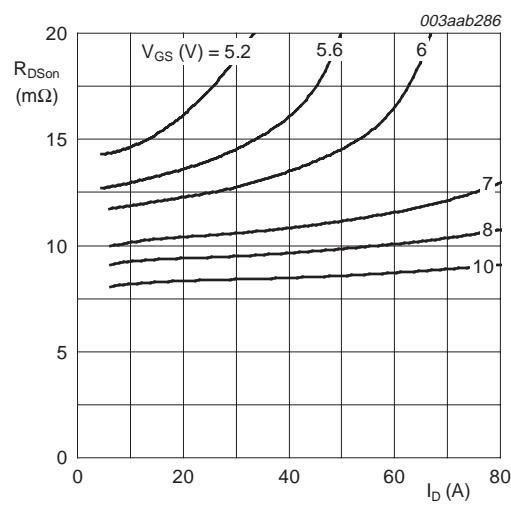
**Table 5. Characteristics** $T_j = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = -55^\circ\text{C}$	25	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a> $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2.1 1.35 -	2.65 - -	3.2 - 3.65	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}$ $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	- -	- -	10 500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$	- -	- -	100	nA
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.2	-	$\Omega$
$R_{DS\text{on}}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a> $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	- -	8.3 15	9.5 17.1	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	17.1	-	nC
$Q_{GS}$	gate-source charge		-	6	-	nC
$Q_{GS1}$	pre- $V_{GS(\text{th})}$ gate-source charge		-	3.2	-	nC
$Q_{GS2}$	post- $V_{GS(\text{th})}$ gate-source charge		-	2.8	-	nC
$Q_{GD}$	gate-drain charge		-	3.2	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage		-	5	-	V
$Q_{G(\text{tot})}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 4.5 \text{ V}$	-	6.2	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 12 \text{ V}; f = 1 \text{ MHz}$ ; see <a href="#">Figure 14</a>	-	860	-	pF
$C_{oss}$	output capacitance		-	400	-	pF
$C_{rss}$	reverse transfer capacitance		-	165	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 0 \text{ V}; f = 1 \text{ MHz}$	-	1200	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 10 \text{ V}; R_G = 5.6 \Omega$	-	8.3	-	ns
$t_r$	rise time		-	7.6	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	24.8	-	ns
$t_f$	fall time		-	6.6	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}$ ; see <a href="#">Figure 13</a>	-	0.9	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}$	-	34	-	ns
$Q_r$	recovered charge		-	12.5	-	nC



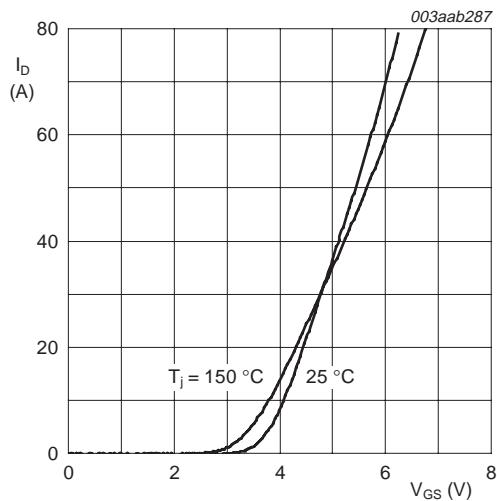
$T_j = 25^\circ\text{C}$

**Fig 5.** Output characteristics: drain current as a function of drain-source voltage; typical values



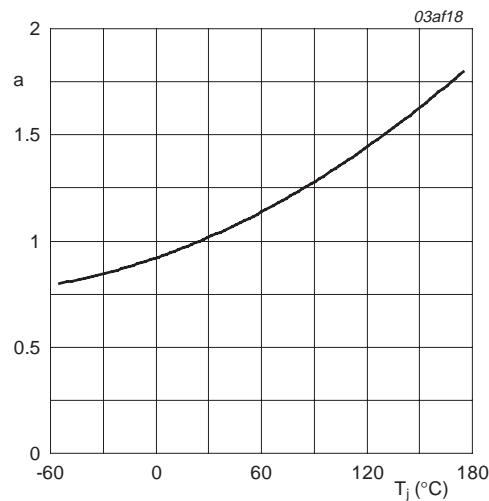
$T_j = 25^\circ\text{C}$

**Fig 6.** Drain-source on-state resistance as a function of drain current; typical values



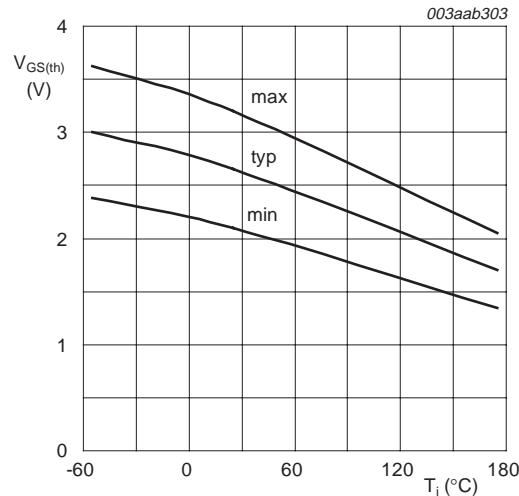
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7.** Transfer characteristics: drain current as a function of gate-source voltage; typical values



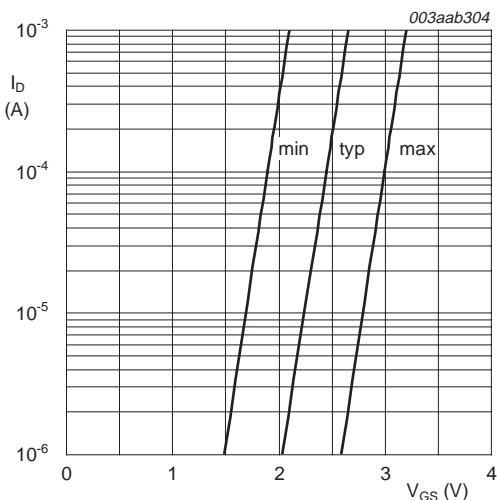
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig 8.** Normalized drain-source on-state resistance factor as a function of junction temperature



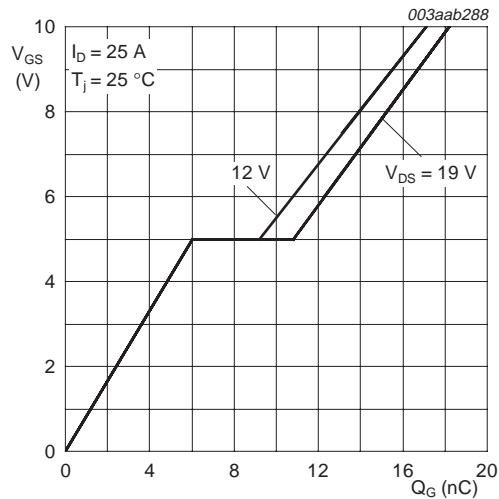
I<sub>D</sub> = 1 mA; V<sub>DS</sub> = V<sub>GS</sub>

**Fig 9.** Gate-source threshold voltage as a function of junction temperature



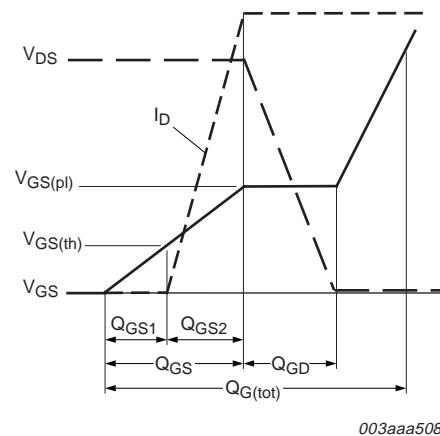
T<sub>j</sub> = 25 °C; V<sub>DS</sub> = 5 V

**Fig 10.** Sub-threshold drain current as a function of gate-source voltage

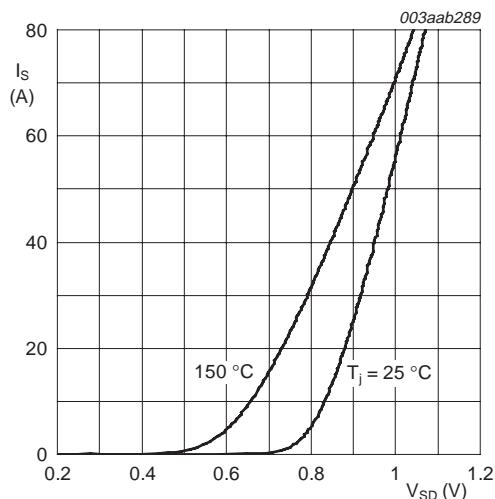


I<sub>D</sub> = 25 A; V<sub>DS</sub> = 12 V and 19 V

**Fig 11.** Gate-source voltage as a function of gate charge; typical values

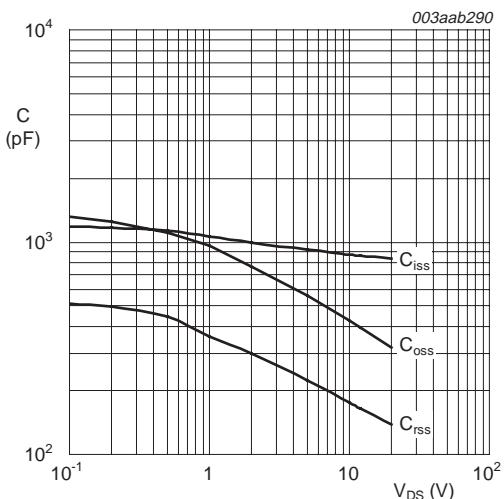


**Fig 12.** Gate charge waveform definitions



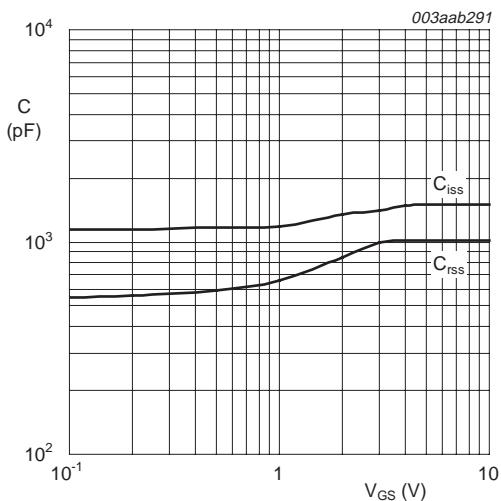
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



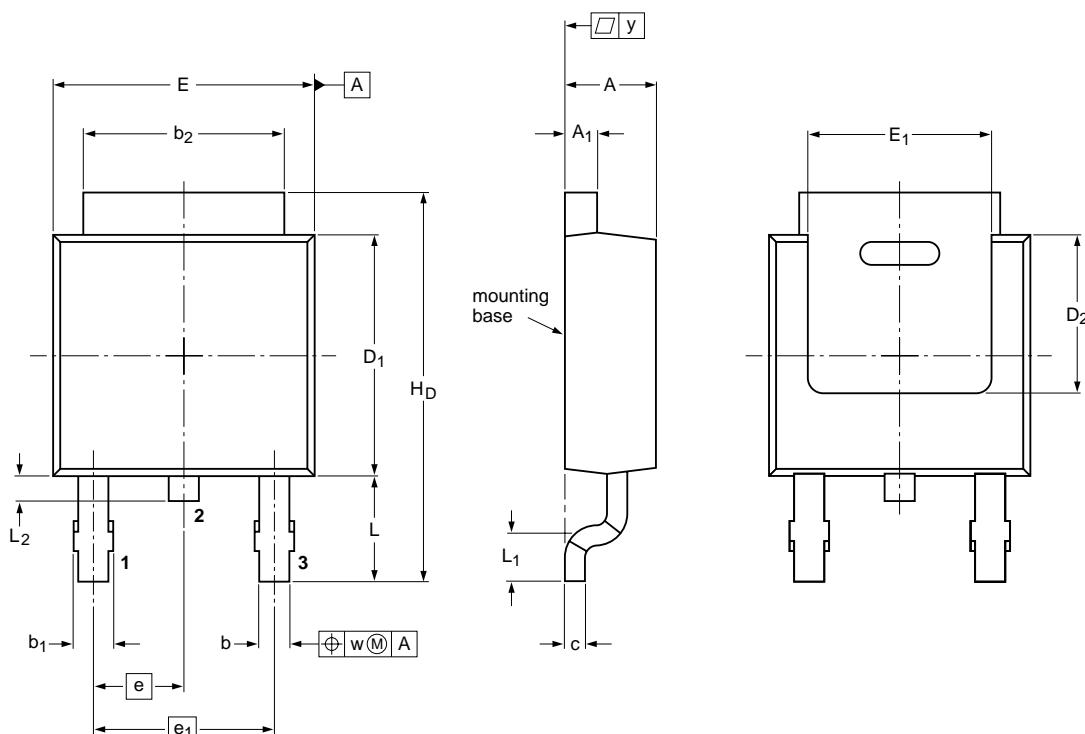
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**

## 7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428



0 5 10 mm  
scale

### DIMENSIONS (mm are the original dimensions)

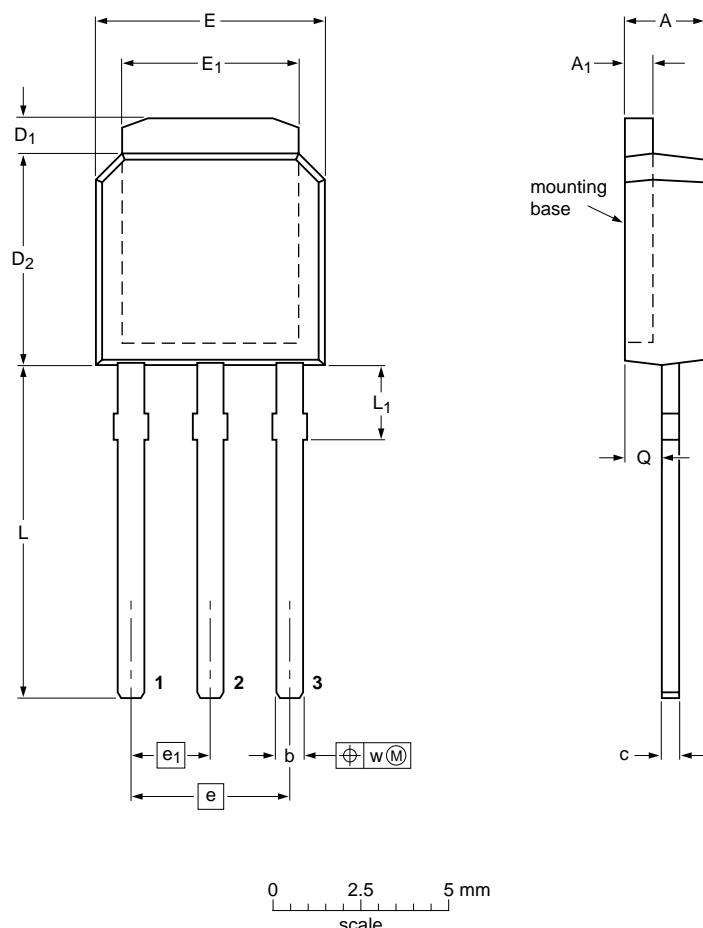
UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sub>1</sub>	D <sub>2</sub> min	E	E <sub>1</sub> min	e	e <sub>1</sub>	H <sub>D</sub>	L	L <sub>1</sub> min	L <sub>2</sub>	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			-06-02-14 06-03-16

Fig 16. Package outline SOT428 (DPAK)

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533



## DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(2)</sup> max	Q	w
mm	2.38 2.22	0.93 0.46	0.89 0.71	0.56 0.46	1.10 0.96	6.22 5.98	6.73 6.47	5.21 5.00	4.57 BSC <sup>(1)</sup>	2.285 BSC <sup>(1)</sup>	9.6 9.2	2.7	1.1 1.0	0.3

## Notes

1. Basic spacing between centers.
2. Terminal dimensions are uncontrolled within zone L<sub>1</sub>.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT533		TO-251				-05-02-11 06-02-14

Fig 17. Package outline SOT533 (IPAK)

## 8. Revision history

**Table 6. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD_PHU77NQ03T_1	20061128	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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