

IP4310CX8/P

Integrated HDMI interface biasing and ESD protection to IEC61000-4-2, level 4

13 October 2009

Product data sheet

1. Product profile

1.1 General description

The IP4310CX8/P is an ESD protection and biasing device for the non-high-speed channels of the HDMI interface. The device provides protection to downstream components from Electrostatic Discharge (ESD) voltages as high as ± 15 kV contact discharge, far exceeding IEC61000-4-2, level 4. The device is fabricated using monolithic silicon technology and integrates three resistors and several low capacitance, high-level ESD-protection diodes in a single *Wafer-Level* chip-scale package. These features make the IP4310CX8/P ideal for use in applications requiring component miniaturization, such as mobile phone handsets.

1.2 Features

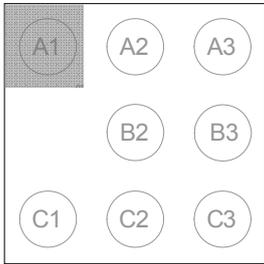
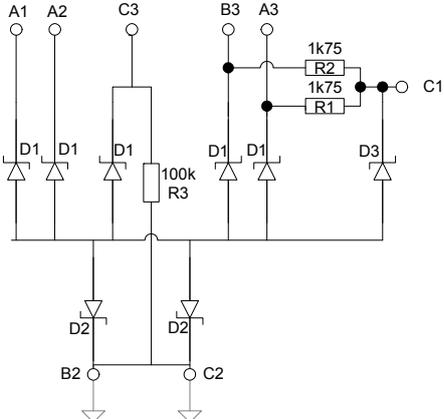
- Pb-free, RoHS compliant and free of Halogen and Antimony (dark green compliant)
- 2 x 1.75 k Ω , 1x 100 k Ω biasing resistors with integrated ESD-protection
- 2 separated back-to-back ESD protection diodes
- Downstream ESD protection up to ± 15 kV (contact) according IEC61000-4-2
- Wafer-Level chip-scale package with 0.4 mm pitch

1.3 Applications

- HDMI non-high-speed interfaces channels in e.g. Cellular and PCS mobile handsets
- DDC, hot plug and CEC line biasing and ESD protection in space constrained appliances

2. Pinning information

Table 1. Pinning IP4310CX8/P

Pin	Description	Simplified outline	Symbol
IP4310CX8/P			
A1	ESD-protection	 <p>Transparent top view WLCSP8</p>	
A2	ESD-protection		
B2, C2	Ground		
C3	Hot plug, ESD-protection		
B3	DDC communication, ESD-protection		
A3	DDC communication, ESD-protection		
C1	Power supply for DDC pull-up resistors		

3. Limiting values

Table 2. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	DC input voltage range for input or output pins		-5.5	+5.5	V
ESD	Electrostatic Discharge All pins to ground (B2&C2)	IEC 61000-4-2, Level 4,			
		Contact	-8 (-15) ¹	+8 (+15) ¹	kV
		Air Discharge	-15	+15	kV
P_{D-ch}	Maximum continuous power dissipation per channel	@ 70 °C		20	mW
T_{stg}	storage temperature range		-55	+150	°C
T_{pk}	Peak solder reflow temperature	10 seconds max.		+260	°C
T_{amb}	Ambient operating temperature		-30	+85	°C

4. Electrical Characteristics

Table 3. Electrical characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R1, R2	Resistor value		1.575	1.75	1.925	k Ω
R3	Resistor value		80	100	120	k Ω
C_{line}	Line capacitance value All pins to ground (B2, D2)	$V_{dc} = 0\text{ V}$; $f = 100\text{ kHz}$, $V_{ac} = 0.15\text{ V}_{rms}$ all other pins connected to GND				
			8.0	10.0	12.0	pF
		Line capacitance value under HDMI compliance test conditions All pins to ground (B2, D2)	$V_{dc} = 2.5\text{ V}$; $f = 100\text{ kHz}$, $V_{ac} = 3.5\text{ V}_{p-p} = (1.25\text{ V}_{rms})$ all other pins connected to GND			
			4.8	6	7.2	pF
$V_{(BR)}$	Diode breakdown voltage	$I_{test} = 1\text{ mA}$	6	-	11	V
		$I_{test} = -1\text{ mA}$	-11	-	-6	V
I_{lkg}	Diode leakage current ²	$V = +3\text{ V}$	-	-	+50	nA
		$V = -3\text{ V}$	-50	-	-	nA

¹ Device is qualified using 1000 pulses of $\pm 15\text{ kV}$ contact discharges each, according to the IEC61000-4-2 model and far exceeds the specified level 4 (8kV contact discharge).

² The leakage for pin C3 cannot be measured due to the 100k Ω resistor. Pins B3, A3 and C1 have to be measured together

5. Application information

5.1 Cross-talk

The setup for cross-talk measurement in a 50 Ω system from one channel to another is shown in Fig 1. Four typical cross-talk measurement results are depicted in Fig 2. Channels not shown there behave similar. Unused channels are terminated with 50 Ω to ground

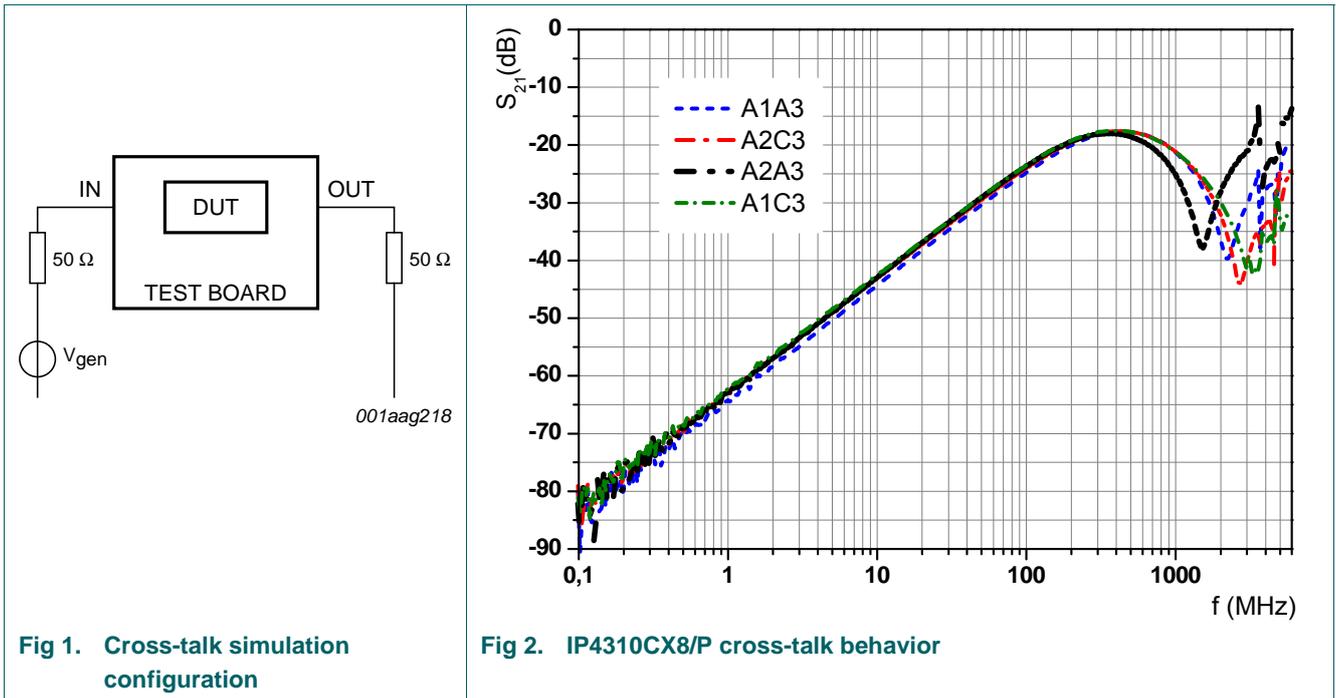


Fig 1. Cross-talk simulation configuration

Fig 2. IP4310CX8/P cross-talk behavior

6. Design/Assembly Recommendations

6.1 PCB Design Guidelines

For the optimum performance, a Non-Solder Mask PCB design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer is recommended. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, the following are the recommended PCB design parameters:

- PCB pad size: 0.20 mm diameter
- Micro-Via diameter: 0.1 mm (0.004")
- Solder Mask opening: 0.37 mm diameter
- Copper thickness: 20-40 μm
- Copper finish: AuNi
- PCB material: FR4

6.2 PCB Assembly Guidelines for Pb-free soldering

The following are recommendations for the assembly of this device:

- Solder Screen Aperture size: 0.33 mm diameter
- Solder Screen thickness: 100 μm (0.004")
- Solder Paste: Pb-free: Sn Ag(3-4) Cu(0.5-0.9)
- Solder/Flux ratio: 50 / 50
- Solder Reflow Profile: see below

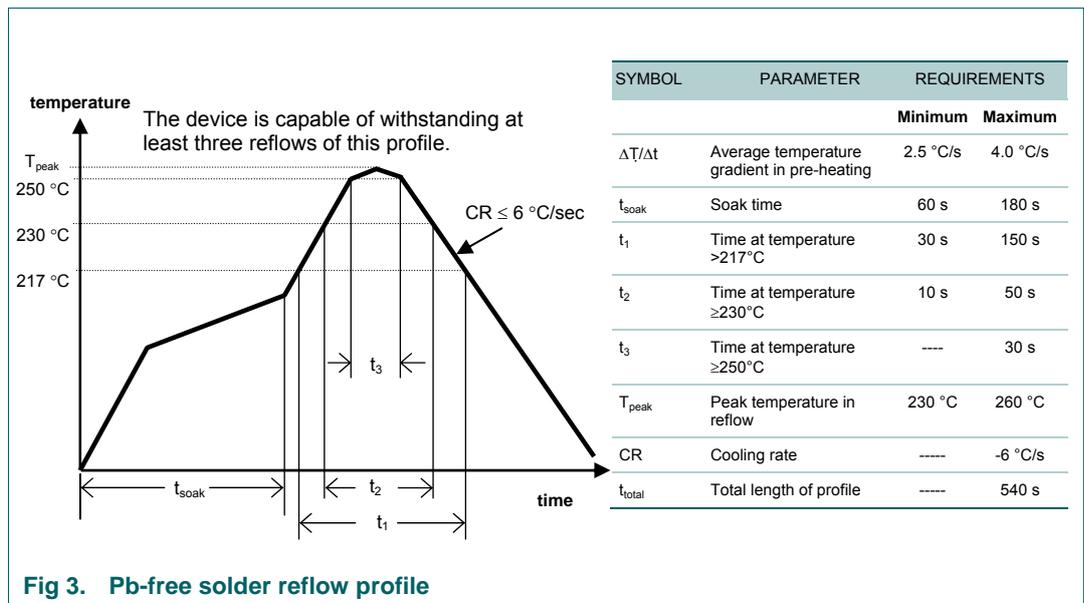
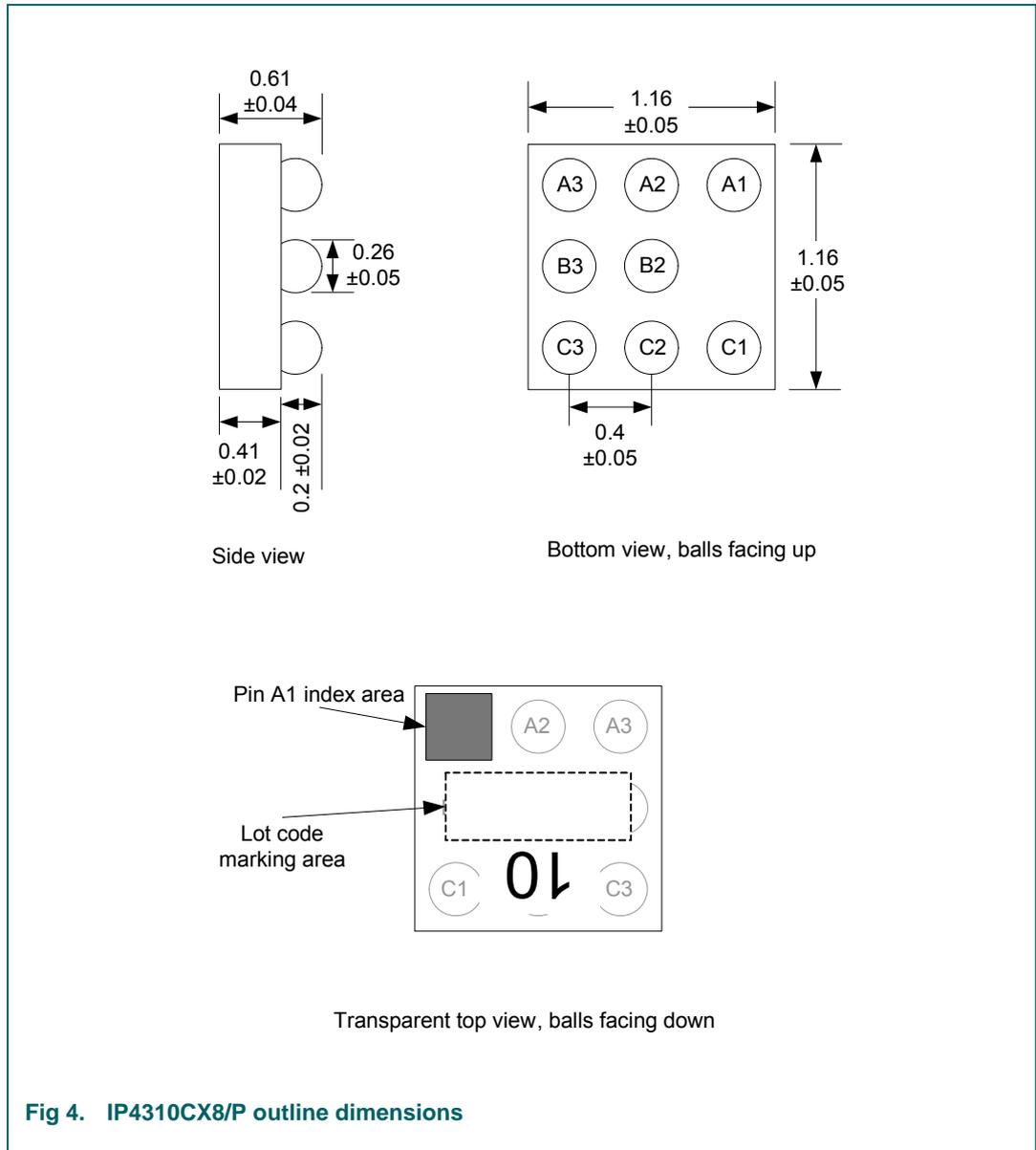


Fig 3. Pb-free solder reflow profile

7. Package outline



8. Tape & Reel information

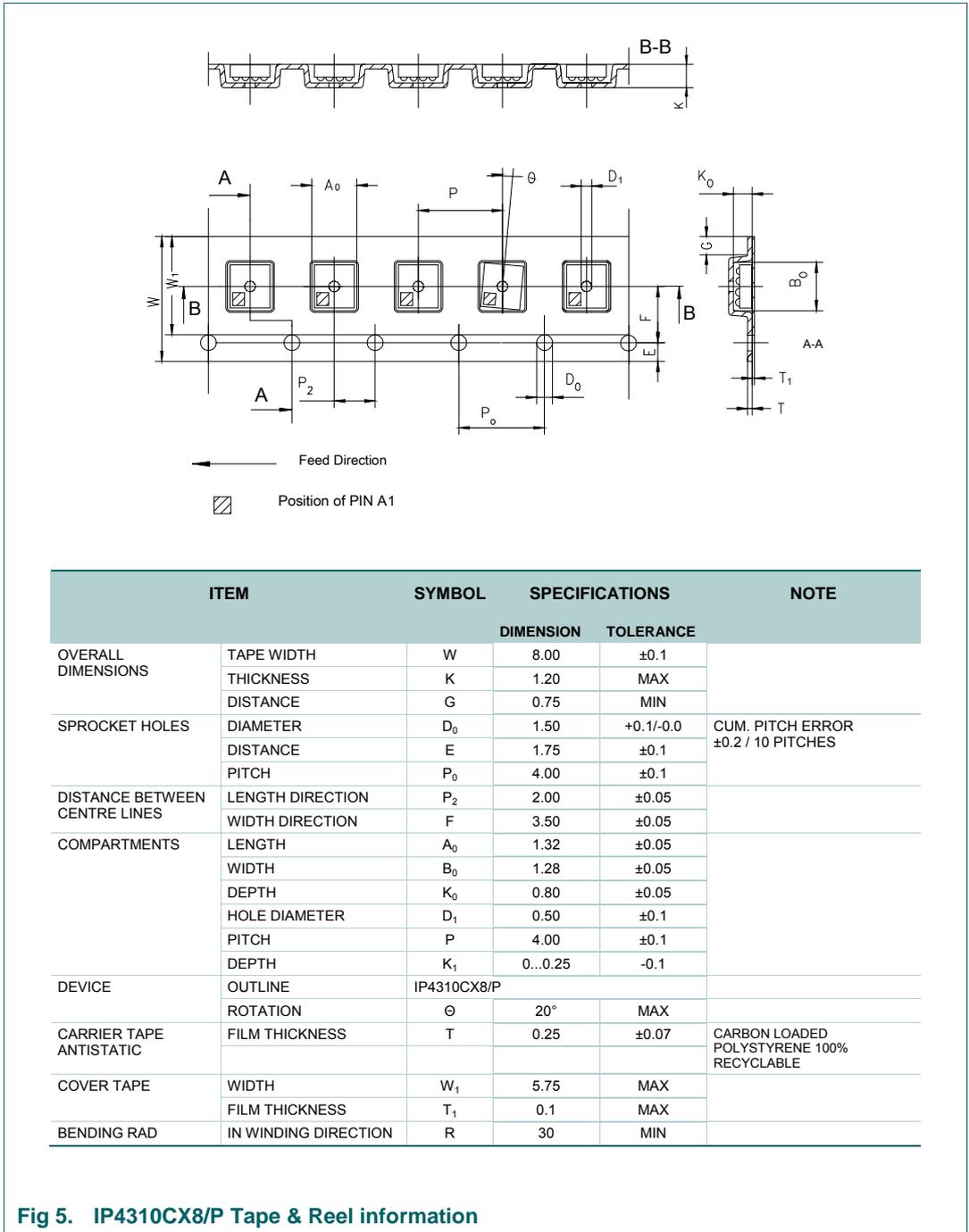


Fig 5. IP4310CX8/P Tape & Reel information

9. Legal information

9.1 Data sheet status

Document status ^{[1],[2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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