Reference Manual

DOC. REV. 12/14/2007

EPM-CPU-10

Pentium III/Celeron processor module with 10/100 Ethernet, Video, and PC/104-Plus interface.

VERSALOGIC CORPORATION

EPM-CPU-10

Pentium III/Celeron processor module with 10/100 Ethernet, Video, and PC/104-*Plus* interface

MEPMCPU10r4

Product Release Notes

This page includes recent changes or improvements that have been made to this product. These changes may affect its operation or physical installation in your application. Please read the following information.

Rev 4 Release

- Rev 4 release.

Rev 3 Release

- Initial public release.

Rev 2 Release

- Beta release only.

Support Page

The **EPM-CPU-10 Support Page**, at **http://www.VersaLogic.com/private/jaguarsupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for EPM-CPU-10 users only. It cannot be reached through our web site. You must enter this address directly to find the support page.

Model EPM-CPU-10

Pentium III/Celeron processor module
with 10/100 Ethernet,
Video, and PC/104-*Plus* interface

REFERENCE MANUAL

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Table of Contents

Introduction 1

Description

The EPM-CPU-10 is a performance-oriented processor board in a compact PC/104-Plus format. It is specifically designed for OEM control projects requiring fast processing, compact size, flexible memory options, high reliability, and long product lifespan / availability. It's features include:

- Socket 370 processors
  - Intel Celeron 350 MHz (equivalent)
  - Intel Celeron 566 MHz
  - Intel Pentium III 850 MHz
- Intel 440BX chipset
- 32 to 256 MB system RAM
- 10 / 100 dual-speed Ethernet
- AGP based video
- Flat panel display support
- 32-pin DiskOnChip support
- PC/104-*Plus* high speed expansion interface
- PCI based IDE controller
- Dual USB 1.1 interfaces
- 2 COM + 1 LPT port
- Keyboard and PS/2 mouse port
- RS-232/422/485 COM port
- CPU temperature sensor
- Watchdog timer
- Vcc sensing reset circuit
- Flash BIOS with OEM enhancements
- Ethernet Remote boot capable
- Single supply (+5V) operation
- Latching I/O connectors
- Customizing available
- Fanless option
- TVS devices
- Customizable setup defaults

The EPM-CPU-10 is a complete computer system in a compact two board set. It may be used alone or with expansion modules. It features a PC/104-*Plus* expansion interface for fast PCI-based interface to a wide variety of PC/104 and PC/104-*Plus* stacking modules.

It is fully compatible with popular operating systems including Windows operating systems, Vx Works, QNX, Linux, and other Real Time Operating Systems.

On-board I/O includes 10/100 Mbit Ethernet, CRT / Flat Panel interface, IDE, USB 1.1, two COM and one LPT port. In addition, one of the COM ports is convertible to RS-232/422/485.

Up to 256 MB of low power system RAM is supported in a high-reliability latching 144-pin SODIMM socket. DiskOnChip Flash space is support for non-volatile program and data file storage without the use of mechanical disk drives.

The high reliability design and construction of this board also features latching I/O connectors, watchdog timer, voltage sensing reset circuit, and self-resetting fuse on the 5V supply to the keyboard, mouse, and USB 1.1 ports. An onboard programmable CPU temperature sensor is included for use in difficult thermal situations. The sensor output can be used to turn on additional fans, create local or remote warnings, or take other action through software triggers.

The EPM-CPU-10 socket 370 compliant 2-board computer will accept Intel Flip-Chip Pentium and Intel Flip-Chip Celeron Chips. Processors speeds up to 850 MHz are available.

This exceptional processor card was designed from the ground up for OEM applications with longevity and reliability as the focus. It is fully supported by the VersaLogic design team. Both hardware and software (BIOS) customization are available. Please contact a VersaLogic Applications Support Specialist to discuss these requirements.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size:
3.95" x 3.775" PCB dimensions 4.23" x 3.775" including connectors. Two board set.

Storage Temperature:
–40° C to 85° C

Free Air Operating Temperature:
0° C to +50° C free air, no airflow (EPM-CPU-10g,h,k)
0° C to +60° C 100 FPM airflow (EPM-CPU-10g,h,k)
-40° C to +75° C free air, no airflow (EPM-CPU-10m)
-40° C to +85° C 100 FPM airflow (EPM-CPU-10m)

Power Requirements: *(with 32 MB SDRAM, keyboard, mouse, running Win95 with Ethernet)*

EPM-CPU-10g	350 MHz equivalent Celeron	5V ±5% @ 3.37 A (16.85 W) typ.
EPM-CPU-10h	566 MHz Celeron	5V ±5% @ 4.47 A (22.35 W) typ
EPM-CPU-10k	850 MHz Pentium III	5V ±5% @ 5.45 A (27.25 W) typ.
EPM-CPU-10m	350 MHz equivalent Celeron	5V ±5% @ 3.52 A (17.60 W) typ.

+3.3V or ±12V may be required by some expansion modules

System Reset:
V_{CC} sensing, resets below 4.75V typ. Watchdog timeout

DRAM Interface:
One 144-pin SODIMM socket, 32 to 256 MB,
SDRAM (EPM-CPU-10k PC-100 compatible or faster, EPM-CPU-10g,h,m runs at PC-66).

Flash Interface:
One 32-pin JEDEC DIP socket.
Accepts one DiskOnChip device . Height limit of 0.330"

Video Interface:
Based on ATi Rage™ XL/Mobility chip. 4 MB VROM standard. Resolutions to 1280 x 1024.
Flat panel display interface, 3.3V and 5V support, TTL and LVDS

IDE Interface:
One PCI-based IDE channel, 40-pin interface, compatible with enhanced IDE mode 4 and Ultra DMA only.
Supports up to two IDE devices (hard drives, CD-ROM, etc.)

Floppy Disk Interface:
Supports two floppy drives

Ethernet Interface:
10/100 Ethernet based on Intel 82551ER chip.

COM1 Interface:
RS-232, 16C550 compatible, 115K baud max.

COM2 Interface:
RS-232/422/485, 16C550 compatible, 460K baud max.

LPT Interface:
Bi-directional/EPP/ECP compatible

Connectors:

I/O:	Two high-density 80-pin (break out to standard .1" IDC and PC connectors).
Video:	10-pin 2mm CRT connector, 44-pin 2mm FPD connector.
Power:	10-pin .1"

BIOS: General Software embedded BIOS with OEM enhancements
Field upgradable with Flash BIOS Upgrade Utility

Bus Speed:

CPU External:	66/100 MHz
PCI, PC/104-*Plus*:	33 MHz
PC/104:	8 MHz

Compatibility:
PC/104-*Plus* Version 1.2 Bus Compatible.
PCI 2.1 compliance, 3.3V or 5V modules.

Specifications are subject to change without notice.

EPM-CPU-10 Block Diagram

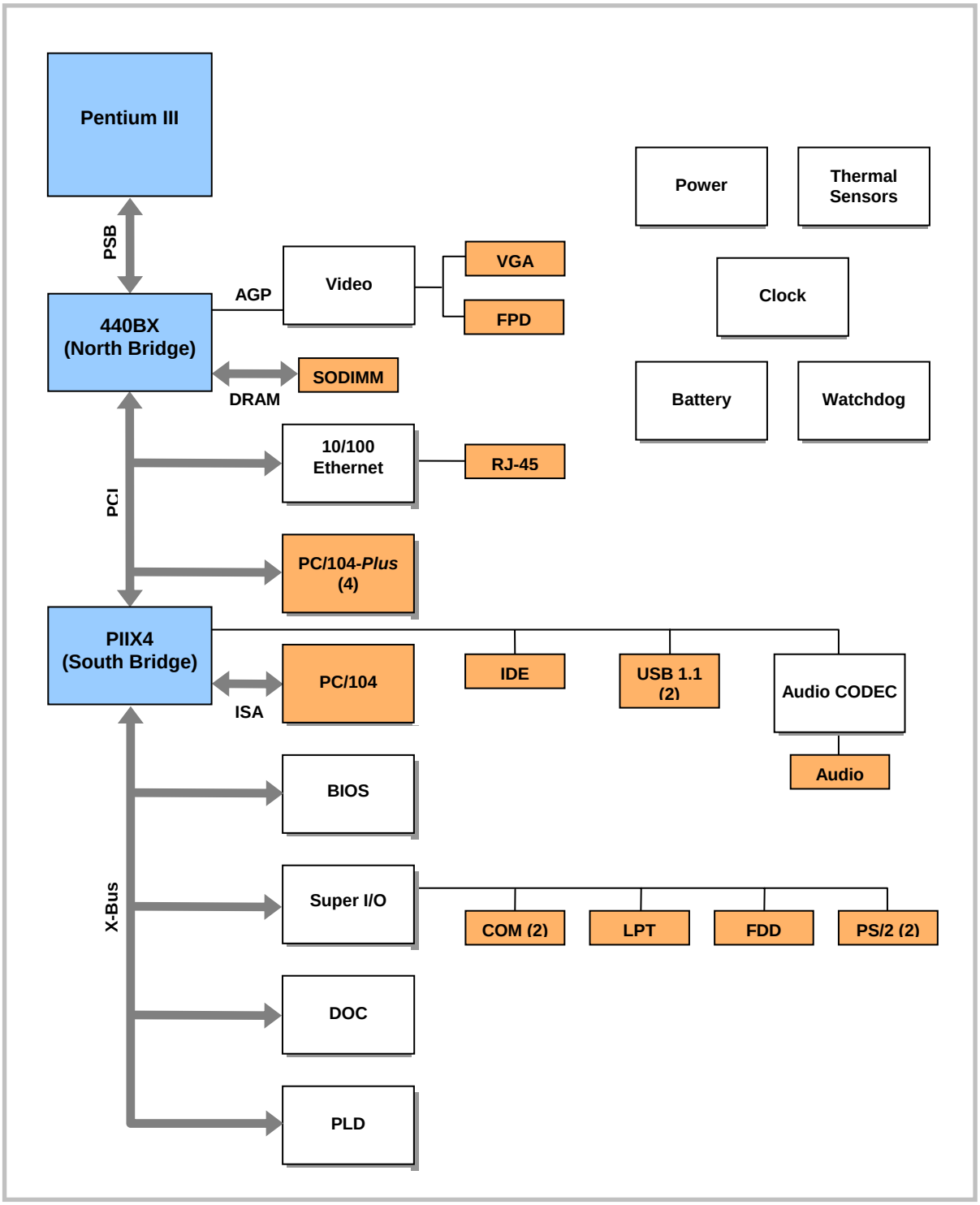


Figure 1. EPM-CPU-10 Block Diagram

Technical Support

If you have problems that this manual can't help you solve, first visit the EPM-CPU-10 Product Support web page at **http://www.VersaLogic.com/private/jaguarsupport.asp**. If you have further questions, contact VersaLogic for technical support at (541) 485-8575. You can also reach our technical support engineers via e-mail at Support@VersaLogic.com.

EPM-CPU-10 Support Website

http://www.VersaLogic.com/private/jaguarsupport.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company, and your phone number
- The name of a technician or engineer who we can contact if we have questions
- Quantity of items being returned
- The model and serial number (bar code) of each item.
- A description of the problem
- Steps you have taken to resolve or repeat the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. We will need to know what shipping method you prefer for return back to your facility, and we will need to secure a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Configuration / Operation 2

Overview

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must be only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an anti-static foam pad if available.

The board should also be protected during shipment or storage by keeping inside a closed metallic anti-static envelope.

Note: The exterior coating on some metallic anti-static bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the EPM-CPU-10.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Initial Configuration and Setup

The following list describes the recommended components and gives an abbreviated outline for setting up a typical development system.

RECOMMENDED COMPONENTS

- EPM-CPU-10 Board Set
- 144-pin SODIMM SDRAM Memory Module (PC-66 or PC-100)
- ATX Power Supply
- SVGA Video Monitor
- Keyboard with PS2 connector
- 3.5" Floppy Disk Drive
- IDE Hard Drive
- IDE CD ROM Drive (optional)

DRAM MODULE

- Insert DRAM module into the SODIMM socket. Latch into place.

CABLES / PERIPHERAL DEVICES

- Plug video adapter cable (p/n CBL-1007) into socket JN2 and attach video monitor.
- Plug keyboard into socket JS4[JC].
- Plug floppy data connector JS3[JK] into floppy drive.

Note: The floppy drive used to boot the system (Drive A) should be connected after the twist in the cable (connector JS3[JK]).

- Plug hard drive data connector JS3[JH] into IDE hard drive.
- Optionally, a CD ROM can be connected to JS3[JJ].
- Plug power supply into JS1.
- Attach power supply cables to external drives.
- Jumper hard drive to operate as a master device.

MEMORY MODULE REQUIREMENTS

- 128MN to 256MB maximum
- 144-pin SODIMM
- PC100 or faster

CMOS Setup / Boot Procedure for EPM-CPU-10

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify correct CMOS Setup information as shown below.
- Insert bootable floppy disk into floppy drive.
- Reset computer using push button reset.
- See KnowledgeBase article VT1485 EPM-CPU-10 CMOS Setup Reference for more information on these options.

Basic CMOS Configuration

```
+--------------------------------------------------------------------------------+
|                  System Bios Setup - Basic CMOS Configuration                  |
|            (C) 2002 General Software, Inc. All rights reserved                 |
+---------------------------+--------------------+-----------------------------+
| DRIVE ASSIGNMENT ORDER:   | Date:>Jan 01, 1980 | Typematic Delay  : 250 ms   |
| Drive A: Floppy 0         | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps   |
| Drive B: (None)           | NumLock:  Disabled | Seek at Boot     : Floppy   |
| Drive C: (None)           +--------------------+ Show "Hit Del"   : Enabled  |
| Drive D: (None)           | BOOT ORDER:        | Config Box       : Enabled  |
| Drive E: (None)           | Boot 1st: Drive A: | F1 Error Wait    : Enabled  |
| Drive F: (None)           | Boot 2nd: (None)   | Parity Checking  : (Unused) |
| Drive G: (None)           | Boot 3rd: (None)   | Memory Test Tick : Enabled  |
| Drive H: (None)           | Boot 4th: (None)   | Debug Breakpoint : (Unused) |
| Drive I: (None)           | Boot 5th: (None)   | Debug Hex Case   : Upper    |
| Drive J: (None)           | Boot 6th: (None)   | Memory Test :StdLo FastHi   |
| Drive K: (None)           +--------------------+-----------------+-----------+
| Boot Method: Boot Sector  | IDE DRIVE GEOMETRY:  Sect  Hds  Cyls | Memory    |
+---------------------------+ Ide 0: Not installed                 |  Base:    |
| FLOPPY DRIVE TYPES:       | Ide 1: Not installed                 |   633KB   |
| Floppy 0: 1.44 MB, 3.5"   | Ide 2: Unused                        |  Ext:     |
| Floppy 1: Not installed   | Ide 3: Unused                        |   127MB   |
+---------------------------+--------------------------------------+-----------+
```

Custom Configuration

```
+--------------------------------------------------------------------------------+
|                  System BIOS Setup - Advanced Configuration                    |
|            (C) 2002 General Software, Inc. All rights reserved                 |
+-------------------------------------+------------------------------------------+
| BIOS Extension            : Disabled  | COM1 (03F8) Enabled/IRQ   : IRQ4      |
| DiskOnChip                : Disabled  | COM2 (02F8) Enabled/IRQ   : IRQ3      |
| Parallel Port Mode        : SPP       | LPT1 (0378) Enabled/IRQ   : IRQ7      |
| Display Type              : CRT       | PS/2 Mouse Enabled/IRQ    : IRQ12     |
| I/O Register Base Address : 0E0h      | PCI Int A                 : IRQ11     |
| CPU Temperture Threshold  : 70°C      | PCI Int B                 : IRQ11     |
| Splash Screen             : Disabled  | PCI Int C                 : IRQ11     |
| Processor Throttling      : Varies    | PCI Int D                 : IRQ11     |
| Throttling Percentage     : Varies    | Reserved                  : (Unused)  |
+-------------------------------------+------------------------------------------+
```

Shadow Configuration

```
+--------------------------------------------------------------------------------+
|                  System BIOS Setup - Shadow/Cache Configuration                |
|            (C) 2002 General Software, Inc. All rights reserved                 |
+-------------------------------------+------------------------------------------+
| Shadowing                 : Chipset   | Shadow 16KB ROM at C000   : Enabled   |
| Shadow 16KB ROM at C400   : Enabled   | Shadow 16KB ROM at C800   : Disabled  |
| Shadow 16KB ROM at CC00   : Disabled  | Shadow 16KB ROM at D000   : Disabled  |
| Shadow 16KB ROM at D400   : Disabled  | Shadow 16KB ROM at D800   : Disabled  |
| Shadow 16KB ROM at DC00   : Disabled  | Shadow 16KB ROM at E000   : Disabled  |
| Shadow 16KB ROM at E400   : Disabled  | Shadow 16KB ROM at E800   : Disabled  |
| Shadow 16KB ROM at EC00   : Disabled  | Shadow 64KB ROM at F000   : Enabled   |
+-------------------------------------+------------------------------------------+
```

Note: Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above. Above screen version is Version 5.1.105

Creating a Bootable DOS DiskOnChip

The DiskOnChip is shipped pre-formatted, non-bootable, without any files on it. The DiskOnChip will appear as Drive D in systems with an installed hard drive. If a hard drive is not installed, the DOC will appear as Drive C:

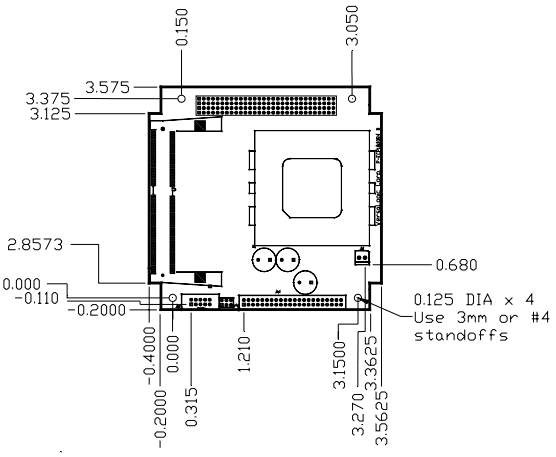
1. Boot your system under DOS or Windows (if using Windows, start a DOS session)
2. Type SYS C: (or SYS D: if appropriate)

Operating System Installation

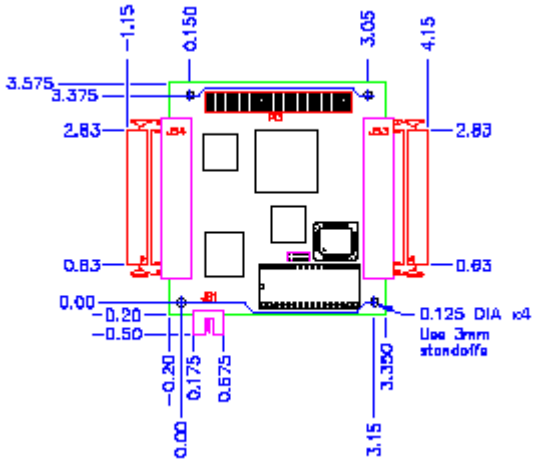
The standard PC architecture used on the EPM-CPU-10 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPM-5 Product Support web page at **http://www.VersaLogic.com/private/jaguarsupport.asp**.

Physical Dimensions

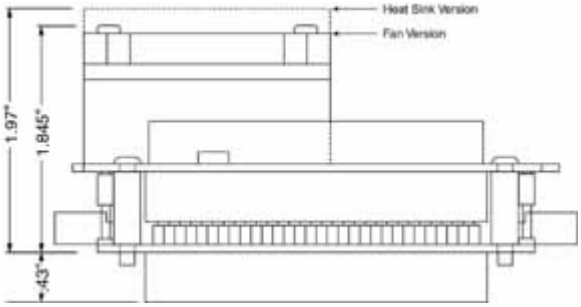
The EPM-CPU-10 is a two board set consisting of a CPU Module (North Bridge) and an I/O Module (South Bridge). Dimensions are given below to help with pre-production planning and layout.



CPU Module (North Bridge)



I/O Module (South Bridge)



Overall Height (Fan & Fanless Model)

Figure 2. Dimensions

(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The EPM-CPU-10 consists of two boards which are mounted together with eight 5mm x 15mm M3 threaded hex male/female standoffs (p/n VL-HDW-101) using the corner mounting holes. These standoffs are secured to the top circuit board using four pan head screws.

Caution Extreme care must be taken not to damage components near the corner mounting holes when tightening standoffs with nut driver tools.

Additional PC/104-*Plus* or PC/104 cards can be attached to the bottom of the EPM-CPU-10 board set and secured with standoffs or 5mm nuts.

PC/104-*Plus* expansion modules can be secured directly to the underside of the EPM-CPU-10.

PC/104 expansion modules can be secured to the underside of the EPM-CPU-10, however, the 40-pin and 64-pin ISA feedthrough connectors may need to be extended, and longer standoffs might need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 module.

The entire assembly can sit on a table top or it can be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Refer to the drawing on page 11 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the modules from the stack.

STACK ARRANGEMENT

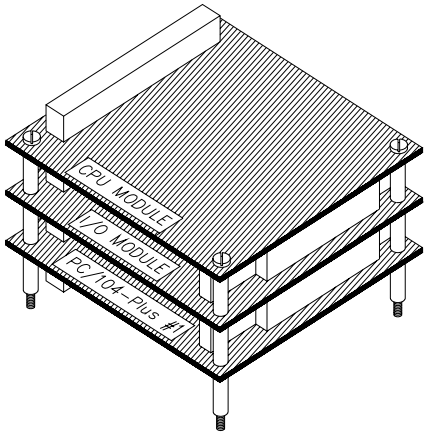


Figure 3. PC/104-*Plus* Card Added to Bottom of Stack

External Connectors

CONNECTOR LOCATION DIAGRAMS

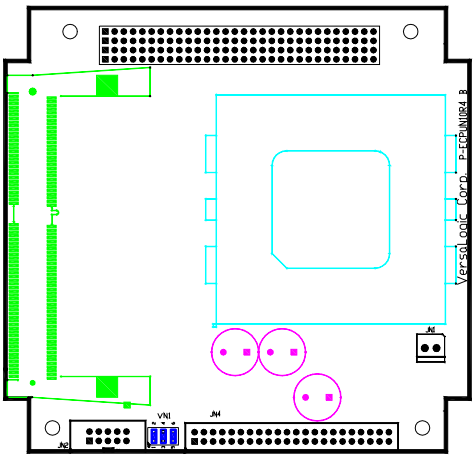


Figure 4. Connector Location Diagram (CPU Module)

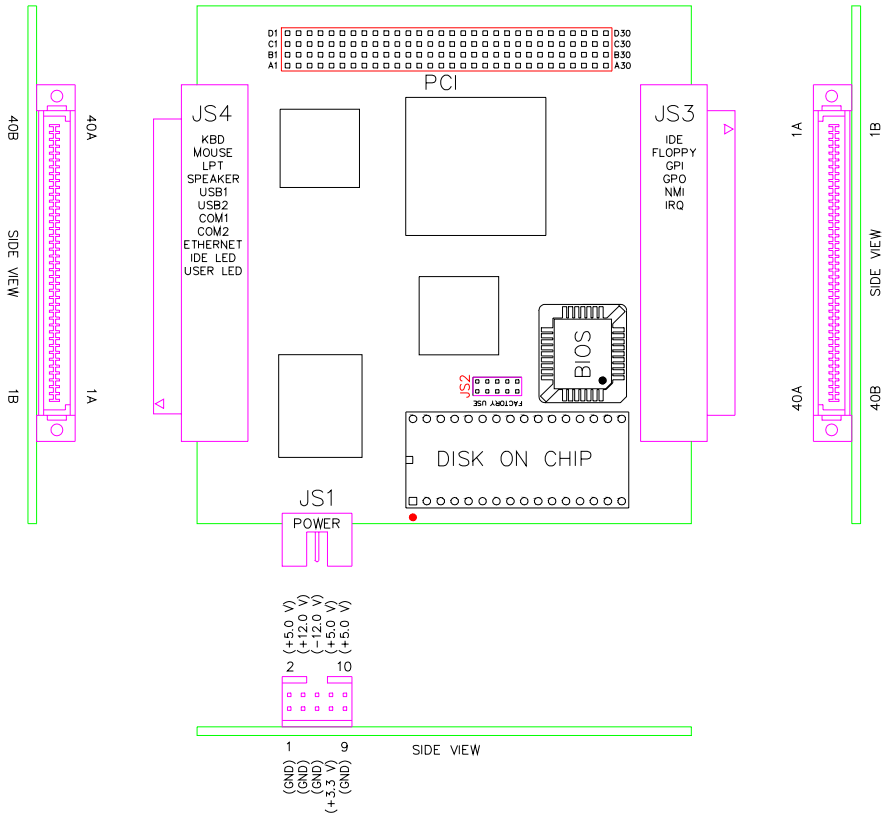


Figure 5. Connector Location Diagram (I/O Module)

CONNECTOR FUNCTIONS AND INTERFACE CABLES

The table below notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page
JN1	Fan Power Output (+5V)	Molex 22-01-3027 or Molex 22-01-2025	Provided with fan assembly	—	22
JN2	SVGA Video Output	SAMTEC TCSD-05-S-12.00-01-F-N	CBL-1007	1 foot 10-pin socket to 15-pin D-sub SVGA connector	33
JN4*	Flat Panel Interface	FCI 90311-044(Housing) + FCI 77138(Crimp Pins)	—	Contact Factory	34
JS1	Main Power Input	Berg 69176-010 (Housing) + Berg 47715-000 (Pins)	CBR-1008	Interface from industry standard ATX power supply	20
JS2	PLD Reprogramming Port *(Factory use Only)*	—	—	—	—
JS3	IDE0, Floppy, General Purpose Input, General Purpose Output, NMI	Robinson-Nugent P50E-080S-TG	CBL-8002	Breakout to standard PC device connectors	16
JS4	Keyboard, Mouse, LPT1, Speaker, USB1, USB2, COM1, COM2, Ethernet, IDE Data LED, Programmable LED	Robinson-Nugent P50E-080S-TG	CBL-8001	Breakout to standard PC device connectors	15

* **Note:** This connector is a 2.00mm housing and crimp terminal, discrete wire style. Number of crimp terminals depends upon flat panel display model being used.

HIGH DENSITY 80-PIN CABLE (JS4)

Cable assembly CBL-8001 is used to break-out this high density connector into standard PC I/O connectors. This chart shows the pinout for the cable assembly.

Table 2: JS4 High Density 80-Pin Connector Pinout

JS4 Pin	External Connector	Pin	Signal
1A	**LPT1**	1	Strobe
2A	JA	14	Auto feed
3A		2	Data bit 1
4A		15	Printer error
5A		3	Data bit 2
6A		16	Reset
7A		4	Data bit 3
8A		17	Select input
9A		5	Data bit 4
10A		18	Ground
11A		6	Data bit 5
12A		19	Ground
13A		7	Data bit 6
14A		20	Ground
15A		8	Data bit 7
16A		21	Ground
17A		9	Data bit 8
18A		22	Ground
19A		10	Acknowledge
20A		23	Ground
21A		11	Port Busy
22A		24	Ground
23A		12	Paper End
24A		25	Ground
25A		13	Select
26A	**MISC**	—	No Connect
27A		—	Programmable LED+
28A		—	Programmable LED–
29A		—	Speaker +
30A		—	Speaker –
31A		—	IDE Data LED–
32A		—	IDE Data LED+
33A	**MOUSE**	4	+5V (Protected)
34A	JB	1	Mouse Data
35A		3	Ground
36A		5	Mouse Clock
37A	**KBD**	4	+5V (Protected)
38A	JC	1	Keyboard Data
39A		3	Ground
40A		5	Keyboard Clock

JS4 Pin	External Connector	Pin	Signal
1B	**USB**	1	+5V (Protected)
2B	JD	6	Ground
3B		2	Channel 0 Data –
4B		7	Cable Shield
5B		3	Channel 0 Data +
6B		8	Channel 1 Data +
7B		4	Cable Shield
8B		9	Channel 1 Data –
9B		5	Ground
10B		10	+5V (Protected)
11B	**ETHERNET**	4	Isolated Ground
12B	JE	5	Isolated Ground
13B		6	Receive Data –
14B		3	Receive Data +
15B		7	Isolated Ground
16B		8	Isolated Ground
17B		2	Transmit Data –
18B		1	Transmit Data +
19B	**PBRESET**	—	Pushbutton Reset
20B		—	Ground
21B	**COM1**	1	Data Carrier Detect
22B	JF	6	Data Set Ready
23B		2	Receive Data
24B		7	Request to Send
25B		3	Transmit Data
26B		8	Clear to Send
27B		4	Data Terminal Ready
28B		9	Ring Indicator
29B		5	Ground
30B		—	No Connect
31B	**COM2**	1	Data Carrier Detect
32B	JG	6	Data Set Ready
33B		2	Receive Data
34B		7	Request to Send
35B		3	Transmit Data
36B		8	Clear to Send
37B		4	Data Terminal Ready
38B		9	Ring Indicator
39B		5	Ground
40B		—	No Connect

HIGH DENSITY 80-PIN CABLE (JS3)

Cable assembly CBL-8002 is used to break-out this high density connector into standard PC I/O connectors. This chart shows the pinout for the cable assembly.

Table 3: JS3 High Density 80-Pin Connector Pinout

JS3 Pin	External Connector	Pin	Signal
1A	**IDE CH0**	1	Reset
2A	JH/JJ	2	Ground
3A		3	Data bit 7
4A		4	Data bit 8
5A		5	Data bit 6
6A		6	Data bit 9
7A		7	Data bit 5
8A		8	Data bit 10
9A		9	Data bit 4
10A		10	Data bit 11
11A		11	Data bit 3
12A		12	Data bit 12
13A		13	Data bit 2
14A		14	Data bit 13
15A		15	Data bit 1
16A		16	Data bit 14
17A		17	Data bit 0
18A		18	Data bit 15
19A		19	Ground
20A		20	No connection
21A		21	No connection
22A		22	Ground
23A		23	I/O write
24A		24	Ground
25A		25	I/O read
26A		26	Ground
27A		27	I/O Channel Ready
28A		28	No connection
29A		29	No connection
30A		30	Ground
31A		31	IRQ14
32A		32	Drive 16-bit I/O
33A		33	Address bit 1
34A		34	No connection
35A		35	Address bit 0
36A		36	Address bit 2
37A		37	Chip select 0
38A		38	Chip select 1
39A		39	Light Emitting Diode –
40A		40	Ground

JS3 Pin	External Connector	Pin	Signal
1B	**FLOPPY**	1	Ground
2B	JK/JL	2	Load Head
3B		3	Ground
4B		4	No Connection
5B		5	Ground
6B		6	No Connection
7B		7	Ground
8B		8	Beginning Of Track
9B		9	Ground
10B		10	Motor Enable 1
11B		11	Ground
12B		12	Drive Select 0
13B		13	Ground
14B		14	Drive Select 1
15B		15	Ground
16B		16	Motor Enable 0
17B		17	Ground
18B		18	Direction Select
19B		19	Ground
20B		20	Motor Step
21B		21	Ground
22B		22	Write Data Strobe
23B		23	Ground
24B		24	Write Enable
25B		25	Ground
26B		26	Track 0 Indicator
27B		27	Ground
28B		28	Write Protect
29B		29	Ground
30B		30	Read Data
31B		31	Ground
32B		32	Head Select
33B		33	Ground
34B		34	Drive Door Open
35B	**MISC**	1	Ground
36B	JM	2	+5V (Protected)
37B		3	General Purpose Output
38B		4	General Purpose Input
39B		5	Non Maskable Interrupt
40B		6	No connection

Jumper Block Locations

Note: Jumpers shown in as-shipped configuration.

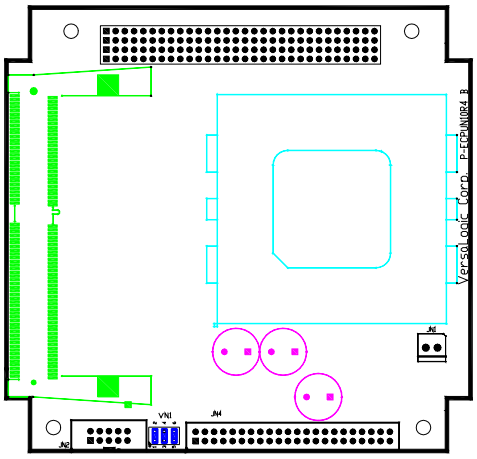


Figure 6. Jumper Block Locations (CPU Module)

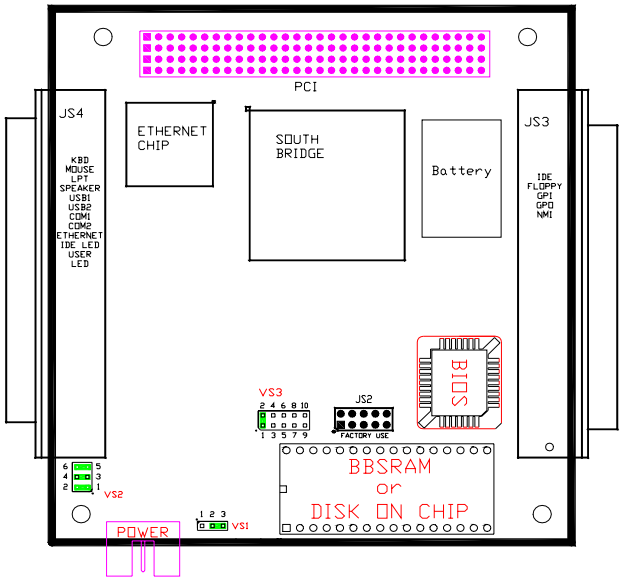


Figure 7. Jumper Block Locations (I/O Module)

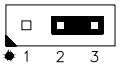
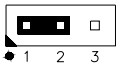
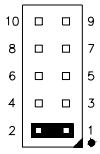
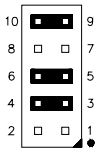
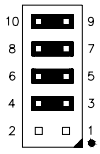
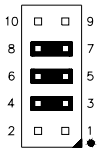
JUMPER SUMMARY

Table 4: Jumper Summary North Board

Jumper Block	Description	As Shipped	Page
VN1	**Video Output Type** **Primary Video BIOS** **VN1[5-6] VN1[3-4] VN1[1-2] Type** In In In CRT only, flat panel display disabled In In Out 640x480 TFT Color In Out In 800x600 TFT Color **Secondary Video BIOS** **VN1[5-6] VN1[3-4] VN1[1-2] Type** In In In CRT only, flat panel display disabled In In Out 800x600 LVDS 18-bit Color* In Out In 1024x768 LVDS 18-bit Color* **Note:** *See VS2[3-4] Video BIOS selector for information on video BIOS selection. The flat panel displays listed for the secondary video BIOS are supported by the default secondary video BIOS. Other flat panel displays are supported by updating the secondary video BIOS. Contact factory for more information.*	—	—

JUMPER SUMMARY

Table 5: Jumper Summary South Board

Jumper Block	Description	As Shipped	Page
VS1	**CMOS RAM and Real Time Clock Erase** Normal Operation  Erase  ***Note:*** *Do not operate the board with the jumper in the erase position. Leave the jumper in position VS1[1-2] for at least 30 seconds to fully erase CMOS RAM.*	Normal	24
VS2[1-2]	**System BIOS Selector** In — Primary System BIOS Out — Secondary System BIOS ***Note:*** *The secondary System BIOS is field upgradable using the BIOS upgrade utility. See www.VersaLogic.com/private/jaguarsupport.asp for further information.*	In	—
VS2[3-4]	**Video BIOS Selector** In — Primary Video BIOS Out — Secondary Video BIOS ***Note:*** *The secondary System BIOS is field upgradable using the BIOS upgrade utility. See www.VersaLogic.com/private/jaguarsupport.asp for further information.*	In	—
VS2[5-6]	**General Purpose Jumper** In — Bit D1 in SCR register 00E2h reads as 1 Out — Bit D1 in SCR register 00E2h reads as 0	In	46
VS3	**COM2 Configuration** RS-232  RS-422  RS-485 Endpoint Station  RS-485 Intermediate Station  	RS-232	27

Power Supply

POWER CONNECTORS

Main power is applied to the *EPM-CPU-10* through a 10-pin polarized connector. Mating connector Berg 69176-010 (Housing) + Berg 47715-000 (Pins).

See page 13 for connector pinout and location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors be wired correctly. Make sure to use all three +5VDC pins and all four ground pins to prevent excess voltage drop.

Table 6: Main Power Connector Pinout

JS1 Pin	Signal Name	Description
1	Ground	Ground
2	+5VDC	Power Input
3	Ground	Ground
4	+12VDC	Power Input
5	Ground	Ground
6	–12VDC	Power Input
7	+3.3VDC	Power Input
8	+5VDC	Power Input
9	Ground	Ground
10	+5VDC	Power Input

Note: The +3.3VDC, +12VDC, and –12VDC inputs are only required for expansion modules that require these voltages.

POWER REQUIREMENTS

The *EPM-CPU-10* only requires +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with an on-board DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the *EPM-CPU-10* depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules, and attached devices. For example, PS/2 keyboards typically draw their power directly from the *EPM-CPU-10*, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the unit on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number T-HB3/5). Life expectancy under normal use is approximately 10 years.

CPU

PROCESSOR REPLACEMENT

Remove or replacement of CPU is not recommended, doing so may damage the CPU. These flip-chip style 370-pin CPU's have the chip dies mounted an a thin substrate. If the substrate is flexed too far, damage will occur to the die bonds. Such damage will not be covered under the board warranty.

PROCESSOR SIDE BUS SELECTION

Pentium and Celeron CPU's normally select their Processor Side Bus Speed.

HEAT SINK

A heat sink and cooling fan must be in place whenever power is applied to the CPU. The fan connects to header JN1 for power.

Table 7: Fan Power Connector

JN1 Pin	Signal Name	Function
1	+5V	Fan Power
2	GND	Ground

Note: A fan is not required for the low-power CELERON 350 MHZ model (g version).

PROCESSOR POWER MANAGEMENT

A form of power management called "throttling" is supported on the EPM-CPU-10. This is an Intel 440BX chipset feature that has been augmented with an I/O control bit in the VersaLogic Special Control Register. CMOS Setup options have been implemented to select throttling percentages from 12.5% to 75%, and to enable or disable throttling. Throttling works by activating the CPU Stop-Clock line every 250 microseconds to create a duty-cycle relative to the selected throttling percentage. These throttling percentages refer to the relative time the CPU is in a stopped mode.

If throttling is enabled with the percentage set to 75%, the CPU will run at full speed (566 MHz for the EPM-CPU-10g, EPM-CPU-10h or EPM-CPU-10m and 850MHz for the EPM-CPU-10k) for 62.5 microseconds (25%) and will be off for 187.5 microseconds (75%) every 250 microsecond period.

Once the throttling percentage is initialized in the CMOS Setup, it can be enabled and disabled by writing to the “Throttle” control bit in the VersaLogic Special Control Register. See page 44. This gives the user a very simple means to throttle back during a time of little activity, and to re-establish full power when needed.

The EPM-CPU-10g Low Power Fanless and the EPM-CPU-10m versions are 566 MHz Celerons with throttling always enabled at a minimum of 37.5% (which gives an effective CPU speed of 350 MHz). It can be slowed down to the maximum throttling rate of 75%, but not less than 37.5%. The Throttle control bit in the VersaLogic Special Control Register can not be changed on the EPM-CPU-10g and EPM-CPU-10m. Contact the factory for information on how to change the throttling percentage via indexed PCI based registers in the chipset.

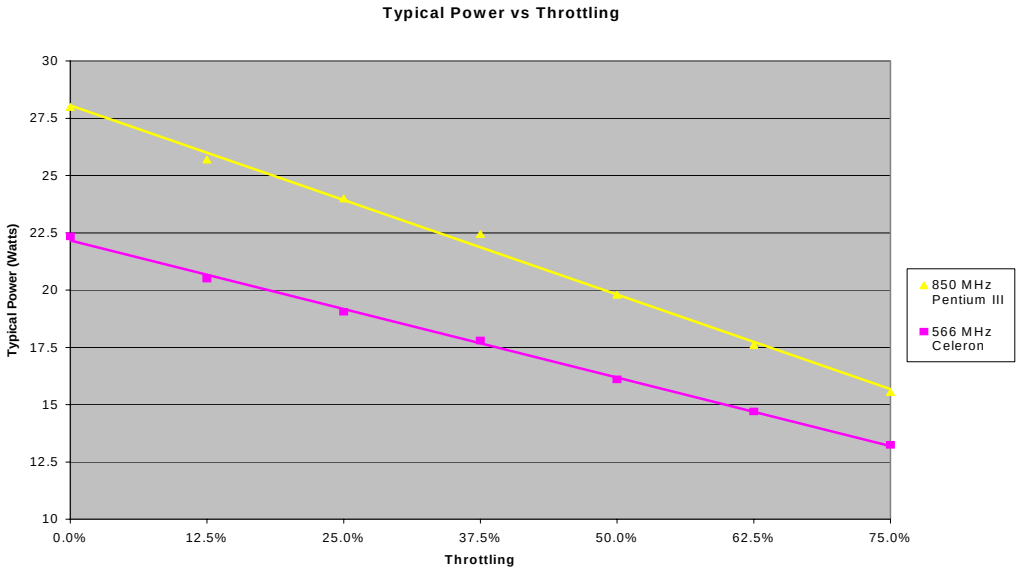


Figure 8

System RAM

COMPATIBLE MEMORY MODULES

The EPM-CPU-10 will accept one 144-pin SODIMM memory module with the following characteristics:

- Storage Capacity 32 to 256 MB
- Voltage 3.3 Volt
- Error Detection Not supported
- Error Correction Not supported
- Type EPM-CPU -10k SDRAM PC-100 or faster
  EPM-CPU-10g,h,m SDRAM PC-66 or faster

The following are qualified memory modules for the EPM-CPU-10. These modules are sold by VersaLogic under part number VL-MM4S-256.

- Crucial CT32M64S4W8E
- Micron MT16LSDF3264HG-10Ex2
- Micron MT16LSDF3264HG-10Ex4

CMOS RAM

CLEARING CMOS RAM

Jumper VS1 can be moved to position [1-2] for 30 seconds to erase the contents of the CMOS RAM. Be sure to move the jumper back to position [2-3] for normal operation.

Note: Operation with the jumper in the erase position [1-2] will cut-off all battery power to the CMOS RAM and Real Time Clock chip. The board will operate in this condition, however, this will force the board to use the factory default parameters as shown on page 9. For custom programming of the Factory Default Parameters, please contact the Customization Department at VersaLogic.

CMOS Setup Defaults

The EPM-CPU-10 features the ability for users to modify the CMOS Setup defaults. This allows the system to boot up with user defined settings from cleared or corrupted CMOS RAM, battery failure, or battery-less operation. All CMOS setup defaults can be changed except the time and date.

Warning - If the CMOS Setup defaults are set in a way that makes the system unbootable and unable for the user to enter CMOS Setup, the EPM-CPU-10 will need to be serviced by the factory.

Real Time Clock

The *EPM-CPU-10* features a year 2000 compliant, battery-backed 146818 compatible real time clock/calendar chip. Under normal battery conditions, the clock will maintain accurate timekeeping functions during periods when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real time clock.

DiskOnChip

A 32-pin socket (U1 on the I/O module) will accept an M-Systems DiskOnChip (DOC) Flash Disk for non-volatile, read/write data storage. The DOC can be configured as a boot device

ENABLE / DISABLE

The DOC can be enabled or disabled through CMOS Setup by going into the Advanced Configuration screen and setting "DiskOnChip" to one of the three base addresses or "Disabled". When enabled, the DOC will take up 8KB at the base address specified.

COMPATIBLE DEVICES

Any 5 Volt, low profile M-Systems series DOC device will work.

INSTALLING THE DOC CHIP

1. Align pin 1 on the DOC with pin 1 of socket U1 on the I/O module.
2. Push the DOC into the socket carefully until it is fully seated.

Warning! ***The DOC will be permanently damaged if installed incorrectly!*** When installing the DOC, be sure to align pin-1 on the chip with pin-1 on the socket. To prevent electrostatic damage, first touch a grounded surface to discharge any static electricity from your body.

CMOS SETUP

To enable the DOC as drive C on a system without a hard disk, set the CMOS setup of drive C to "not installed", and reboot the computer.

Note: The DOC needs to be formatted with the System files in order for it to be a bootable drive. Refer to the M-Systems web site (www.m-sys.com) for documentation on the DOC 2000 and details on making it a bootable device.

Serial Ports

The *EPM-CPU-10* features two on-board 16550 based serial channels located at standard PC I/O addresses. COM1 is an RS-232 (115.2K baud) serial port.

COM2 can be operated in RS-232, RS-422, or RS-485 modes. Two additional non-standard baud rates are also available (programmable in the normal baud rate registers) of 230K and 460K baud.

Interrupt assignment for each COM port is handled in CMOS Setup, and each port can be independently enabled or disabled.

COM Port Configuration

There are no configuration jumpers for COM1 because it only operates in RS-232 mode.

Jumper VS3 is used to configure COM2 for RS-232/422/485 operation. See page 18 and 19 for jumper configuration details.

COM2 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the DTR handshaking line.

The following code example shows how to turn the line driver for COM2 on and off:

```
mov   dx,02FCh   ; Point to COM2 Modem Control register
in    al,dx      ; Fetch existing value
or    al,01h     ; Set bit D0
out   dx,al      ; Turn DTR on (enables line driver)

in    al,dx      ; Fetch existing value
and   al,0FEh    ; Clear bit D0
out   dx,al      ; Turn DTR off (disables line driver)
```

SERIAL PORT CONNECTORS

See the *Connector Location Diagram* on pages 13 and 14 for connector and cable information. The pinout of the DB9 connector applies to use of the VersaLogic transition cable CBL-8001.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Table 8: Connectors JF / JG — Serial Port Pinout

COM1 JS4 Pin	COM2 JS4 Pin	RS-232	RS-422	RS-485	JF/JG DB9 Pin
21B	31B	DCD	—	—	1
22B	32B	DSR	—	—	6
23B	33B	RXD*	TxD+	TxD+	2
24B	34B	RTS	TxD–	TxD–	7
25B	35B	TXD*	—	—	3
26B	36B	CTS	Ground	Ground	8
27B	37B	DTR	RxD–	TxD/RxD–	4
28B	38B	RI	RxD+	TxD/RxD+	9
29B	39B	Ground	Ground	Ground	5
30B	40B	N/C	—	—	—

Parallel Port

The *EPM-CPU-10* includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled/disabled and interrupt assignments can be made via the CMOS Setup screen. The pinout of the JA connector applies to use of the VersaLogic transition cable CBL-8001.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Table 9: LPT1 Parallel Port Pinout

JS4 Pin	Centronics Signal	Signal Direction	JA Pin
1A	Strobe	Out	1
2A	Auto feed	Out	14
3A	Data bit 1	In/Out	2
4A	Printer error	In	15
5A	Data bit 2	In/Out	3
6A	Reset	Out	16
7A	Data bit 3	In/Out	4
8A	Select input	Out	17
9A	Data bit 4	In/Out	5
10A	Ground	—	18
11A	Data bit 5	In/Out	6
12A	Ground	—	19
13A	Data bit 6	In/Out	7
14A	Ground	—	20
15A	Data bit 7	In/Out	8
16A	Ground	—	21
17A	Data bit 8	In/Out	9
18A	Ground	—	22
19A	Acknowledge	In	10
20A	Ground	—	23
21A	Port Busy	In	11
22A	Ground	—	24
23A	Paper End	In	12
24A	Ground	—	25
25A	Select	In	13

IDE Hard Drive / CD-ROM Interfaces

One IDE interface is available to connect up to two hard disk or CD-ROM drives. Use CMOS Setup to specify the drive parameters of the attached drives.

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 10: EIDE Hard Drive Connector Pinout

JS3 Pin	Signal Name	EIDE Signal Name	Function	JH/JJ Pin
1A	HRST*	Host Reset	Reset signal from CPU	1
2A	Ground	Ground	Ground	2
3A	IDE7	DATA 7	Data bit 7	3
4A	HD8	DATA 8	Data bit 8	4
5A	HD6	DATA 6	Data bit 6	5
6A	HD9	DATA 9	Data bit 9	6
7A	HD5	DATA 5	Data bit 5	7
8A	HD10	DATA 10	Data bit 10	8
9A	HD4	DATA 4	Data bit 4	9
10A	HD11	DATA 11	Data bit 11	10
11A	HD3	DATA 3	Data bit 3	11
12A	HD12	DATA 12	Data bit 12	12
13A	HD2	DATA 2	Data bit 2	13
14A	HD13	DATA 13	Data bit 13	14
15A	HD1	DATA 1	Data bit 1	15
16A	HD14	DATA 14	Data bit 14	16
17A	HD0	DATA 0	Data bit 0	17
18A	HD15	DATA 15	Data bit 15	18
19A	Ground	Ground	Ground	19
20A	NC	NC	No connection	20
21A	NC	NC	No connection	21
22A	Ground	Ground	Ground	22
23A	HWR*	HOST IOW*	I/O write	23
24A	Ground	Ground	Ground	24
25A	HRD*	HOST IOR*	I/O read	25
26A	Ground	Ground	Ground	26
27A	NC	NC	No connection	27
28A	HAEN	ALE	Address latch enable	28
29A	NC	NC	No connection	29
30A	Ground	Ground	Ground	30
31A	HINT	HOST IRQ14	IRQ14	31
32A	XI16*	HOST IOCS16*	Drive register enabled	32
33A	HA1	HOST ADDR1	Address bit 1	33
34A	NC	NC	No connection	34
35A	HA0	HOST ADDR0	Address bit 0	35
36A	HA2	HOST ADDR2	Address bit 2	36
37A	HCS0*	HOST CS0*	Reg. access chip select 0	37
38A	HCS1*	HOST CS1*	Reg. access chip select 1	38
39A	NC	NC	No connection	39
40A	Ground	Ground	Ground	40

Utility Connector

KEYBOARD/MOUSE INTERFACE

A standard PS/2 keyboard and mouse interface is accessible through connector JS4. In addition, you will find a programmable LED output, hard drive activity LED, and a speaker output as shown in the table below. The pinout of the PS/2 connectors applies to use of the VersaLogic transition cable CBL-8001.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Table 11: Utility Connector

JS4 Pin	Description	PS/2 Pin	
27A	Programmable LED +		
28A	Programmable LED –		
29A	Speaker +		
30A	Speaker –		
31A	IDE Drive Indicator LED –		
32A	IDE Drive Indicator LED +		
33A	Protected +5V	4	(JB) Mouse Connector
34A	Mouse Data	1	
35A	Ground	3	
36A	Mouse Clock	5	
37A	Protected +5V	4	(JC) Keyboard Connector
38A	Keyboard Data	1	
39A	Ground	3	
40A	Keyboard Clock	5	

PROGRAMMABLE LED

The high-density I/O connector JS4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to JS4[28A]; anode to JS4[27A]. An on-board resistor limits the current to 15 mA when the circuit is turned on.

To turn the LED on and off, set or clear bit D7 in I/O port 0E0h (or 1E0h if selected in CMOS Setup). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn on and off the LED. Refer to page 44 for further information:

LED On

```
in    al,E0h
or    al,80h
out   E0h,al
```

LED Off

```
in    al,E0h
and   al,7Fh
out   E0,al
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

EXTERNAL SPEAKER

A miniature 8 ohm speaker can be connected between JS4[29A] and JS4[30A].

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Push-Button Reset

A normally open, momentary action push-button reset switch can be connected between JS4[19B] and JS4[20B]. Shorting JS4[19B] to ground will cause the *EPM-CPU-10* to reboot.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Floppy Drive Interface

The *EPM-CPU-10* supports a standard 34-pin PC/AT style floppy disk interface via connector JS3[JK] and JS3[JL]. Up to two floppy drives can be attached. CMOS Setup can be used to enable or disable the floppy disk interface.

Note: The floppy drive used to boot the system (Drive A) should be connected after the twist in the cable, JS3[JK].

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 12: Floppy Disk Interface Connector Pinout

JS3 Pin	Signal Name	Function	JK/JL Pin
1B	Ground	Ground	1
2B	R/LC	Load Head	2
3B	Ground	Ground	3
4B	NC	No Connection	4
5B	Ground	Ground	5
6B	NC	No Connection	6
7B	Ground	Ground	7
8B	INDX*	Beginning Of Track	8
9B	Ground	Ground	9
10B	MTR1*	Motor Enable 1	10
11B	Ground	Ground	11
12B	DRV0*	Drive Select 0	12
13B	Ground	Ground	13
14B	DRE1*	Drive Select 1	14
15B	Ground	Ground	15
16B	MTR0*	Motor Enable 0	16
17B	Ground	Ground	17
18B	DIR	Direction Select	18
19B	Ground	Ground	19
20B	STEP*	Motor Step	20
21B	Ground	Ground	21
22B	WDAT*	Write Data Strobe	22
23B	Ground	Ground	23
24B	WGAT*	Write Enable	24
25B	Ground	Ground	25
26B	TRK0*	Track 0 Indicator	26
27B	Ground	Ground	27
28B	WPRT*	Write Protect	28
29B	Ground	Ground	29
30B	RDAT*	Read Data	30
31B	Ground	Ground	31
32B	HDSL	Head Select	32
33B	Ground	Ground	33
34B	DCHG	Drive Door Open	34

Video Interface

An on-board ATi Rage™ XL/Mobility video controller with 4MB video RAM on the EPM-CPU-10 provides full SVGA video output capabilities for the *EPM-CPU-10*.

VIDEO RESOLUTIONS

This table displays the *EPM-CPU-10* standard VESA SVGA modes and color depths.

Table 13: Video Resolutions

4 MB Video RAM *(EPM-CPU-10)*
640 x 480, 16M colors
800 x 600, 16M colors
1024 x 768, 16M colors
1280 x 1024, 64K colors
1600 X 1200, 64K colors

VIDEO OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 13 for pin and connector location information. An adapter cable, part number CBL-1007 is available to translate JN2 into a standard 15-pin D-Sub SVGA connector.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Table 14: Video Output Pinout

JN2 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red Video	1
3	GND	Ground	7
4	CGRN	Green Video	2
5	GND	Ground	8
6	CBLU	Blue Video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14

FLAT PANEL DISPLAY CONNECTOR

See the *Connector Location Diagram* on page 13 for pin and connector location information.

Table 15: Flat Panel Display Pinout

Pin	Signal Name	Function	Color TFT 18-bit/ 24-bit VBIOS	Color TFT 24-bit	Color LVDS 18-bit	Color LVDS 24-bit	Color TFT 18-bit (only) VBIOS
JN4[1]	+12V	Power Supply					
JN4[2]	+12V	Power Supply					
JN4[3]	GND	Ground					
JN4[4]	GND	Ground					
JN4[5]	+5V	Power Supply					
JN4[6]	+5V	Power Supply					
JN4[7]	ENAVEE	Power sequencing control for LCD bias voltage					
JN4[8]	GND	Ground					
JN4[9]	FP0	Data Output		B0			B0
JN4[10]	FP1	" "		B1			B1
JN4[11]	FP2	" "	B0	B2			B2
JN4[12]	FP3	" "	B1	B3			B3
JN4[13]	FP4	" "	B2	B4			B4
JN4[14]	FP5	" "	B3	B5			B5
JN4[15]	FP6	" "	B4	B6			
JN4[16]	FP7	" "	B5	B7			
JN4[17]	FP8	" "		G0		TX3-	G0
JN4[18]	FP9	" "		G1		TX3+	G1
JN4[19]	FP10	" "	G0	G2			G2
JN4[20]	FP11	" "	G1	G3			G3
JN4[21]	FP12	" "	G2	G4			G4
JN4[22]	FP13	" "	G3	G5			G5
JN4[23]	FP14	" "	G4	G6			
JN4[24]	FP15	" "	G5	G7			
JN4[25]	FP16	" "		R0	TX0-	TX0-	R0
JN4[26]	FP17	" "		R1	TX0+	TX0+	R1
JN4[27]	FP18	" "	R0	R2	TX1-	TX1-	R2
JN4[28]	FP19	" "	R1	R3	TX1+	TX1+	R3
JN4[29]	FP20	" "	R2	R4	TX2-	TX2-	R4
JN4[30]	FP21	" "	R3	R5	TX2+	TX2+	R5
JN4[31]	FP22	" "	R4	R6	TXCLK-	TXCLK-	
JN4[32]	FP23	" "	R5	R7	TXCLK+	TXCLK+	
JN4[33]	GND	Ground					
JN4[34]	GND	Ground					
JN4[35]	SHFCLK	Shift Clock. Pixel clock for flat panel data.					
JN4[36]	FLM	First Line Marker. Flat panel equivalent of VSYNC.					
JN4[37]	DE	Display Enable or M signal (ADCCLK) or BLANK#					
JN4[38]	LP	Latch Pulse. Flat panel equivalent of HSYNC.					
JN4[39]	GND	Ground					
JN4[40]	ENABKL	Enable Backlight. Can be programmed for other functions.					
JN4[41]	DDCDATA	Serial Data					
JN4[42]	DDCCLK	Serial Data					
JN4[43]	+3V	Power Supply					
JN4[44]	+3V	Power Supply					

COMPATIBLE FLAT PANEL DISPLAYS

The following list of flat panel displays are reported to work properly with the ATi Rage ™ XL/Mobility video controller chip used on the *EPM-CPU-10*:

- Sharp LQ057Q3DC02
- Sharp LQ084V1DG21
- Sharp LQ10D344
- Sharp LQ10D346
- Sharp LQ10D367
- Sharp LQ10D421
- Sharp LQ9D161
- Sharp LQ9D340
- Sharp LQ10D131
- Sharp LQ12S08
- Sharp LQ12S31
- Sharp LQ12S41
- Sharp LQ64D142
- Sharp LQ64D341
- Sharp LQ64D343
- Sharp LQ104V1DG11
- Sharp LM64K101
- Sharp LM64P101
- Sharp LM64P839
- Sharp LM32P10
- Sharp LM8V31
- Sharp LM64C35P
- NEC NL6448AC33-27
- NEC NL6448AC33-18
- NEC NL6448AC33-24
- LG Elec. LCA4VE02A
- LG Elec. LP104S2
- Samsung LT104V4-101
- Hitachi TX31D27VC1CAB
- Hitachi TX26D80VC1CAA

Ethernet Interface

The EPM-CPU-10 features an industry-standard 10baseT / 100baseTX Ethernet interface based on the Intel 82551ER interface chip. While this interface is not NE2000 compatible, the 82551ER series is widely supported. Drivers are readily available to support a variety of operating systems such as QNX, VxWorks and other RTOS vendors.

ETHERNET CONNECTOR

Table 16: RJ45 Ethernet Connector

JS4 Pin	Signal Name	Function	JE Pin
11B	IGND	Isolated Ground	4
12B	IGND	Isolated Ground	5
13B	R–	Receive Data –	6
14B	R+	Receive Data +	3
15B	IGND	Isolated Ground	7
16B	IGND	Isolated Ground	8
17B	T–	Transmit Data –	2
18B	T+	Transmit Data +	1

Ethernet Status

A dual LED (D2) indicates the status of the Ethernet port.

Yellow = 10/100
Off = 10 Base T
On = 100 Base T

Green = Link/Activity
On = (solid) Link
Off = (Flickers) Blinks Activity

Watchdog Timer

A watchdog timer circuit is included on the EPM-CPU-10 to reset the CPU or issue a NMI if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

To enable or disable the watchdog to reset the CPU, set or clear bit D0 in I/O port 0E0h (or 1E0h). When changing the contents of the register, make sure not to alter the value of the other bits. To prevent sporadic system reset at the moment the watchdog is enabled, care must be taken to use the procedure shown below.

The following code example enables the watchdog reset:

```
        in    al,E0h   ;Clear bit D2 (WDOGSTA) in the SCR register
        and   al,FBh
        out   E0h,al

loop:   in    al,E0h   ;Loop while bit D2 (WDOGSTA) = 0
        and   al,04h
        jz    loop

        in    al,E0h   ;Enable the watchdog (reset mode)
        or    al,01h
        out   E0h,al
```

To enable or disable the watchdog to issue an NMI, set or clear bit D1 in I/O per 0E0h (or 1E0h). When changing the contents of the register, make sure not to alter the value of the other bits. It is recommend to refresh the watchdog prior to enabling or disabling the watchdog. Bit D2 can be read to determine if watchdog timer has expired.

The following code example enables the watchdog NMI:

```
        in    al,E0h   ;Enable the watchdog(NMI mode)
        or    al,01h
        out   E0h,al
```

Note: The watchdog timer powers up and resets to a disabled state.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1.0 sec minimum). Outputting a 5Ah to the *Watchdog Timer Hold-Off Register* at 0E1h (or 1E1h) resets the watchdog time-out period, see page 44 for additional information.

There is no provision for selecting a different timeout period using software.

The following code example refreshes the watchdog:

```
        mov   al,5Ah
        out   E1h,al
```

CPU Temperature Monitor

A thermometer circuit is located directly under the CPU chip which constantly monitors the case temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

CMOS Setup is used to set the temperature detection threshold. A status bit in the *Special Control Register* can be read to determine if the case temperature is above or below the threshold.

The system can be configured to generate a Non-Maskable Interrupt (NMI) when the temperature exceeds the threshold.

See page 44 for additional information.

USB1.1 Interface

A USB 1.1 (Universal Serial Bus) connector provides a common interface to connect a wide variety of keyboards, modems, mice, and telephony devices to the *EPM-CPU-10*. With USB 1.1, there is no need to have separate connectors for many common PC peripherals.

The USB 1.1 interface on the *EPM-CPU-10* is UHCI (Universal Host Controller Interface) compatible, which provides a common industry software/hardware interface.

This connector is protected with IEC 61000-4-2 (Level 4) rated TVS components to help protect against ESD damage.

Table 17: USB 1.1 Interface Connector

JS4 Pin	Signal Name	Function	JD Pin
1B	USBPWR1	+5V (Protected)	1
2B	GND	Ground	6
3B	USBP00	Channel 0 Data –	2
4B	GND1	Cable Shield	7
5B	USBP01	Channel 0 Data +	3
6B	USBP11	Channel 1 Data +	8
7B	GND1	Cable Shield	4
8B	USBP10	Channel 1 Data –	9
9B	GND	Ground	5
10B	USBPWR1	+5V (Protected)	10

Warning! Connector JD is not numbered in the conventional manner as most dual-row headers. Care must be taken to attach the USB 1.1 adapter cables as shown below to prevent voltage reversal.

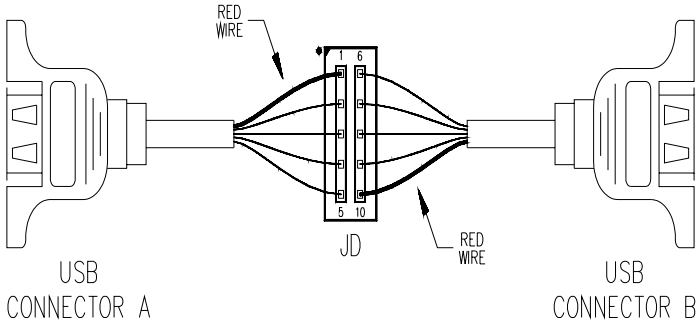


Figure 9. USB 1.1 Connector Orientation Diagram

Expansion Bus

The *EPM-CPU-10* will accept up to four PC/104 and/or four PC/104-*Plus* expansion modules. Both 3.3V and 5.0V modules are supported.

PC/104-*PLUS*

PC/104-*Plus* modules can be secured directly to the underside of the *EPM-CPU-10* The first added module (closest to CPU) is called "Slot 0", the next module is "Slot 1". Make sure to correctly configure the "slot position" jumpers on each PC/104-*Plus* module appropriately.

The BIOS automatically configures the I/O ports and Memory map allocation, including allocation of interrupts.

PC/104

PC/104 modules are stacked under the *EPM-CPU-10* (under any PC/104-*Plus* modules); 16-bit modules first followed by 8-bit PC/104 modules. If necessary, a 40-pin and 64-pin ISA feedthrough connector "extender", and long standoffs may need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 module.

I/O CONFIGURATION

PC/104–*Plus* Modules

No configuration is necessary except to jumper the expansion module for the correct slot number.

PC/104 Modules

PC/104 I/O modules should be addressed in the 100h – 3FFh address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 42. These ports are used by on-board peripherals and video devices.

Memory and I/O Map

MEMORY MAP

The lower 1 MB memory map of the *EPM-CPU-10* is arranged as shown in the following table.

Various blocks of memory space between A0000h and FFFFFh can be shadowed. CMOS setup is used to enable or disable this feature.

Table 18: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS, Flash Page (BIOS Ext.)
D0000h	DFFFFh	PC/104, and DOC
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System DRAM

Note: The memory region from E0000h-EFFFFh is controlled by the Map and Paging Control Register.

I/O MAP

The following table lists the common I/O devices in the *EPM-CPU-10* I/O map. User I/O devices should be added in the 100h – 3FFh range, using care to avoid the devices already in the map as shown below.

Table 19: On-Board I/O Devices

I/O Device	Standard I/O Addresses	Alternate * I/O Addresses
Special Control Register	0E0h	1E0h
Watchdog Hold-Off Register/Revision Indicator	0E1h	1E1h
Special Control Register	0E2h	1E2h
Map and Paging Control Register	0E3h	1E3h
Primary Hard Drive Controller	1F0h – 1F7h	
COM2 Serial Port	2F8h – 2FFh	
Super I/O	370h – 371h	
LPT1 Parallel Port	378h – 37Fh	
SVGA Video	3B0h – 3DFh	
Floppy Disk Controller	3F0h – 3F7h	
COM1 Serial Port	3F8h – 3FFh	

* User selectable via CMOS Setup.

Interrupt Configuration

The *EPM-CPU-10* has the standard complement of PC type interrupts. Ten non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines are automatically allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configuration is handled through CMOS setup. The switches in the diagram below indicate the various CMOS Setup options. Closed switches show factory default settings.

The temperature monitor interrupt and watchdog interrupt are enabled/disabled with the *Special Control Register*.

Note: If your design needs to use interrupt lines on the PC/104 bus, we recommend using IRQ5, IRQ9, and/or IRQ10.

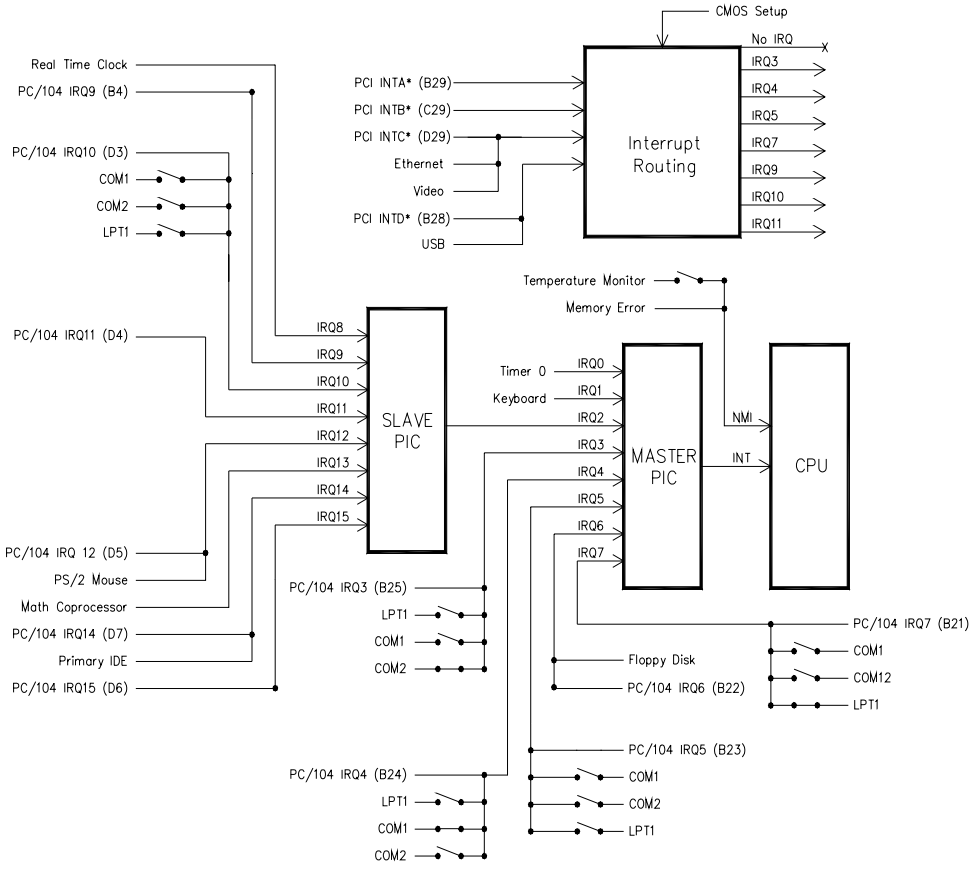


Figure 10. Interrupt Circuit Diagram

Special Control Register

SCR (READ/WRITE) 00E0h (or 01E0h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
LED	OVERTEMP	GPI	GPO	HDOGNMI	WDOGSTA	WDOGNMI	WDOGRST

Table 20: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	LED	**Light Emitting Diode** — Controls the programmable LED connected to JS4[27A/28A] LED = 0 Turns LED off. LED = 1 Turns LED on.
D6	OVERTEMP	**Temperature Status** — Indicates CPU die temperature. TEMP = 0 CPU die temperature is below value set in CMOS Setup TEMP = 1 CPU die temperature is above value set in CMOS Setup ***Note:*** *This bit is a read-only bit.*
D5	GPI	**General Purpose Input** — Indicates the status of TTL input at JS3[38B]. GPI = 0 Logic High GPI = 1 Logic Low ***Note:*** *This bit is a read-only bit.*
D4	GPO	**General Purpose Output** — Controls TTL output at JS3[37B]. GPO = 0 Logic High GPO = 1 Logic Low
D3	HDOGNMI	**Non-Maskable Interrupt Enable** — Controls the generation of Non-Maskable Interrupts whenever the CPU temperature sensor detects an over-temperature condition. HDOGNMI = 0 Disable HDOGNMI = 1 Enable
D2	WDOGSTA	**WDOG STATUS** — Indicates if the watchdog timer has expired. WDOGSTA = 0 Timer has not expired. WDOGSTA = 1 Timer has expired.
D1	WDOGNMI	**Watch Dog Non-Maskable Interrupt Enable** — Enables the generation of a Non-maskable interrupt when the watchdog timer expires. WDOGNMI = 0 Disables WDOGNMI = 1 Enables
D0	WDOGRST	**Watch Dog Reset Enable** — Enables and disables the watchdog timer reset circuit. WDOGRST = 0 Disables the watchdog timer. WDOGRST = 1 Enables the watchdog timer.

Revision Indicator Register

REVIND (READ ONLY) 00E1h (or 01E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	TCO	REV1	REV0

This register is used to indicate the revision level of the *EPM-CPU-10* product.

Bit	Mnemonic	Description
D7-D3	PC4-PC0	**Product Code** — These bits are hard coded to represent the product type. The EPM-CPU-10 will always read as 00010. Other codes are reserved for future products. **PC4 PC3 PC2 PC1 PC0 Product Code** 0 0 0 1 0 EPM-CPU-10 ***Note:*** *These bits are read-only.*
D2	TCO	**Throttling Code** — This bit specifies how throttling is enabled at power-up and reset. 0 = EPM-CPU-10h EPM-CPU-10k No Throttling 1 = EPM-CPU-10g EPM-CPU-10m Throttling set at 37.5% ***Note:*** *This bit is read-only.*
D1-D0	REV1-REV0	**Revision Level** — These bits are representative of the EPM-CPU-10 circuit revision level. **REV1 REV0 Revision Level** 0 0 Rev 3 or earlier 0 1 Rev 3.01 1 0 Rev 4.00 or later 1 1 Reserved ***Note:*** *These bits are read-only.*

Watchdog Timer Hold-Off Register

WDHOLD (WRITE ONLY) 00E1h (or 01E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the EPM-CPU-10 board to reset the CPU or issue an NMI if proper software execution fails or a hardware malfunction occurs. The watchdog timer is enabled/disabled by writing to bit D0 of SCR

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1 second minimum). Writing a 5Ah to WDHOLD resets the watchdog timeout period, preventing the CPU from being reset or generation of NMI for the next 1 second.

Special Control Register

SCR (READ/WRITE) 00E2h (or 01E2h via CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	JPI	Throttle

Table 21: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7-D2	Reserved	**Reserved** — These bits have no function.
D1	JPI	**Jumper Input** — Indicates the status of jumper VS2[5-6] JPI = 0 Jumper VS2[5-6] = Out JPI = 1 Jumper VS2[5-6] = In ***Note:*** *This bit is a read-only bit.*
D0	Throttle	**Throttling Enable** — Enables and disables CPU throttling. Throttling = 0 Disable Throttling = 1 Enable ***Note:*** *Models H & K are read write. Models G & M are set only and cleared by Reset.*

Map and Paging Control Register

MPCR (READ/WRITE) 00E3H (or 01E3h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
FPGEN	DOCEN1	DOCEN0	SB-SEL	VB-SEL	PG2	PG1	PG0

Table 22: Map and Paging Control Register Bit Assignments

Bit	Mnemonic	Description
D7	FPGEN	**FLASH Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the on-board FLASH memory. FPGEN = 0 FLASH page frame disabled. FPGEN = 1 FLASH page frame enabled.
D6-D5	DOCEN1-DOCENO	**DiskOnChip Enable** — Enables a 8K page frame used to gain access to the Disk on Chip. **PG2** **PG1** **Memory Range within DiskOnChip** 0 0 Disabled 0 1 D000:0 1 0 D800:0 1 1 DE00:0
D4	SB-SEL	**System BIOS Selection** — Indicates the status of jumper VS2[1-2]. SB-SEL = 0 Jumper out, Secondary System BIOS selected. SB-SEL = 1 Jumper in, Primary System BIOS selected. ***Note:*** *This is a read-only bit*
D3	VB-SEL	**Video BIOS Selection** — Indicates the status of jumper VS2[3-4]. VB-SEL = 0 Jumper out, Secondary System BIOS selected. VB-SEL = 1 Jumper in, Primary System BIOS selected. ***Note:*** *This is a read-only bit*
D2-D0	PG2-PG0	**Page Select** — Selects which 64K block of FLASH will be mapped into the page frame at E0000h to EFFFFh **PG2** **PG1** **PG0** **Memory Range within FLASH** 0 0 0 000000h to 00FFFFh 0 0 1 010000h to 01FFFFh 0 1 0 020000h to 02FFFFh 0 1 1 030000h to 03FFFFh 1 0 0 040000h to 04FFFFh 1 0 1 050000h to 05FFFFh 1 1 0 060000h to 06FFFFh 1 1 1 070000h to 07FFFFh

Appendix A — Other References

PC Chipset *440BX Chipset*	Intel Corporation (http://developer.intel.com/design/index.htm)
Ethernet Controller *Intel 82551ER*	Intel Corporation (http://developer.intel.com/design/index.htm)
Video Controller	ATi Rage XL/Mobility (http://ati.amd.com/)
Disk On Chip *DOC2000*	M-Systems Inc. (http://www.m-sys.com/)
PC/104 Specification	VersaLogic Corp. (http://www.versalogic.com/support/pdf/PC104Specv246.pdf)
PC/104-*Plus* Specification	VersaLogic Corp. (http://www.versalogic.com/support/pdf/PC104-PlusV125.pdf)
CPU Chips *Celeron* *Pentium III*	Intel Corporation (http://developer.intel.com/design/index.htm)
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press (http://www.microsoft.com/learning/books/)
General PC Documentation *The Undocumented PC*	Powell's Books (www.powells.com)