## LV8415XA

Bi-CMOS IC

## Blurring correction driver H bridge $\times 2$-channel driver

ON Semiconductor ${ }^{\text {® }}$
http:/lonsemi.com

## Overview

LV8415XA is dual channel H-bridge driver IC for digital still camera.

## Function

- Actuator driver (saturation drive H bridge) $\times 2$-channel
- Hall Amplifier $\times 2$-channel
- Constant current hall bias circuit $\times 2$-channel
- General-purpose amplifier $\times 2$-channel
- With built-in for PWM signal generation logic circuit $\times 2$-channel
- 8-bit DAC for hall bias $\times 2$-channel
- 8-bit DAC for hall amplifier offset adjustment $\times 2$-channel


WLP32L

- Three line serial input
- Two systems in power supply ( $\mathrm{V}_{\mathrm{M}}$ : for actuator, $\mathrm{V}_{\mathrm{CC}}$ )
- With built-in thermal protection circuit
- With built-in low voltage malfunction prevention circuit


## Specifications

Absolute Maximum Ratings at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage 1 | $\mathrm{V}_{\mathrm{M}}$ max |  | 6 | V |
| Supply voltage 2 | $\mathrm{V}_{\text {CC }}$ max |  | 6 | V |
| Output peak current | lo peak | OUT1 to 2 ( $\mathrm{t} \leq 10 \mathrm{msec}$, duty $\leq 20 \%$ ) | 600 | mA |
| Output current | $\mathrm{I}_{0} \mathrm{max}$ | OUT1 to 2 | 350 | mA |
| Hall bias current | IHB max |  | 5 | mA |
| Allowable power dissipation | Pd max | On a specified board * | 1 | W |
| Operating temperature | Topr |  | -20 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

* Specified board: $40.0 \mathrm{~mm} \times 50.0 \mathrm{~mm} \times 0.8 \mathrm{~mm}$, Four layers fiberglass epoxy circuit board.
* 2 Tjmax $=150^{\circ} \mathrm{C}$ Please design PCB so that internal chip temperature does not exceed $150^{\circ} \mathrm{C}$.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at $\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :--- | :--- | :--- | :--- | :---: |
| Supply voltage range 1 | $\mathrm{~V}_{\mathrm{M}}$ |  | 2.7 to 5.5 | V |
| Supply voltage range 2 | $\mathrm{~V}_{\mathrm{CC}}$ |  | 2.7 to 5.5 | V |
| Logic input voltage | $\mathrm{V}_{\mathrm{IN}}$ |  | 0 to $\mathrm{V}_{\mathrm{CC}}+0.3$ | V |

## ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

LV8415XA
Electrical Characteristics at $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{M}}=5.0 \mathrm{~V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| Current consumption when standing by | ${ }^{\text {I CCO }}$ | ST = "L" |  |  | 1.0 | $\mu \mathrm{A}$ |
| VM current consumption | ${ }^{\prime} \mathrm{M}$ | $\mathrm{V}_{\mathrm{M}}=5.0 \mathrm{~V}, \mathrm{ST}=$ " H ", no load |  |  | 10 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {CC }}$ current consumption | ${ }^{\text {ICC }}$ | ST = "H", no load |  | 2 | 3.2 | mA |
| $\mathrm{V}_{\text {CC }}$ low voltage cutting voltage | VTHVCC |  | 2.1 | 2.40 | 2.6 | V |
| Low voltage hysteresis voltage | VTHHYS |  | 100 | 150 | 200 | mV |
| Thermal shutdown temperature | TSD | Design guarantee | 155 | 175 | 195 | ${ }^{\circ} \mathrm{C}$ |
| Thermal hysteresis width | $\Delta T S D$ | Design guarantee | 15 | 35 | 55 | ${ }^{\circ} \mathrm{C}$ |
| H bridge output (OUT1-2) |  |  |  |  |  |  |
| Output on resistance | Ronu | $\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$, Upper-side on resistance |  | 0.7 | 0.98 | $\Omega$ |
|  | Rond | $\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$, Under-side on resistance |  | 0.5 | 0.7 | $\Omega$ |
| Output leakage current | IO leak |  |  |  | 1 | $\mu \mathrm{A}$ |
| Diode forward voltage | VD | $I D=-100 \mathrm{~mA}$ |  | 0.7 |  | V |
| Operational amplifier (OP-AMP1-4) |  |  |  |  |  |  |
| Input offset voltage | OP_VIO |  |  | $\pm 1$ | $\pm 5$ | mV |
| Input offset current | OP_ІІ |  |  | $\pm 5$ | $\pm 50$ | nA |
| Input bias current | OP_IB |  |  | 30 | 250 | nA |
| Equal phase input voltage range | VICM |  | 0 |  | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Equal phase signal removal ratio | CMR | $\mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega, \mathrm{VIN}=1 \mathrm{mV}$ (open loop gain) | 60 | 80 |  | dB |
| Large amplitude voltage range | VG | $\mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | 1 | 10 |  | $\mathrm{V} / \mathrm{mV}$ |
| Output voltage range | $\mathrm{V}_{\mathrm{O}} \mathrm{H}$ | $\mathrm{R}_{\mathrm{L}}=20 \mathrm{k} \Omega$ | $\mathrm{V}_{\mathrm{CC}}-0.2$ |  |  | V |
|  | $\mathrm{V}_{\mathrm{O}} \mathrm{L}$ |  |  |  | 0.2 | V |
| Power supply change removal ratio | SVR |  | 65 | 85 |  | dB |
| Output current (sink/source) | OP_IO |  | 1 | 2 |  | mA |
| Hall bias (HB1-2) |  |  |  |  |  |  |
| Output current | IHB | $\mathrm{RHG}=1 \mathrm{k} \Omega$, VHBIN $=1.0 \mathrm{~V}$ | 0.95 | 1.00 | 1.05 | mA |
| Output saturation voltage | VSATHB | $\mathrm{I}_{\mathrm{HB}}=1 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{CC}}-0.2$ |  |  | V |
| Reference voltage |  |  |  |  |  |  |
| Reference voltage | VREF |  | 1.60 | 1.65 | 1.70 | V |
| Reference voltage load characteristic | VRref | $\mathrm{I}_{\text {REF }}=100 \mu \mathrm{~A}$ | 1.60 | 1.65 | 1.70 | V |
| Internal CLK frequency for PWM drive |  |  |  |  |  |  |
| CLK frequency | Fclk |  | 13.5 | 15 | 17.25 | MHz |
| Control pin (ST, SCLK, DATA, STB) |  |  |  |  |  |  |
| Built-in pull-down resistance | Rin |  | 50 | 100 | 200 | k ת |
| Input current | ${ }_{1} \mathrm{~N}^{\text {L }}$ | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ |  |  | 1.0 | $\mu \mathrm{A}$ |
|  | ${ }_{\text {IN }}{ }^{\text {H }}$ | $\mathrm{V}_{\text {IN }}=3.3 \mathrm{~V}$ | 20 | 33 | 50 | $\mu \mathrm{A}$ |
| Input " L " level voltage | $\mathrm{V}_{\text {IN }} \mathrm{L}$ |  |  |  | 1.0 | V |
| Input "H" level voltage | $\mathrm{V}_{\text {IN }} \mathrm{H}$ |  | 2.5 |  |  | V |

## Block Diagram




## Package Dimensions



SIDE VIEW



## Pin Assignment


(NC_TEST) is pin only for the test. Please NC_TESTpin connect GND line.
$\bigcirc$ Power supply pin
GND pinOutput pin
Logic control pinAnalog control pin
Ball side view

## Pin function

| Pin No. | Pin name | Pin function | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { E2 } \\ & \text { E3 } \\ & \text { E4 } \\ & \text { E5 } \end{aligned}$ | ST <br> SCLK <br> DATA <br> STB | Input pin. <br> High level 2 V to $\left(\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}\right)$ <br> Low level 0 to $0.5 \mathrm{~V}\left(\mathrm{~V}_{\mathrm{CC}}=3.3 \mathrm{~V}\right)$ |  |
| $\begin{aligned} & \hline \text { F1 } \\ & \text { F2 } \\ & \text { F4 } \\ & \text { F5 } \\ & \text { E1 } \\ & \text { F3 } \end{aligned}$ | OUT1A OUT1B OUT2A OUT2B VM PGND | Output pin. (PWM output) <br> VM : POWER - Power supply pin. PGND : POWER - GND pin. |  |
| $\begin{aligned} & \hline \text { D1 } \\ & \text { D6 } \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}$ SGND | Signal system power supply pin Signal system GND pin |  |
| $\begin{aligned} & \text { C1 } \\ & \text { B1 } \\ & \text { C6 } \\ & \text { B6 } \end{aligned}$ | HB1 <br> HGND1 <br> HB2 <br> HGND2 | HB1, 2 pin <br> Hall bias source pin <br> HGND1, 2 pin <br> Hall bias current setting pin |  |
| $\begin{aligned} & \text { A1 } \\ & \text { A2 } \\ & \text { A3 } \\ & \text { A6 } \\ & \text { A5 } \\ & \text { A4 } \end{aligned}$ | $\mathrm{V}_{\mathrm{IN}^{+1}}$ <br> $\mathrm{V}_{\mathrm{IN}}-1 \mathrm{~A}$ <br> $V_{I N^{-1 B}}$ <br> $\mathrm{V}_{\mathrm{IN}}+2$ <br> $\mathrm{V}_{\mathrm{IN}}-2 \mathrm{~A}$ <br> $V_{I N}-2 B$ | Hall amplifier input pin <br> $\mathrm{V}_{\mathrm{IN}^{+}}$Hall amplifier+ input pin <br> $\mathrm{V}_{\mathrm{IN}}$-A Hall amplifier- input pin <br> $\mathrm{V}_{\mathrm{IN}}$-B LPF formation pin <br> (The filter is formed for the noise removal.) |  |
| $\begin{aligned} & \text { B3 } \\ & \text { B4 } \end{aligned}$ | VOUT1 VOUT2 | Hall amplifier output pin. <br> VOUT1 : Hall amplifier 1ch output pin. <br> VOUT2 : Hall amplifier 2ch output pin. |  |

Continued from preceding page.

| Pin No. | Pin name | Pin function | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{D} 2 \\ & \mathrm{C} 2 \\ & \mathrm{D} 5 \\ & \mathrm{C} 5 \end{aligned}$ | $\mathrm{V}_{1 \mathrm{~N}^{+3}}$ <br> $V_{1 N^{-3}}$ <br> $\mathrm{V}_{1 \mathrm{~N}^{+4}}$ <br> $\mathrm{V}_{\mathrm{IN}}{ }^{+4}$ | General purpose amplifier input pin. <br> $\mathrm{V}_{\mathrm{IN}^{+3}}$ : 3ch general purpose amplifier+ input pin <br> $\mathrm{V}_{\mathrm{IN}} \mathrm{N}^{-3}$ : 3ch general purpose amplifier- input pin <br> $\mathrm{V}_{\mathrm{IN}^{+4}}$ : 4ch general purpose amplifier+ input pin <br> $\mathrm{V}_{\mathrm{IN}}-4$ : 4ch general purpose amplifier- input pin |  |
| $\begin{aligned} & \text { B2 } \\ & \text { B5 } \end{aligned}$ | VOUT3 <br> VOUT4 | General purpose amplifier output pin. <br> VOUT3 : 3ch general purpose amplifier output pin <br> VOUT4 : 4ch general purpose amplifier output pin |  |
| E6 | VREF | Internal standard voltage pin $\mathrm{V}_{\mathrm{CC}} / 2$ output |  |
| F6 | NC-TEST | ```N.C. pin TEST pin Please NC_TEST pin connect GND line.``` |  |

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3 line serial communication electrical Characteristics at $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{M}}=5.0 \mathrm{~V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| Serial data forwarding pin |  |  |  |  |  |  |
| Logic pin input current | ${ }_{1} \mathrm{~N}^{\text {L }}$ | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ (SCLK, DATA, STB) |  |  | 1.0 | $\mu \mathrm{A}$ |
|  | ${ }_{\text {IN }} \mathrm{H}$ | $\mathrm{V}_{\text {IN }}=3.3 \mathrm{~V}$ (SCLK, DATA, STB) |  | 33 | 50 | $\mu \mathrm{A}$ |
| Input "H" level voltage | $\mathrm{V}_{1 N^{\prime}} \mathrm{H}$ | SCLK, DATA, STB | 2.5 |  |  | V |
| Input "L" level voltage | $\mathrm{V}_{\text {IN }} \mathrm{L}$ | SCLK, DATA, STB |  |  | 1.0 | V |
| Minimum SCLK "H" pulse width | $\mathrm{Tsch}^{\text {H }}$ |  | 0.1 |  |  | $\mu \mathrm{s}$ |
| Minimum SCLK " L " pulse width | $\mathrm{T}_{\text {SCL }}$ |  | 0.1 |  |  | $\mu \mathrm{s}$ |
| STB regulation time | Tlat |  | 0.1 |  |  | $\mu \mathrm{s}$ |
| Minimum STB pulse width | Tlatw |  | 0.1 |  |  | $\mu \mathrm{s}$ |
| Data set-up time | Tds |  | 0.1 |  |  | $\mu \mathrm{S}$ |
| Data hold time | Tdh |  | 0.1 |  |  | $\mu \mathrm{s}$ |
| maximum CLK frequency | Fclk |  |  |  | 4 | MHz |



Serial data timing condition
Serial data input timing chart


It inputs it from A0 in order of D11. The data transfer is done by the rising edge, and after all data transfers, the latch does all data to SCLK by the STB signal standing up. The STB signal accepts and the internal logic of IC doesn't accept the SCLK signal during "H".

Serial logic map
PWMh - bridge relation serial map

| Input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Setting mode | Set content | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 |  |  |  |
| 0 | 0 | 0 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1ch PWM Duty set | 100\% | Reverse |
|  |  |  |  | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 511/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 510/512 $\times 100 \%$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\ldots$ |  |
|  |  |  |  | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | 2/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | $1 / 512 \times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | 0\% | Middle point |
|  |  |  |  | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | 1/512 $\times 100 \%$ | Normal rotation |
|  |  |  |  | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | $2 / 512 \times 100 \%$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\ldots$ |  |
|  |  |  |  | * | * | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 509/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | $510 / 512 \times 100 \%$ |  |
|  |  |  |  | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 511/512 $\times 100 \%$ |  |
| 1 | 0 | 0 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2ch PWM Duty set | 100\% | Reverse |
|  |  |  |  | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 511/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 510/512 $\times 100 \%$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\ldots$ |  |
|  |  |  |  | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | 2/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | $1 / 512 \times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | 0\% | Middle <br> point |
|  |  |  |  | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | 1/512 $\times 100 \%$ | Normal rotation |
|  |  |  |  | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | $2 / 512 \times 100 \%$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\ldots$ |  |
|  |  |  |  | * | * | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 509/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 510/512 $\times 100 \%$ |  |
|  |  |  |  | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 511/512 $\times 100 \%$ |  |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 1ch hall bias set <br> (8bit DAC) | 0V |  |
|  |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $1 / 255 \times$ VREF |  |
|  |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $2 / 255 \times$ VREF |  |
|  |  |  |  |  |  |  |  |  |  |  |  | * | * | * | * |  | $\ldots$ |  |
|  |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | 253/255 $\times$ VREF |  |
|  |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | 254/255 $\times$ VREF |  |
|  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | VREF |  |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 2ch hall bias set <br> (8bit DAC) | 0V |  |
|  |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $1 / 255 \times$ VREF |  |
|  |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $2 / 255 \times$ VREF |  |
|  |  |  |  |  |  |  |  |  |  |  |  | * | * | * | * |  | $\ldots$ |  |
|  |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | 253/255 $\times$ VREF |  |
|  |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $254 / 255 \times$ VREF |  |
|  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | VREF |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 1ch hall amplifier offset adjustment (8bit DAC) | 0V |  |
|  |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $1 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $2 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  | * | * | * | * |  | 2 |  |
|  |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $253 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $254 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $\mathrm{V}_{\mathrm{CC}}$ |  |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 2ch hall amplifier offset adjustment (8bit DAC) | 0V |  |
|  |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $1 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * |  | $2 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  | * | * | * | * |  | $\ldots$ |  |
|  |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $253 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $254 / 255 \times \mathrm{V}_{\mathrm{CC}}$ |  |
|  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * |  | $\mathrm{V}_{\mathrm{CC}}$ |  |

The PWMh-bridge driver's ON/OFF operation is done with the ST pin.

Hall amplifier gain setting range
Hall amplifier relation serial map

| Input |  |  |  |  |  |  |  | Setting mode | Hall amplifier magnification ()Inside: Resistance |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 |  |  |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1ch hall amplifier gain setting <br> ( " 3 " Resistance $\div$ " 2 " Resistance) | 10 (36k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 20 (72k/3.6k) |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 40 (144k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 50 (180k//3.6k) |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 60 (216k//3.6k) |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 70 (252k//3.6k) |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 90 (324k//3.6k) |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 100 (360k//3.6k) |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 110 (396k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 120 (432k//3.6K) |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 140 (504k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 150 (540k/3.6k) |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 160 (570k/3.6k) |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 170 (612k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 190 (684k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 200 (720k/3.6k) |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 2ch hall amplifier gain setting <br> (" 3 " Resistance $\div$ " 2 " Resistance) | 10 (36k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 20 (72k/3.6k) |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 40 (144k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 50 (180k//3.6k) |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 60 (216k/3.6k) |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 70 (252k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 90 (324k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 100 (360k/3.6k) |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 110 (396k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 120 (432k/3.6K) |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 140 (504k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 150 (540k/3.6k) |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 160 (570k/3.6k) |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 170 (612k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 190 (684k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 200 (720k/3.6k) |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1ch hall amplifier offset resistance / input resistance <br> ( " 1 " Resistance $\div$ " 2 " Resistance) | 10 (36k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 20 (72k/3.6k) |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 40 (144k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 50 (180k/3.6k) |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 60 (216k/3.6k) |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 70 (252k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 90 (324k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 100 (360k/3.6k) |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 110 (396k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 120 (432k//3.6K) |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 140 (504k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 150 (540k//3.6k) |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 160 ( $570 \mathrm{k} / 3.6 \mathrm{k}$ ) |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 170 (612k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 190 (684k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 200 (720k//3.6k) |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 2ch hall amplifier offset resistance / input resistance <br> ( " 1 " Resistance $\div$ " 2 " Resistance) | 10 (36k/3.6k) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 20 (72k/3.6k) |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 40 (144k//3.6k) |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 50 (180k/3.6k) |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 60 (216k/3.6k) |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 70 (252k/3.6k) |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 90 (324k/3.6k) |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 100 (360k//3.6k) |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 110 (396k//3.6k) |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 120 (432k//3.6K) |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 140 ( $504 \mathrm{k} / 3.6 \mathrm{k}$ ) |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 150 ( $540 \mathrm{k} / 3.6 \mathrm{kk}$ ) |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 160 (570k//3.6k) |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 170 (612k//3.6k) |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 190 ( $684 \mathrm{k} / 3.6 \mathrm{k}$ ) |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 200 (720k//3.6k) |

General-purpose amplifier ON/OFF setting

| Input |  |  |  |  |  |  |  | Setting mode | Set content |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## PWM circuit accuracy setting

| Input |  |  |  |  |  | Setting mode | Set content | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 | D0 | D1 |  |  |  |
| 1 | 0 | 1 | 1 | 0 | 0 | PWM accuracy setting | 10bit resolution | Initial value |
|  |  |  |  | 0 | 1 |  | 11bit resolution |  |
|  |  |  |  | 1 | 0 |  | 12bit resolution |  |
|  |  |  |  | * | * |  | - |  |

PWM pulse width of moving
1ch ( X axis side)

| Input [3:0] |  |  |  |  |  |  |  | Setting mode | Moving pulse number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 |  |  |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1ch ( X axis) side width of moving | 0 (Initialization) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 1 |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 2 |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 3 |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 4 |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 5 |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 6 |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 7 |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 8 |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 9 |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 10 |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 11 |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 12 |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 13 |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 14 |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 15 |

Note : 1 pulse = 1CLK
2ch (Y axis side)

| Input [7:4] |  |  |  |  |  |  |  | Setting mode | Moving pulse number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 | D4 | D5 | D6 | D7 |  |  |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 2ch (Y axis) side width of moving | 0 (Initialization) |
|  |  |  |  | 1 | 0 | 0 | 0 |  | 1 |
|  |  |  |  | 0 | 1 | 0 | 0 |  | 2 |
|  |  |  |  | 1 | 1 | 0 | 0 |  | 3 |
|  |  |  |  | 0 | 0 | 1 | 0 |  | 4 |
|  |  |  |  | 1 | 0 | 1 | 0 |  | 5 |
|  |  |  |  | 0 | 1 | 1 | 0 |  | 6 |
|  |  |  |  | 1 | 1 | 1 | 0 |  | 7 |
|  |  |  |  | 0 | 0 | 0 | 1 |  | 8 |
|  |  |  |  | 1 | 0 | 0 | 1 |  | 9 |
|  |  |  |  | 0 | 1 | 0 | 1 |  | 10 |
|  |  |  |  | 1 | 1 | 0 | 1 |  | 11 |
|  |  |  |  | 0 | 0 | 1 | 1 |  | 12 |
|  |  |  |  | 1 | 0 | 1 | 1 |  | 13 |
|  |  |  |  | 0 | 1 | 1 | 1 |  | 14 |
|  |  |  |  | 1 | 1 | 1 | 1 |  | 15 |

Note : 1 pulse = 1CLK
The ON/OFF operation of the hall amplifier and the hall bias is done with the ST pin.
Note : An initial value of A0 to A3 = 1111 is a static test mode. Use it specifying data D0 for one.
TEST mode setting

| Input |  |  |  | Setting mode | Content | Remarks |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0 | A1 | A2 | A3 |  |  |  |  |
| 1 | 1 | 1 | 1 | 0 | NC pin_TEST mode | External CLK | It uses it by the shipment inspection. |
|  |  |  |  | 1 |  | Internal CLK operation |  |

[^0]Hall bias, Offset adjustment circuit configuration


Hall amplifier, Hall bias equivalent circuit
About the gain adjustment
The resistance ratio of " 2 " and " 3 " is adjusted in figure and the gain is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

## About the Offset adjustment

The resistance ratio of " 1 " and " 2 " is adjusted in figure and the Offset is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

## Note in design

- Stand-by function

IC becomes a stand-by state at $\mathrm{ST}=$ "L", and IC enters the state of operation at $\mathrm{ST}=$ " H ". Moreover, the register in IC is reset as for $\mathrm{ST}=$ "L" at times.

- Hall bias

The constant current output is built into for the hall element drive. The constant current value is set from detection resistance (RHG) connected from the HBIN pin impression voltage and the HGND pin between GND.

Constant current value ( $\mathrm{I}_{\mathrm{O}}$ ) $=$ HBIN voltage $\div$ Detection resistance


Constant current value ( IO ) becomes about 1 mA when assuming HBIN pin impressed voltage $=1.0 \mathrm{~V}$ and detection resistance $=1 \mathrm{k} \Omega$ from the above-mentioned calculation type. Moreover, the HGND pin must connect with the HB pin, and connect the detection resistance of a large value as much as possible when you do not use the hall bias circuit.

- Operation amplifier

Impress the bias to the $\mathrm{V}_{\mathrm{IN}}{ }^{+}$pin, and compose the buffer by the connection to the VOUT pin in the $\mathrm{V}_{\mathrm{IN}}$ pin in the operational amplifier not used.


ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
| :---: | :---: | :---: |
| LV8415XA-MH | WLP32L $(2.47 \mathrm{~mm} \times 2.47 \mathrm{~mm})$ <br> (Pb-Free / Halogen Free) | $5000 /$ Tape \& Reel |

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[^0]:    Note : External CLK mode is for the shipment inspection. Use it with internal CLK. Use it after it internal CLK switches because default is external CLK mode.

