



**3.3V, PRECISION, 33MHz to 500MHz  
PROGRAMMABLE LVPECL AND HSTL BUS  
CLOCK SYNTHESIZER**

**Precision Edge®  
SY89531L**

**FEATURES**

- Integrated synthesizer plus fanout buffers, clock drivers, and translator in a single 64-pin package
- 3.3V ±10% power supply
- Low jitter: <50ps cycle-to-cycle
- Low pin-to-pin skew: <50ps
- 33MHz to 500MHz output frequency range
- Direct interface to crystal: 14MHz to 18MHz
- LVPECL/HSTL outputs
- TTL/CMOS compatible control logic
- 3 independently programmable output frequency banks:
  - 9 differential output pairs @BankB (HSTL)
  - 2 differential output pairs @BankA (LVPECL)
  - 2 differential output pairs @BankC (LVPECL)
- ExtVCO input allows synthesizer and crystal interface to be bypassed
- Available in 64-pin EPAD-TQFP



Precision Edge®

**DESCRIPTION**

The SY89531L programmable clock synthesizer/driver is part of a 3.3V, high-frequency, precision PLL-based clock synthesizer family optimized for multi-frequency, multi-processor server, enterprise networking and other computing applications that require the highest precision and integration. The device integrates the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop)-based synthesizer
- Fanout buffers
- Clock generator (dividers)
- Logic translation (LVPECL, HSTL)

This level of integration minimizes the additive jitter and part-to-part skew associated with the discrete alternative, resulting in superior system-level timing as well as reduced board space and power. For applications that must interface to a reference clock, see the SY89536L.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

**APPLICATIONS**

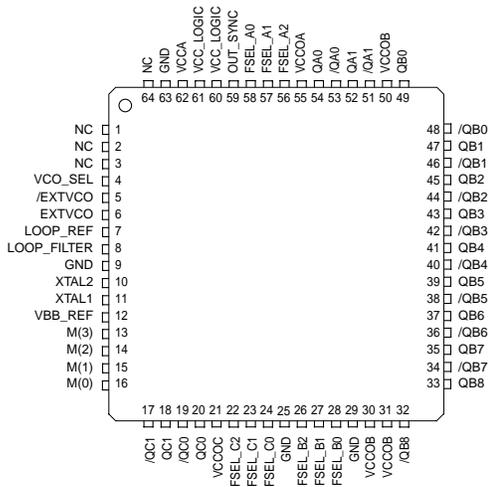
- Servers
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

**PRODUCT SELECTION GUIDE**

| Device    | Input   |           | Output |        |        |
|-----------|---------|-----------|--------|--------|--------|
|           | Crystal | Reference | BankA  | BankB  | BankC  |
| SY89531L  | X       |           | LVPECL | HSTL   | LVPECL |
| SY89532L* | X       |           | LVPECL | LVPECL | LVPECL |
| SY89533L* | X       |           | LVPECL | LVDS   | LVPECL |
| SY89534L* |         | X         | LVPECL | LVPECL | LVPECL |
| SY89535L* |         | X         | LVPECL | LVDS   | LVPECL |
| SY89536L* |         | X         | LVPECL | HSTL   | LVPECL |

\*Refer to individual data sheet for details.

**PACKAGE/ORDERING INFORMATION**



**64-Pin EPAD-TQFP (H64-1)**

**Ordering Information<sup>(1)</sup>**

| Part Number                    | Package Type | Operating Range | Package Marking                            | Lead Finish      |
|--------------------------------|--------------|-----------------|--|------------------|
| SY89531LHC                     | H64-1        | Commercial      | SY89531LHC                                 | Sn-Pb            |
| SY89531LHCTR <sup>(2)</sup>    | H64-1        | Commercial      | SY89531LHC                                 | Sn-Pb            |
| SY89531LHZ <sup>(3)</sup>      | H64-1        | Commercial      | SY89531LHZ with Pb-Free bar-line indicator | Matte-Sn Pb-Free |
| SY89531LHZTR <sup>(2, 3)</sup> | H64-1        | Commercial      | SY89531LHZ with Pb-Free bar-line indicator | Matte-Sn Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**PIN DESCRIPTION****Power**

| Pin Number                     | Pin Name   | Pin Function   |
|--------------------------------|--|--|
| 60, 61                         | V <sub>CC_Logic</sub>  | Power for Core Logic: Connect to 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.  |
| 62                             | V <sub>CCA</sub>   | Power for PLL: Connect to “quiet” 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB. |
| 55<br>30, 31, 50<br>21         | V <sub>CCO</sub> A<br>V <sub>CCO</sub> B<br>V <sub>CCO</sub> C | Power for Output Drivers: Connect all V <sub>CCO</sub> A and V <sub>CCO</sub> C pins to 3.3V supply and V <sub>CCO</sub> B pins to 1.8V supply.    |
| 9, 25, 63, 29<br>(exposed pad) | GND  | Ground: Exposed pad must be soldered to a ground plane.  |

**Configuration**

| Pin Number  | Pin Name     | Pin Function  |
|-------------|--------------|---|
| 4           | VCO_SEL      | LVTTL/CMOS Compatible Input: Selects between internal or external VCO. For external VCO, leave floating. Default condition is logic HIGH. Internal 25kΩ pull-up. When tied LOW, internal VCO is selected. |
| 7           | LOOP REF     | Analog Input/Output: Provides the reference voltage for PLL loop filter.  |
| 8           | LOOP FILTER  | Analog Input/Output: Provides the loop filter for PLL. See “ <i>External Loop Filter Considerations</i> ” for loop filter values.   |
| 13,14,15,16 | M (3:0)      | LVTTL/CMOS Compatible Input: Used to change the PLL feedback divider. Internal 25kΩ pull-up. M0 = LSB. Default is logic HIGH. See “ <i>Feedback Divide Select</i> ” table.                                |
| 22, 23, 24  | FSEL_C (2:0) | LVTTL/CMOS Compatible Input: Bank C post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See “ <i>Post-Divide Frequency Select</i> ” table. FSEL_C0 = LSB.                                   |
| 26, 27, 28  | FSEL_B (2:0) | LVTTL/CMOS Compatible Input: Bank B post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See “ <i>Post-Divide Frequency Select</i> ” table. FSEL_B0 = LSB.                                   |
| 56, 57, 58  | FSEL_A (2:0) | LVTTL/CMOS Compatible Input: Bank A post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See “ <i>Post-Divide Frequency Select</i> ” table. FSEL_A0 = LSB.                                   |
| 59          | OUT_SYNC     | Banks A, B, C Output Synchronous Control: (LVTTL/CMOS compatible). Internal 25kΩ pull-up. After any bank has been programmed, toggle with a HIGH-LOW-HIGH pulse to resynchronize all output banks.        |

**Input/Output**

| Pin Number     | Pin Name             | Pin Function  |
|----------------|----------------------|---|
| 1, 2, 3        | NC                   | No Connect: Leave floating.   |
| 10, 11         | XTAL2, XTAL1         | Crystal Input. Directly connect a series resonant crystal across inputs.  |
| 12             | VBB_REF              | Reference Output Voltage. Used for single-ended input. Maximum sink/source current = 0.5mA.   |
| 5, 6           | /EXT_VCO,<br>EXT_VCO | Differential “Any In” Compatible Input Pair. Allows for external VCO connection. The “Any In” input structure accepts many popular logic types. See “ <i>Input Interface for ExtVCO Pins</i> ” section for interface diagrams. Can leave unconnected if using internal VCO. |
| 51, 52, 53, 54 | QA1 to QA0           | Bank A 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_A (0:2). Terminate outputs with 50Ω to V <sub>CC</sub> -2V. See “ <i>Output Termination Recommendations</i> ” section.  |
| 32–49          | QB8 to QB0           | Bank B Output Drivers: Differential HSTL outputs. See “ <i>Output Termination Recommendations</i> ” section. Output frequency is controlled by FSEL_B (0:2).  |
| 17, 18, 19, 20 | QC1 to QC0           | Bank C 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_C (0:2). Terminate outputs with 50Ω to V <sub>CC</sub> -2V. See “ <i>Output Termination Recommendations</i> ” section.  |
| 64             | NC                   | No Connect: Leave floating.   |

### Absolute Maximum Ratings<sup>(Note 1)</sup>

|   |                               |
|---|-------------------------------|
| Supply Voltage ( $V_{IN}$ ) .....                       | -0.5V to +4.0V                |
| $V_{CC}$ Pin Potential to Ground Pin (All $V_{CC}$ ) .. | -0.5V to +4.0V                |
| Input Voltage (except XTAL 1,2 pins) ( $V_{IN}$ ) ...   | -0.5V to $V_{CCI}$            |
| XTAL 1, 2 Input Voltage ( $V_{XTAL\ 1,2}$ ) .....       | ( $V_{CC}-1.9V$ ) to $V_{CC}$ |
| DC Output Current ( $I_{OUT}$ )                         |                               |
| -LVPECL, HSTL outputs .....                             | -50mA                         |
| Lead Temperature (soldering, 20 sec.) .....             | 260°C                         |
| Storage Temperature ( $T_S$ ) .....                     | -65°C to +150°C               |

### Operating Ratings<sup>(Note 2)</sup>

|  |              |
|--|--------------|
| Supply Voltage                                     |              |
| $V_{CCO\ A}$ and $V_{CCO\ C}$ .....                | 3.0V to 3.6V |
| $V_{CCO\ B}$ .....                                 | 1.6V to 2.0V |
| Ambient Temperature ( $T_A$ ) .....                | 0°C to +85°C |
| Package Thermal Resistance (Junction-to-Ambient)   |              |
| With Die attach soldered to GND:                   |              |
| TQFP ( $\theta_{JA}$ ) Still-Air .....             | 23°C/W       |
| TQFP ( $\theta_{JA}$ ) 200lfpm .....               | 18°C/W       |
| TQFP ( $\theta_{JA}$ ) 500lfpm .....               | 15°C/W       |
| With Die attach NOT soldered to GND, <b>Note 3</b> |              |
| TQFP ( $\theta_{JA}$ ) Still-Air .....             | 44°C/W       |
| TQFP ( $\theta_{JA}$ ) 200lfpm .....               | 36°C/W       |
| TQFP ( $\theta_{JA}$ ) 500lfpm .....               | 30°C/W       |
| Package Thermal Resistance (Junction-to-Case)      |              |
| TQFP ( $\theta_{JC}$ ) .....                       | 4.3°C/W      |

## DC ELECTRICAL CHARACTERISTICS

### Power Supply

| Symbol                       | Parameter                             | Condition     | Min | Typ | Max | Units |
|------------------------------|---------------------------------------|---------------|-----|-----|-----|-------|
| $V_{CCA}$<br>$V_{CC\_Logic}$ | PLL and Logic Supply Voltage          | <b>Note 4</b> | 3.0 | 3.3 | 3.6 | V     |
| $V_{CCO\ A/C}$               | Bank A and C $V_{CC}$ Output          |               | 3.0 | 3.3 | 3.6 | V     |
| $V_{CCO\ B}$                 | Bank B $V_{CC}$ Output<br>LVPECL/HSTL |               | 1.6 | 1.8 | 2.0 | V     |
| $I_{CC}$                     | Total Supply Current                  | <b>Note 5</b> | —   | 230 | 295 | mA    |

**Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** It is recommended that the user always solder the exposed die pad to a ground plane for enhanced heat dissipation.

**Note 4.**  $V_{CCA}$ ,  $V_{CC\_LOGIC}$ ,  $V_{CCO\ A/C}$  are *not* internally connected together inside the device. They must be connected together on the PCB.  $V_{CCO\ B}$  is a separate supply.

**Note 5.** No load. Outputs floating, Banks A, B, and C enabled.

**DC ELECTRICAL CHARACTERISTICS****LVCMOS/LVTTL Input Control Logic** ( $V_{CCA}$ ,  $V_{CC\_LOGIC}$ ,  $V_{CCO A/C} = +3.3V \pm 10\%$ )

| Symbol   | Parameter          | Condition | Min | Typ | Max  | Units   |
|----------|--------------------|-----------|-----|-----|------|---------|
| $V_{IH}$ | Input HIGH Voltage |           | 2.0 | —   | —    | V       |
| $V_{IL}$ | Input LOW Voltage  |           | —   | —   | 0.8  | V       |
| $I_{IH}$ | Input HIGH Current |           | —   | —   | 150  | $\mu A$ |
| $I_{IL}$ | Input LOW Current  |           | —   | —   | -300 | $\mu A$ |

**ExtVCO (Pins 5, 6) INPUT** (All  $V_{CC}$  pins except  $V_{CCO B} = +3.3V \pm 10\%$ ,  $V_{CCO B} = +1.8V \pm 10\%$ )

| Symbol   | Parameter                  | Condition | Min  | Typ | Max            | Units |
|----------|----------------------------|-----------|------|-----|----------------|-------|
| $V_{ID}$ | Differential Input Voltage |           | 100  | —   | —              | mV    |
| $V_{IH}$ | Input HIGH Voltage         |           | —    | —   | $V_{CC} + 0.3$ | V     |
| $V_{IL}$ | Input LOW Voltage          |           | -0.3 | —   | —              | V     |

**100K LVPECL Output** (All  $V_{CC}$  pins except  $V_{CCO B} = +3.3V \pm 10\%$ ,  $V_{CCO B} = +1.8V \pm 10\%$ ) (Note 6)

| Symbol    | Parameter                | Condition | Min              | Typ              | Max              | Units |
|-----------|--------------------------|-----------|------------------|------------------|------------------|-------|
| $V_{OH}$  | Output HIGH Voltage      |           | $V_{CC} - 1.145$ | $V_{CC} - 1.020$ | $V_{CC} - 0.895$ | V     |
| $V_{OL}$  | Output LOW Voltage       |           | $V_{CC} - 1.945$ | $V_{CC} - 1.820$ | $V_{CC} - 1.695$ | V     |
| $V_{BB}$  | Output Reference Voltage |           | $V_{CC} - 1.325$ | $V_{CC} - 1.425$ | $V_{CC} - 1.525$ | V     |
| $V_{OUT}$ | Output Voltage Swing     |           | —                | 800              | —                | mV    |

**HSTL Output (Bank B QB0:8)** (All  $V_{CC}$  pins except  $V_{CCO B} = +3.3V \pm 10\%$ ,  $V_{CCO B} = +1.8V \pm 10\%$ ) (Note 7)

| Symbol    | Parameter            | Condition | Min | Typ | Max | Units |
|-----------|----------------------|-----------|-----|-----|-----|-------|
| $V_{OUT}$ | Output Voltage Swing |           | —   | 800 | —   | mV    |
| $V_{OH}$  | Output HIGH Voltage  |           | 1.0 | —   | 1.2 | V     |
| $V_{OL}$  | Output LOW Voltage   |           | 0.2 | —   | 0.4 | V     |

**Note 6.** All LVPECL outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$ .**Note 7.** All HSTL outputs loaded with  $50\Omega$  to GND.

**AC ELECTRICAL CHARACTERISTICS**

$$V_{CC\_LOGIC} = V_{CCA} = V_{CCO\ A/C} = +3.3V \pm 10\%, V_{CCO\ B} = +1.8V \pm 10\%$$

| Symbol                          | Parameter   | Condition                        | Min      | Typ        | Max        | Units              |
|---------------------------------|---|----------------------------------|----------|------------|------------|--------------------|
| f <sub>IN</sub>                 | Xtal Input Frequency Range                                  | <b>Note 8</b>                    | 14       | —          | 18         | MHz                |
| f <sub>OUT</sub>                | Output Frequency Range                                      | w/Internal VCO                   | 33.33    | —          | 500        | MHz                |
|                                 |   | w/External VCO                   | —        | —          | 622.08     | MHz                |
| f <sub>VCO</sub>                | Internal VCO Frequency Range                                |                                  | 600      | —          | 1000       | MHz                |
|                                 | External VCO Frequency                                      |                                  | —        | —          | 1250       | MHz                |
| t <sub>skew</sub>               | Within Device Skew  |                                  | —        | —          | 50         | ps                 |
|                                 | <b>Note 9</b><br>Within-Bank PECL                           |                                  | —        | —          | 50         | ps                 |
|                                 | Within-Bank HSTL  |                                  | —        | —          | 75         | ps                 |
|                                 | Between Banks   |                                  | —        | —          | 150        | ps                 |
|                                 | Part-to-Part Skew   | <b>Note 10</b>                   | —        | —          | 200        | ps                 |
| t <sub>LOCK</sub>               | Maximum PLL Lock Time                                       |                                  | —        | —          | 10         | ms                 |
| t <sub>JITTER</sub>             | Cycle-to-Cycle Jitter (Pk-to-Pk)                            | <b>Note 11</b>                   | —        | 25         | —          | ps                 |
|                                 | Period Jitter (RMS)   | <b>Note 12</b>                   | —        | —          | 50         | ps                 |
| t <sub>pw</sub> (min)           | Minimum Pulse Width   |                                  | 50       | —          | —          | ns                 |
|                                 | Target PLL Loop Bandwidth                                   |                                  | —        | —          | —          | —                  |
|                                 | Feedback Divider Ratio: 72<br>Feedback Divider Ratio: 34    | <b>Note 13</b><br><b>Note 13</b> | —        | 1.0<br>2.0 | —          | MHz<br>MHz         |
| t <sub>DC</sub>                 | f <sub>OUT</sub> Duty Cycle                                 |                                  | 45       | 50         | 55         | %                  |
| t <sub>r</sub> , t <sub>f</sub> | Output Rise/Fall Time<br>(20% to 80%)LVPECL_Out<br>HSTL_Out |                                  | —<br>100 | 250<br>—   | 450<br>450 | ps<br>ps           |
|                                 |   | <b>Note 14</b>                   | —        | —          | 10         | ns                 |
| t <sub>OUTPUT_RESET</sub>       |   |                                  | 5        | —          | —          | ns                 |
| t <sub>HOLD_FSEL</sub>          |   |                                  | 5        | —          | —          | ns                 |
| t <sub>SETUP_FSEL</sub>         |   |                                  | 1        | —          | —          | VCO<br>clock cycle |
| t <sub>OUTPUT_SYNC</sub>        |   |                                  | —        | —          | 1          | μs                 |
| t <sub>SETUP_OUT_SYNC</sub>     |   |                                  | 500      | —          | —          | ps                 |

**Note 8.** Fundamental mode crystal.

**Note 9.** The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.

**Note 10.** The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.

**Note 11.** Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs.  $T_{JITTER\_CC} = T_n - T_{n+1}$  where T is the time between rising edges of the output signal.

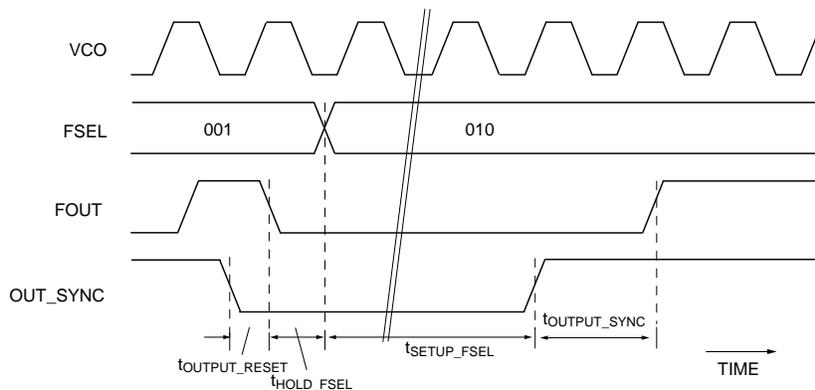
**Note 12.** Period Jitter definition: For a specified amount of time (i.e., 1ms), there are N periods of a signal, and  $T_n$  is defined as the average period of that signal. Period jitter is defined as the variation in the period of the output signal for corresponding edges relative to  $T_n$ .

**Note 13.** Using recommended loop filter components. See "Functional Description, External Loop Filter Considerations."

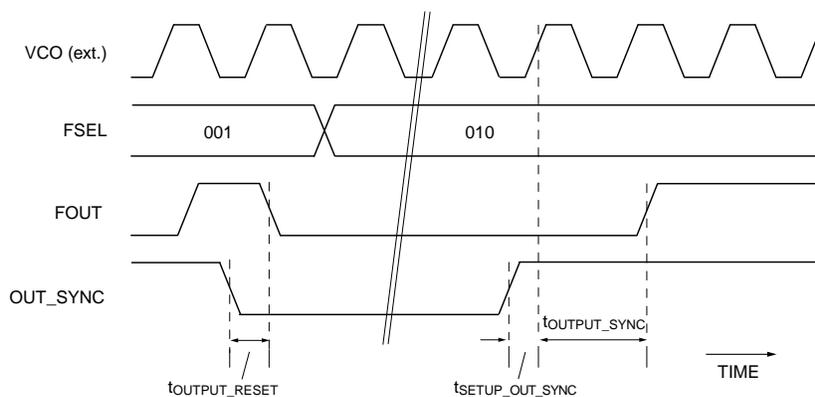
**Note 14.** See "Timing Diagrams."

**TIMING DIAGRAMS**

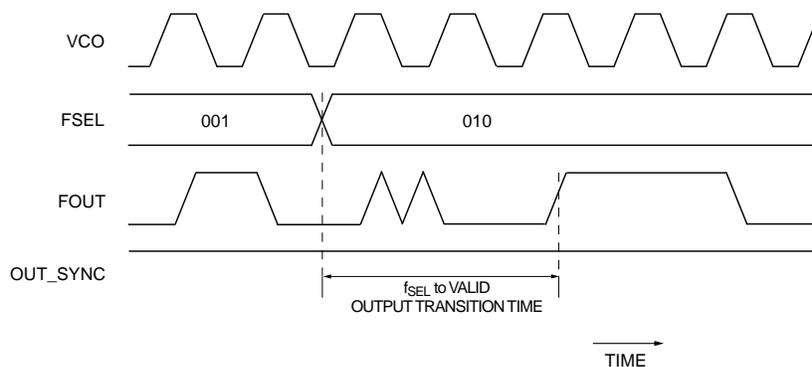
Conditions: Internal VCO, unless otherwise stated.



**Frequency Programming (Internal VCO Clock)**



**Frequency Programming (External VCO Clock)**



**Output Frequency Update to Valid Output**



**FUNCTIONAL DESCRIPTION**

At the core of the SY89531L clock synthesizer is a precision PLL driven by 14MHz to 18MHz series resonant crystal. For users who wish to supply a TTL or LVPECL clock input, please use the SY89536L. The PLL output is sent to three banks of outputs. Each bank has its own programmable frequency divider, and the design is optimized to provide very low skew between banks, and very low jitter.

**PLL Programming and Operation**

**IMPORTANT:** If the internal VCO will be used, VCO\_SEL **must** be tied LOW, and ExtVCO pins can be left unconnected.

The internal VCO range is 600MHz to 1000MHz, and the feedback ratio is selectable via the MSEL divider control (M3:0 pins). The VCO\_SEL pin must be tied low. The feedback ratio can be changed without powering the chip down. The PLL output is fed to three banks of outputs: Bank A, Bank B, and Bank C. Banks A and C each have two differential LVPECL output pairs. Bank B has nine differential HSTL output pairs.

Each bank has a separate frequency divider circuit that can be reprogrammed on the fly. The FSEL\_x0:2 (where x is A, B, or C) pins control the divider value. The FSEL divider can be programmed in ratios from 2 to 18, and the outputs of Banks A, B, and C can be synchronized after programming by pulsing the OUT\_SYNC pin HIGH-LOW-HIGH. Setting a value of 000 for FSEL is an output disable forcing the Q outputs to be LOW and the /Q outputs to be HIGH. Doing so will decrease power consumption by approximately 5mA per bank.

To determine the correct settings for the SY89531L follow these steps:

1. Refer to the *“Suggested Selections for Specific Customer Applications”* section for common applications, as well as the formula used to compute the output frequency.
2. Determine the desired output frequency, such as 66MHz.
3. Choose a crystal frequency between 14MHz and 18MHz. In this example, we choose 18MHz for the crystal frequency. This results in an input/output ratio of 66/18.
4. Refer to the *“Feedback Divide Select”* table and the *“Post-Divide Frequency Select”* table to find values for MSEL and FSEL such that MSEL/FSEL equals the same 66/18 ratio. In this example, values of MSEL=44 and FSEL=12 work.
5. Make sure that XTAL (the crystal frequency) multiplied by MSEL is between 600MHz and 1000MHz.

The user may need to experiment with different crystal frequencies to satisfy these requirements.

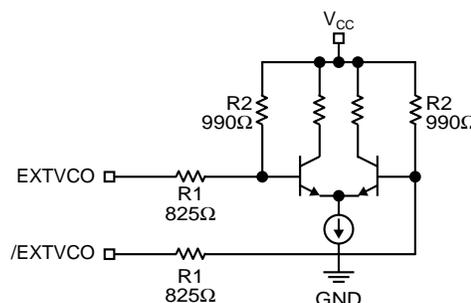
**ExtVCO Input Interface**

The flexible ExtVCO inputs are designed to accept any differential or single-ended input signal within 300mV above V<sub>CC</sub> and 300mV below ground.

Do not leave unused ExtVCO inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating.

**Input Levels**

LVDS, CML and HSTL differential signals may be connected directly to the ExtVCO inputs. Depending on the actual worst case voltage seen, the minimum input voltage swing varies.



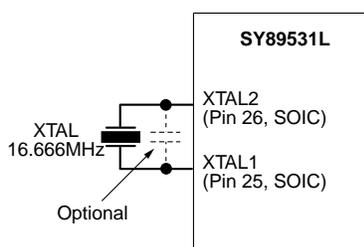
**Figure 1. Simplified Input Structure**

### Crystal Input and Oscillator Interface

The SY89531L features a fully integrated on-board oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design, and thus, a series-resonant crystal is preferred, but not required.

A parallel-resonant crystal can be used with the SY89531L with only a minor error in the desired frequency. A parallel-resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified; a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the SY89531L as possible to avoid any board level parasitics. In addition, trace lengths should be matched. Figure 2 shows how to interface with a crystal. Table 1 illustrates the crystal specifications. Certain crystals may require a 10pF capacitor across XTAL1 and XTAL2 for proper operation. This is normally not required, but it is recommended that provisions be made for it.



Quartz Crystal Selection:  
(1) Raltron Series Resonant: AS-16.666-S-SMD-T-MI  
(2) Raltron Parallel Resonant: AS-16.666-18-SMD-T-MI

Figure 2. Crystal Interface

### External Loop Filter Considerations

The SY89531L features an external PLL loop filter that allows the user to tailor the PLL's behavior to their application and operating environment. We recommend using ceramic capacitors with NPO or X7R dielectric, as they have very-low effective series resistance. For applications that require ultra-low cycle-to-cycle jitter, use the components shown in Figure 3. The PLL loop bandwidth is a function of feedback divider ratio, and the external loop filter allows the user to compensate. For instance, the PLL's loop bandwidth can be decreased by using a smaller resistor in the loop filter. This results in less noise from the PLL input, but potentially more noise from the VCO. Refer to "AC Electrical Characteristics" for target PLL loop bandwidth. The designer should take care to keep the loop filter components on the same side of the board and as close as possible to the SY89531L's LOOP\_REF and LOOP\_FILTER pins. To insure minimal noise pick up on the loop filter, it is desirable to cut away the ground plane directly underneath the loop filter component pads and traces. However, the benefit may not be significant in all applications and one must be careful to not alter the characteristic impedance of nearby traces.

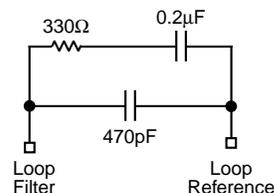


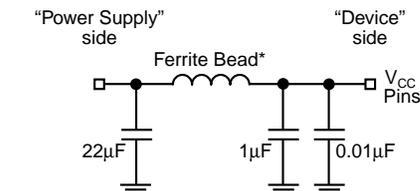
Figure 3. External Loop Filter Connection

| Output Frequency: 14MHz-18MHz        |     |                |      |      |
|--------------------------------------|-----|----------------|------|------|
| Mode of Oscillation: Fundamental     |     |                |      |      |
|                                      | Min | Typ            | Max  | Unit |
| Frequency Tolerance @25°C            | —   | ±30            | ±50  | ppm  |
| Frequency Stability over 0°C to 70°C | —   | ±50            | ±100 | ppm  |
| Operating Temperature Range          | -20 | —              | +70  | °C   |
| Storage Temperature Range            | -55 | —              | +125 | °C   |
| Aging (per yr/first 3 yrs)           | —   | —              | ±5   | ppm  |
| Load Capacitance                     | —   | 18 (or series) | —    | pF   |
| Equivalent Series Resistance (ESR)   | —   | —              | 50   | Ω    |
| Drive Level                          | —   | 100            | —    | µW   |

Table 1. Quartz Crystal Oscillator Specifications

**Power Supply Filtering Techniques**

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum,  $V_{CCA}$ ,  $V_{CC\_Logic}$ , and all  $V_{CCO}$  pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 4.



\*For  $V_{CC\_Analog}$ ,  $V_{CC\_TTL}$ ,  $V_{CC1}$ , use ferrite bead = 200mA, 0.45Ω DC, Murata P/N BLM21A1025

\*For  $V_{CC\_OUT}$  use ferrite bead = 3A, 0.025Ω DC, Murata, P/N BLM31P005

\*Component size: 0805

**Figure 4. Power Supply Filtering**

**Output Logic Characteristics**

See “Output Termination Recommendations” for illustrations. In cases where single-ended output is desired, the designer should terminate the unused complimentary

output in the same manner as the normal output that is begin used. Unused output pairs can be left floating. Unused output banks can be switched off by tying the appropriate FSEL pins to ground. Unused output pairs that are in a bank that is disabled can be left floating, regardless of output driver type.

LVPECL operation:

- Typical voltage swing is 700mV<sub>PP</sub> to 800mV<sub>PP</sub> into 50Ω.
- Common mode voltage is  $V_{CC}-1.3V$ , typical.
- 100Ω termination across the output pair is NOT recommended for LVPECL.

HSTL operation (Bank B):

- Typical voltage swing is 250mV<sub>PP</sub> to 450mV<sub>PP</sub> into effective 50Ω.

**Thermal Considerations**

This part has an exposed die pad for enhanced heat dissipation. We strongly recommend soldering the exposed pad to a ground plane. Where this is not possible, we recommend maintaining at least 500lfpm air flow.

For additional information on exposed-pad characteristics and implementation details, see Amkor Technology’s write-up at [www.amkor.com](http://www.amkor.com).

**POST-DIVIDE FREQUENCY SELECT TABLE (FSEL)**

| FSEL_A2 <sup>(1)</sup> (MSB) | FSEL_A1 <sup>(1)</sup> | FSEL_A0 <sup>(1)</sup> (LSB) | Output Divider   |
|------------------------------|------------------------|------------------------------|--|
| 0                            | 0                      | 0                            | Output Disable Function, all outputs: Q = LOW, /Q = HIGH |
| 0                            | 0                      | 1                            | VCO ÷ 2  |
| 0                            | 1                      | 0                            | VCO ÷ 4  |
| 0                            | 1                      | 1                            | VCO ÷ 6  |
| 1                            | 0                      | 0                            | VCO ÷ 8  |
| 1                            | 0                      | 1                            | VCO ÷ 10   |
| 1                            | 1                      | 0                            | VCO ÷ 12   |
| 1                            | 1                      | 1                            | VCO ÷ 18   |

**Note 1.** Same dividers apply to FSEL\_B (0:2) and FSEL\_C (0:2).

**FEEDBACK DIVIDE SELECT TABLE (MSEL)**

| M3 | M2 | M1 | M0 | VCO Frequency <sup>(1)</sup> |
|----|----|----|----|------------------------------|
| 0  | 0  | 0  | 0  | Ref × 34                     |
| 0  | 0  | 0  | 1  | Ref × 36                     |
| 0  | 0  | 1  | 0  | Ref × 38                     |
| 0  | 0  | 1  | 1  | Ref × 40                     |
| 0  | 1  | 0  | 0  | Ref × 42                     |
| 0  | 1  | 0  | 1  | Ref × 44                     |
| 0  | 1  | 1  | 0  | Ref × 48                     |
| 0  | 1  | 1  | 1  | Ref × 50                     |
| 1  | 0  | 0  | 0  | Ref × 52                     |
| 1  | 0  | 0  | 1  | Ref × 54                     |
| 1  | 0  | 1  | 0  | Ref × 56                     |
| 1  | 0  | 1  | 1  | Ref × 60                     |
| 1  | 1  | 0  | 0  | Ref × 62                     |
| 1  | 1  | 0  | 1  | Ref × 66                     |
| 1  | 1  | 1  | 0  | Ref × 70                     |
| 1  | 1  | 1  | 1  | Ref × 72                     |

**Note 1.** Ref = Crystal Frequency.

**SUGGESTED SELECTIONS FOR SPECIFIC CUSTOMER APPLICATIONS<sup>(Notes 1, 2)</sup>**

| Protocol      | Rate (MHz) | FSEL (Post Divider) | MSEL (Feedback Div.) | XTAL (MHz) | FOUT |
|---------------|------------|---------------------|----------------------|------------|------|
| PCI           | 33         | 18                  | 36                   | 16.67      | 33   |
| Fast Ethernet | 100        | 6                   | 40                   | 15         | 100  |
| 1/8 FC        | 133        | 6                   | 52                   | 15.36      | 133  |
| ESCON         | 200        | 4                   | 50                   | 16         | 200  |

$$FOUT = \frac{(XTAL \times MSEL)}{FSEL}$$

**Note 1.** 600MHz < (XTAL x MSEL) < 1000MHz.

**Note 2.** Where two settings provide the user with the identical desired frequency, the setting with the higher input reference frequency (and lower feedback divider) will usually have lower output jitter. However, the reference input frequency, as well as the VCO frequency, must be kept within their respective ranges.

**INPUT INTERFACE FOR EXTVCO PINS**

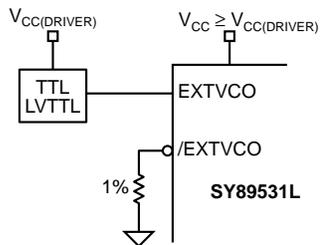


Figure 5a. 3.3V "TTL"

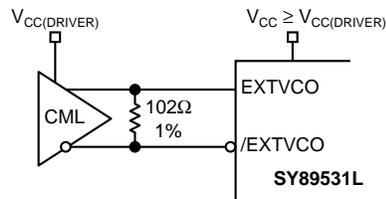


Figure 5b. CML DC-Coupled

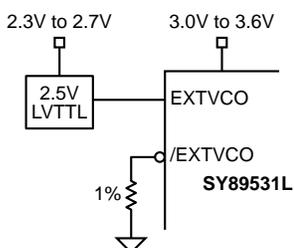


Figure 5c. 2.5V "LVTTTL"

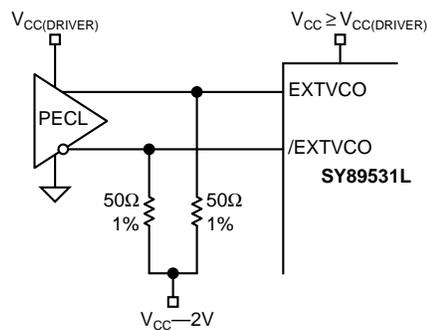


Figure 5d. 3.3V LVPECL DC-Coupled

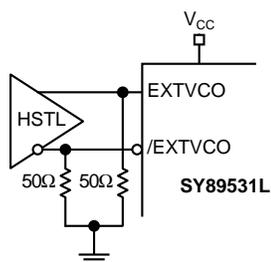


Figure 5e. HSTL

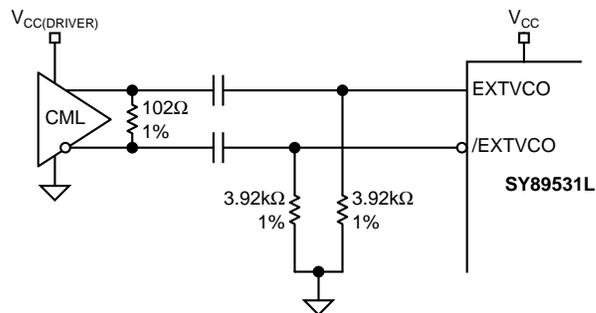


Figure 5f. CML AC-Coupled (Short Trace Lengths)

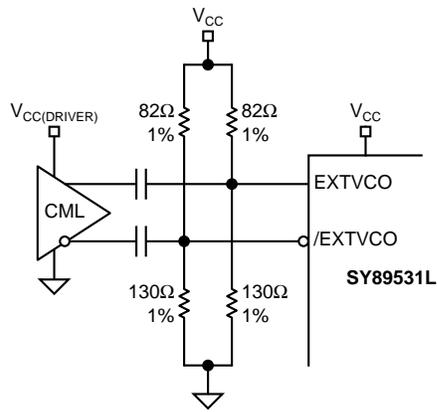


Figure 5g. CML AC-Coupled (Long Trace Lengths)

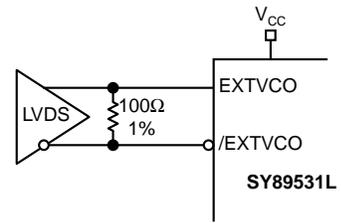
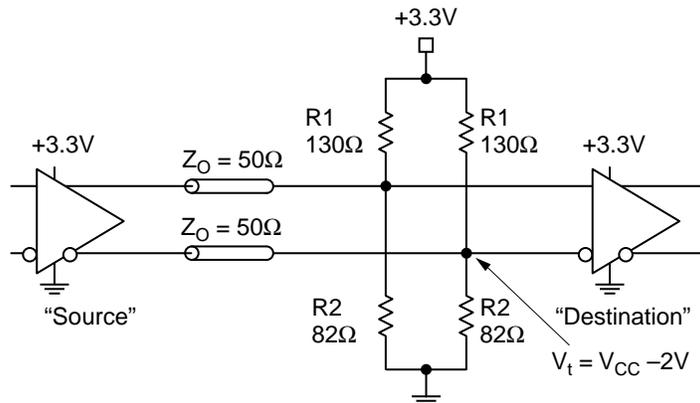
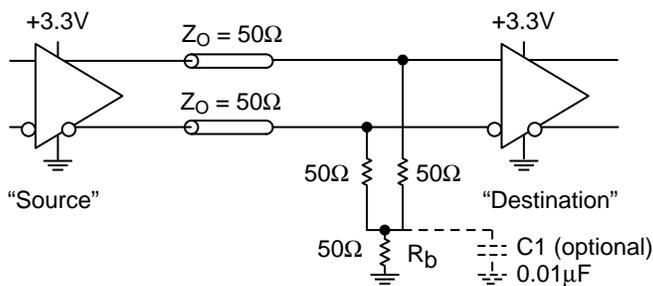


Figure 5h. LVDS

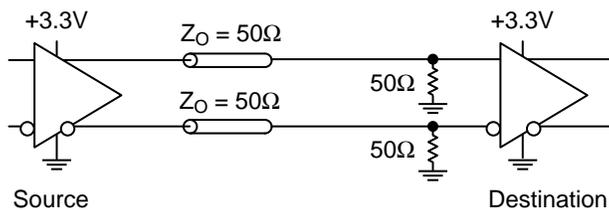
**OUTPUT TERMINATION RECOMMENDATIONS**



**Figure 6. PECL Parallel Termination Thevenin Equivalent (Note 1)**



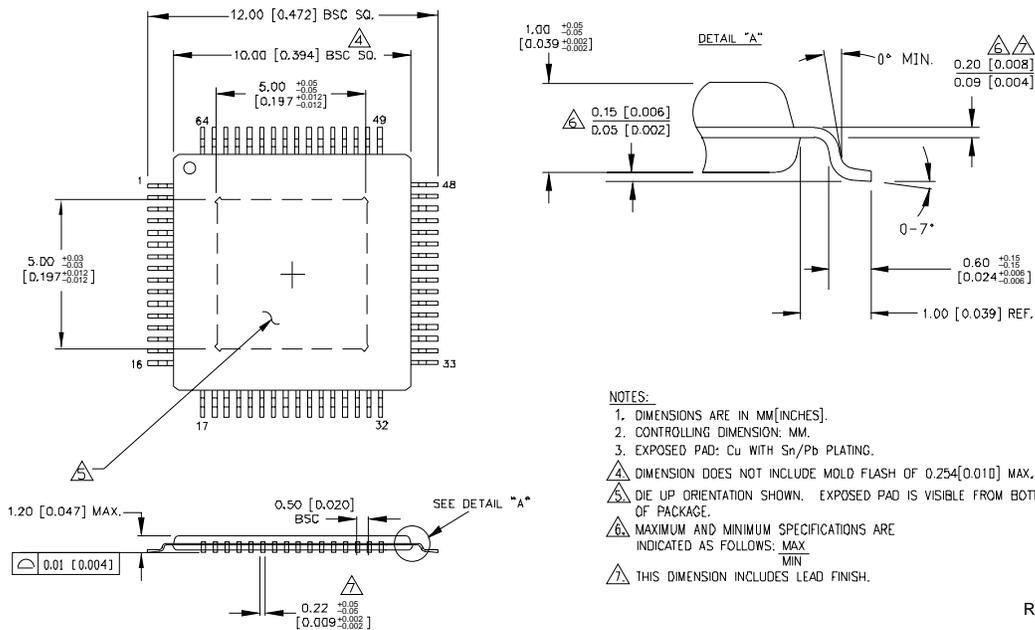
**Figure 7. LVPECL Three-Resistor "Y-Termination" (Notes 1, 2, 3)**



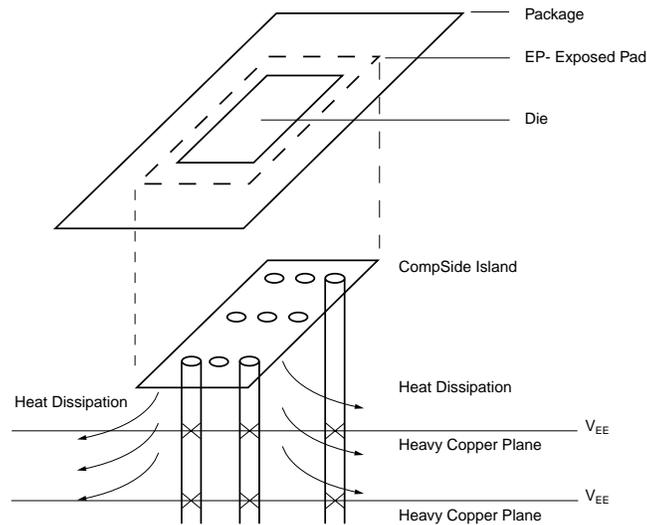
**Figure 8. HSTL Differential Termination (Note 1)**

- Note 1.** Place termination resistors as close to destination inputs as possible.
- Note 2.** PECL Y-termination is a power-saving alternative to Thevenin termination.
- Note 3.**  $R_b$  resistor sets the DC bias voltage, equal to  $V_t$ . For +3.3V systems  $R_b = 46\Omega$  to  $50\Omega$ .

**64-PIN EPAD-TQFP (DIE UP) (H64-1)**



Rev. 02



**PCB Thermal Consideration for 64-Pin EPAD-TQFP Package**

**Package Notes:**

- Note 1.** Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.
- Note 2.** Exposed pads must be soldered to a ground for proper thermal management.

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