

# NTGS3447P

## Power MOSFET

-12 V, -5.3 A, Single P-Channel, TSOP-6

### Features

- Low  $R_{DS(on)}$  in TSOP-6 Package
- 1.8 V Gate Rating
- This is a Pb-Free Device

### Applications

- Battery Switch and Load Management Applications in Portable Equipment
- High Side Load Switch
- PA Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	-12	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8$	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	-4.7	A
			$T_A = 85^\circ\text{C}$	-3.4	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-5.3		
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	1.25	W
	$t \leq 5 \text{ s}$		1.6		
Continuous Drain Current (Note 2)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	-3.4	A
			$T_A = 85^\circ\text{C}$	-2.5	
Power Dissipation (Note 2)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	0.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	-19	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size.

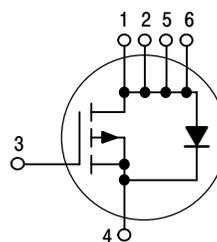


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-12 V	40 m $\Omega$ @ -4.5 V	-4.7 A
	53 m $\Omega$ @ -2.5 V	-4.1 A
	72 m $\Omega$ @ -1.8 V	-2.0 A

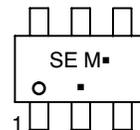
### P-Channel



### MARKING DIAGRAM

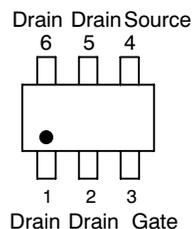


TSOP-6  
CASE 318G  
STYLE 1



SE = Device Code  
M = Date Code  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
NTGS3447PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	78	
Junction-to-Ambient – Minimum Pad (Note 4)	$R_{\theta JA}$	188	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)  
 4. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ $\mu\text{A}$	-12			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = -12$ V	$T_J = 25^\circ\text{C}$		-1.0	$\mu\text{A}$
			$T_J = 85^\circ\text{C}$		-5.0	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			$\pm 0.1$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = -250$ $\mu\text{A}$	-0.45		-1.0	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -4.7$ A		30	40	m $\Omega$
		$V_{GS} = -2.5$ V, $I_D = -4.1$ A		40	53	
		$V_{GS} = -1.8$ V, $I_D = -2.0$ A		53	72	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5$ V, $I_D = -4.7$ A		12		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -6$ V		1053		pF
Output Capacitance	$C_{OSS}$			254		
Reverse Transfer Capacitance	$C_{RSS}$			129		
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = -4.5$ V, $V_{DS} = -6$ V; $I_D = -4.7$ A		10.4	15	nC
Threshold Gate Charge	$Q_G(TH)$			1.0		
Gate-to-Source Charge	$Q_{GS}$			1.7		
Gate-to-Drain Charge	$Q_{GD}$			0.4		

### SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DS} = -6$ V, $I_D = -1.0$ A, $R_G = 6.0$ $\Omega$		7	11	ns
Rise Time	$t_r$			14	22	
Turn-Off Delay Time	$t_{d(OFF)}$			78	117	
Fall Time	$t_f$			47	71	

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0$ V, $I_S = -1.7$ A	$T_J = 25^\circ\text{C}$		-0.7	-1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0$ V, $dI_{SD}/dt = 100$ A/ $\mu\text{s}$ , $I_S = -1.7$ A			33	66	ns

5. Pulse Test: pulse width  $\leq 300$   $\mu\text{s}$ , duty cycle  $\leq 2\%$   
 6. Switching characteristics are independent of operating junction temperatures

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

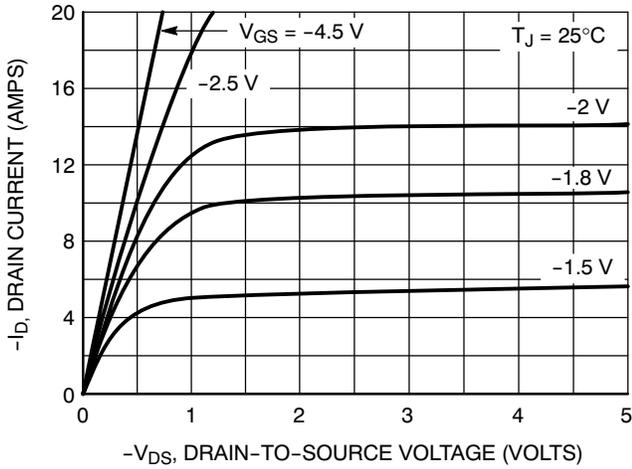


Figure 1. On-Region Characteristics

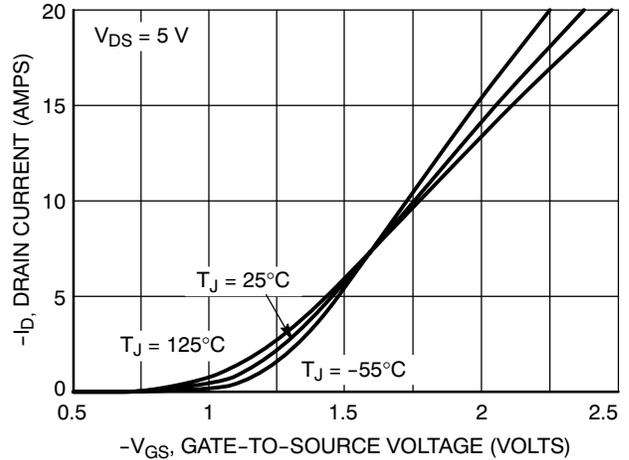


Figure 2. Transfer Characteristics

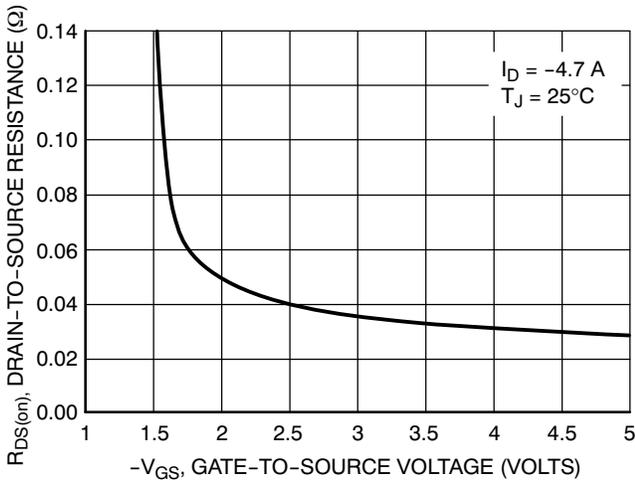


Figure 3. On-Resistance vs. Gate-to-Source Voltage

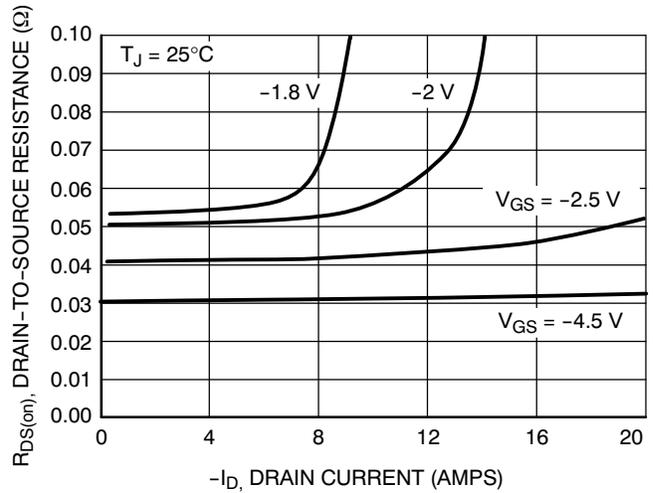


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

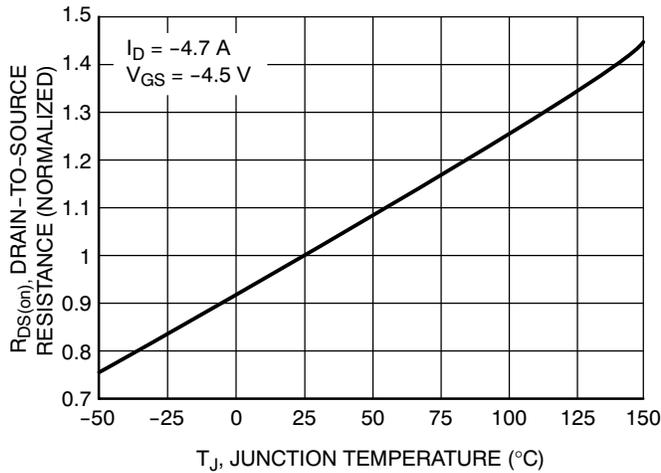


Figure 5. On-Resistance Variation with Temperature

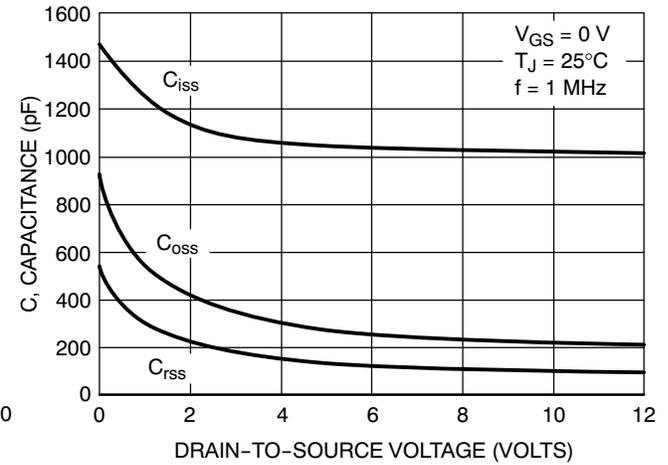
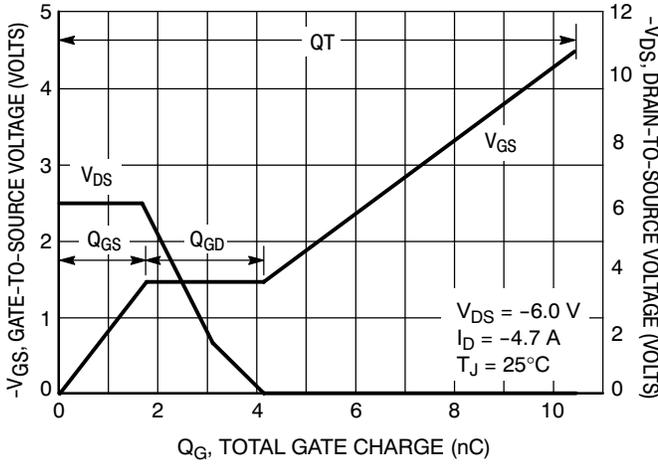


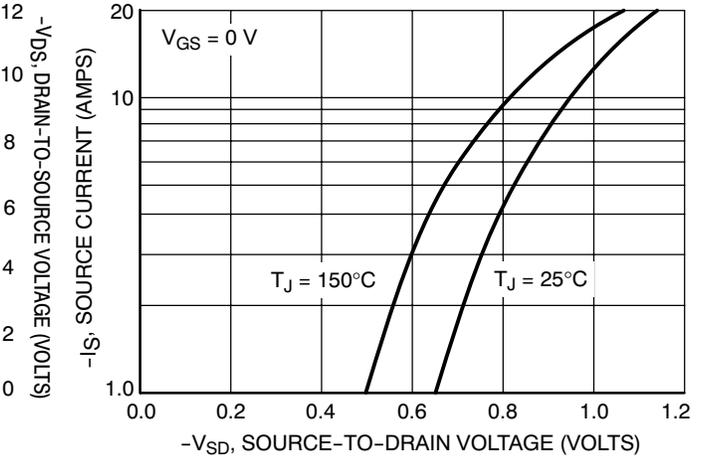
Figure 6. Capacitance Variation

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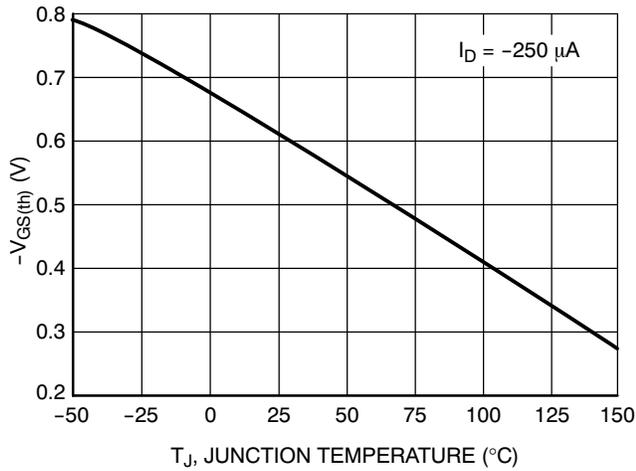
## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)



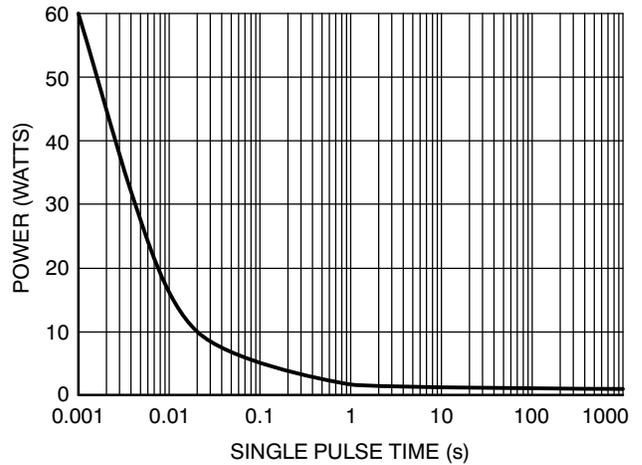
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



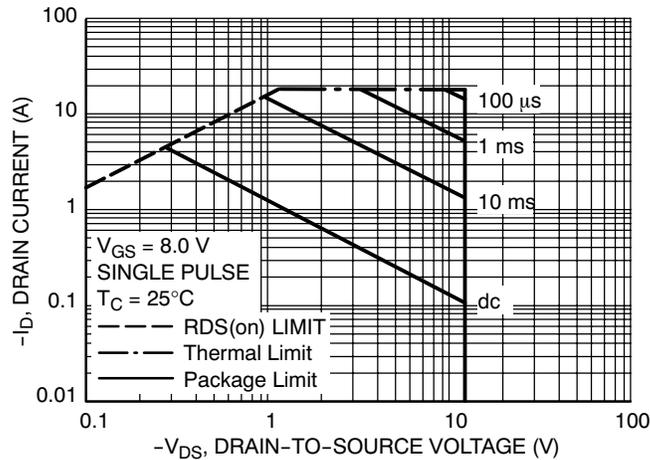
**Figure 8. Diode Forward Voltage vs. Current**



**Figure 9. Threshold Voltage**



**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

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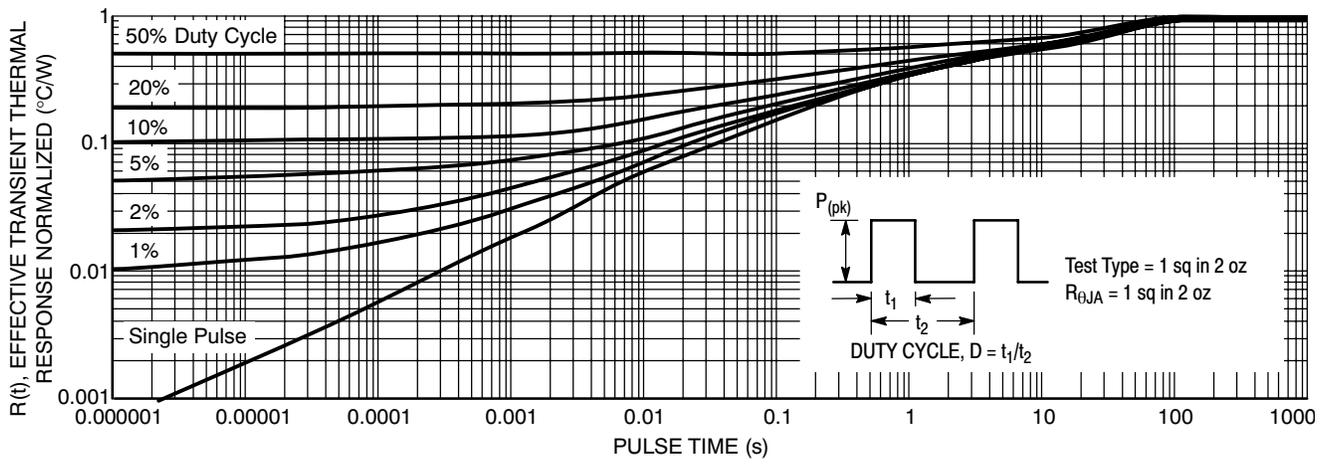
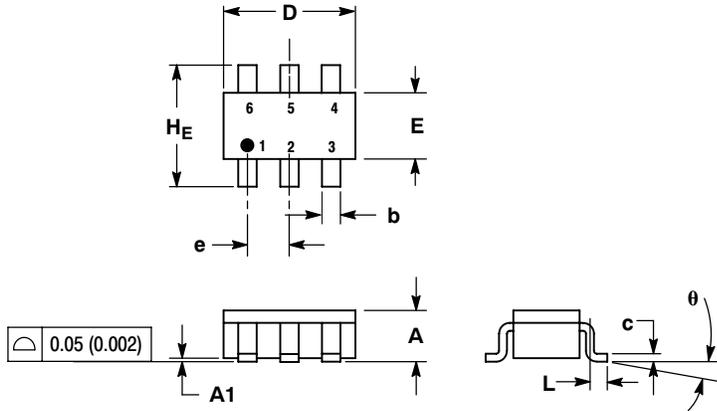


Figure 12. FET Thermal Response

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## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE S



#### NOTES:

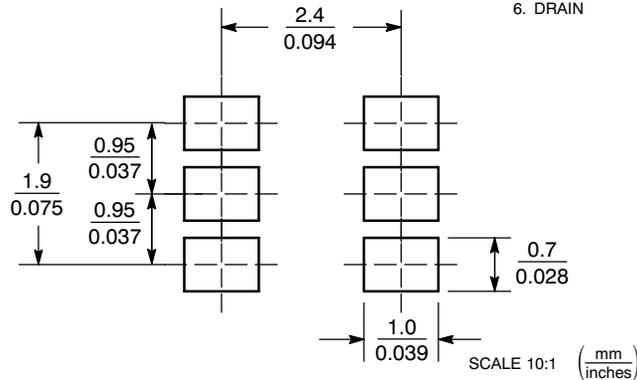
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

#### STYLE 1:

- PIN 1. DRAIN
- DRAIN
- GATE
- SOURCE
- DRAIN
- DRAIN

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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