

Handset-only

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Typical Application Schematic	16
3. Bill of Materials	17
4. Functional Description	18
4.1. Overview	18
4.2. Operating Modes	18
4.3. FM Receiver	19
4.4. AM Receiver	19
4.5. Digital Audio Interface	19
4.6. Stereo Audio Processing	21
4.7. Received Signal Qualifiers	21
4.8. De-emphasis	21
4.9. Volume Control	21
4.10. Stereo DAC	21
4.11. Soft Mute	21
4.12. FM Hi-Cut Control	22
4.13. RDS/RBDS Processor (Si4731 Only)	22
4.14. Tuning	22
4.15. Seek	22
4.16. Reference Clock	22
4.17. Control Interface	23
4.18. GPO Outputs	24
4.19. Firmware Upgrades	24
4.20. Reset, Powerup, and Powerdown	24
4.21. Programming with Commands	24
5. Pin Descriptions: Si4730/31-GM	25
6. Ordering Guide	26
7. Package Markings (Top Marks)	27
7.1. Si4730/31 Top Mark	27
7.2. Top Mark Explanation	27
8. Package Outline: Si4730/31	28
9. PCB Land Pattern: Si4730/31	29
10. Additional Reference Resources	31
Document Change List:	32
Contact Information	34

Si4730/31-D50

1. Electrical Specifications

Table 1. Recommended Operating Conditions*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Voltage	V_A		2.7	—	5.5	V
Digital and I/O Supply Voltage	V_D		1.62	—	3.6	V
Analog Power Supply Powerup Rise Time	V_{ARISE}		10	—	—	μ s
Digital Power Supply Powerup Rise Time	V_{DRISE}		10	—	—	μ s
Ambient Temperature	T_A		-20	25	85	$^{\circ}$ C

*Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at $V_A = 3.3$ V and 25 $^{\circ}$ C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings^{1,2}

Parameter	Symbol	Value	Unit
Analog Supply Voltage	V_A	-0.5 to 5.8	V
Digital and I/O Supply Voltage	V_D	-0.5 to 3.9	V
Input Current ³	I_{IN}	10	mA
Input Voltage ³	V_{IN}	-0.3 to ($V_{IO} + 0.3$)	V
Operating Temperature	T_{OP}	-40 to 95	$^{\circ}$ C
Storage Temperature	T_{STG}	-55 to 150	$^{\circ}$ C
RF Input Level ⁴		0.4	V_{pK}

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4730/31 device is a high-performance RF integrated circuit with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins DFS, SCLK, SEN, SDIO, RST, RCLK, GPO1, GPO2, GPO3, and DCLK.
4. At RF input pins FMI and AMI.

Table 3. DC Characteristics(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
V _A Supply Current	I _{FMVA}		—	7.5	9.7	mA
V _D Supply Current	I _{FMVD}	Digital Output Mode ¹	—	8.5	11.1	mA
V _D Supply Current	I _{FMVD}	Analog Output Mode	—	8.4	11.1	mA
AM Mode						
V _A Supply Current	I _{AMVA}		—	7.5	8.5	mA
V _D Supply Current	I _{AMVD}	Digital Output Mode ¹	—	8.5	11.0	mA
V _D Supply Current	I _{AMVD}	Analog Output Mode	—	8.0	10.2	mA
Powerdown and Interface						
V _A Powerdown Current	I _{APD}		—	4	15	μA
V _D Powerdown Current	I _{DOPD}	SCLK, RCLK inactive	—	3	10	μA
High Level Input Voltage ²	V _{IH}		0.7 × V _D	—	V _D + 0.3	V
Low Level Input Voltage ²	V _{IL}		-0.3	—	0.3 × V _D	V
High Level Input Current ²	I _{IH}	V _{IN} = V _D = 3.6 V	-10	—	10	μA
Low Level Input Current ²	I _{IL}	V _{IN} = 0 V, V _D = 3.6 V	-10	—	10	μA
High Level Output Voltage ³	V _{OH}	I _{OUT} = 500 μA	0.8 × V _D	—	—	V
Low Level Output Voltage ³	V _{OL}	I _{OUT} = -500 μA	—	—	0.2 × V _D	V
Notes:						
1. Guaranteed by characterization.						
2. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.						
3. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.						

Si4730/31-D50

Table 4. Reset Timing Characteristics^{1,2,3}

($V_A = 2.7$ to 5.5 V, $V_D = 1.62$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RST}}$ Pulse Width and GPO1, GPO2/ $\overline{\text{INT}}$ Setup to $\overline{\text{RST}}\uparrow^4$	t_{SRST}	100	—	—	μs
GPO1, GPO2/ $\overline{\text{INT}}$ Hold from $\overline{\text{RST}}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$, and stays high until after the first start condition.
3. When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 μs , to provide time for on-chip 1 M Ω devices (active while $\overline{\text{RST}}$ is low) to pull GPO1 high and GPO2 low.

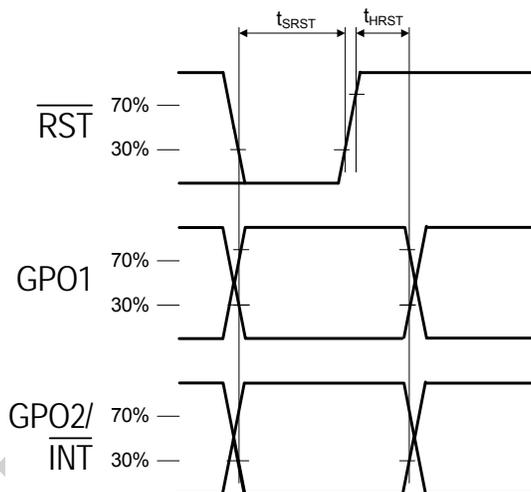


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics^{1,2,3}(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f _{SCL}		0	—	400	kHz
SCLK Low Time	t _{LOW}		1.3	—	—	μs
SCLK High Time	t _{HIGH}		0.6	—	—	μs
SCLK Input to SDIO ↓ Setup (START)	t _{SU:STA}		0.6	—	—	μs
SCLK Input to SDIO ↓ Hold (START)	t _{HD:STA}		0.6	—	—	μs
SDIO Input to SCLK ↑ Setup	t _{SU:DAT}		100	—	—	ns
SDIO Input to SCLK ↓ Hold ^{4,5}	t _{HD:DAT}		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	t _{SU:STO}		0.6	—	—	μs
STOP to START Time	t _{BUF}		1.3	—	—	μs
SDIO Output Fall Time	t _{f:OUT}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	t _{f:IN} t _{r:IN}		$20 + 0.1 \frac{C_b}{1\text{pF}}$	—	300	ns
SCLK, SDIO Capacitive Loading	C _b		—	—	50	pF
Input Filter Pulse Suppression	t _{SP}		—	—	50	ns

Notes:

1. When V_D = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$, and stays high until after the first start condition.
4. The Si4730/31 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum t_{HD:DAT} specification.
5. The maximum t_{HD:DAT} has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, t_{HD:DAT} may be violated as long as all other timing parameters are met.

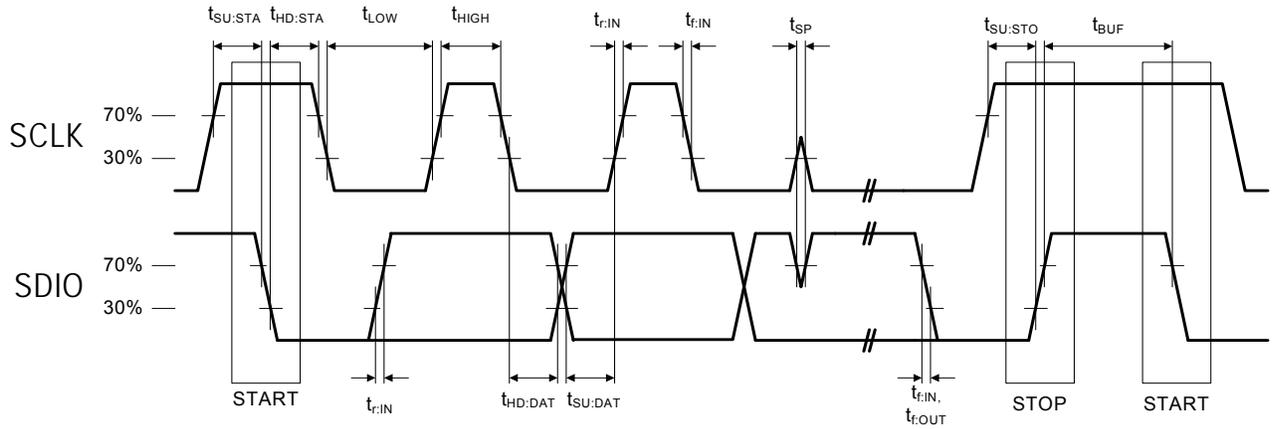


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

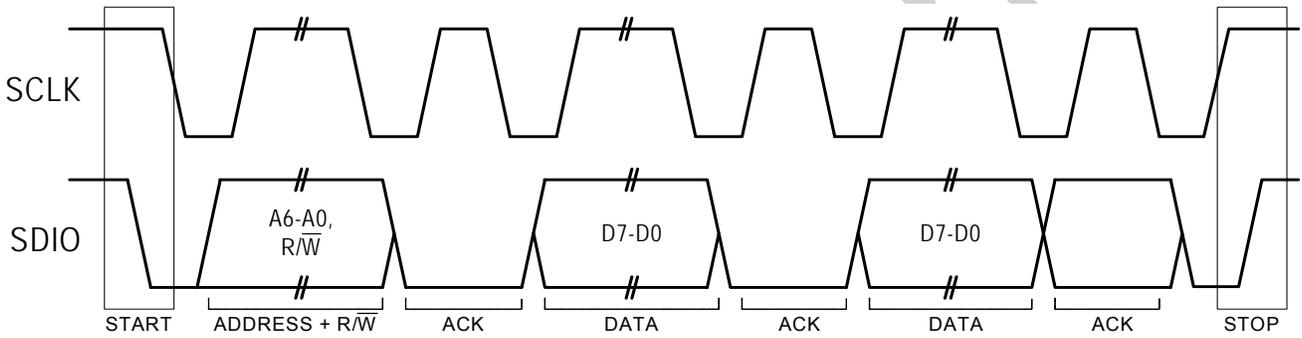
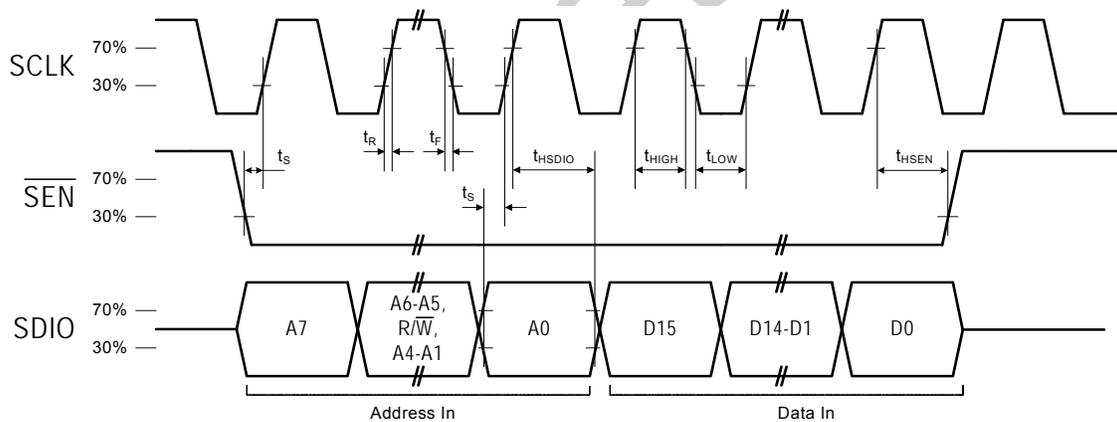
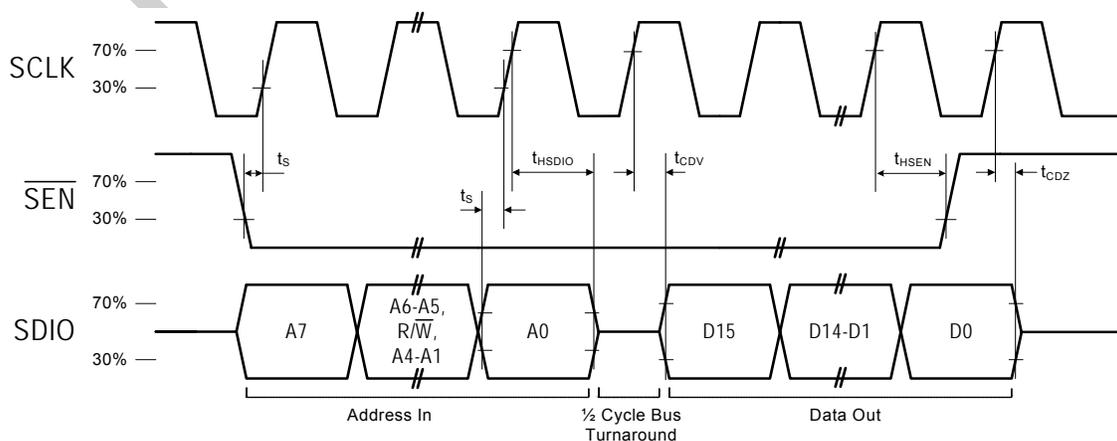


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics $(V_A = 2.7 \text{ to } 5.5 \text{ V}, V_D = 1.62 \text{ to } 3.6 \text{ V}, T_A = -20 \text{ to } 85 \text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{\text{SEN}}$ to SCLK \uparrow Setup	t_s		20	—	—	ns
SDIO Input to SCLK \uparrow Hold	t_{HSDIO}		10	—	—	ns
$\overline{\text{SEN}}$ Input to SCLK \downarrow Hold	t_{HSEN}		10	—	—	ns
SCLK \uparrow to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK \uparrow to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{\text{SEN}}$, SDIO, Rise/Fall time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

**Figure 4. 3-Wire Control Interface Write Timing Parameters****Figure 5. 3-Wire Control Interface Read Timing Parameters**

Si4730/31-D50

Table 7. Digital Audio Interface Characteristics

($V_A = 2.7$ to 5.5 V, $V_D = 1.62$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOOUT}$		0	—	12	ns

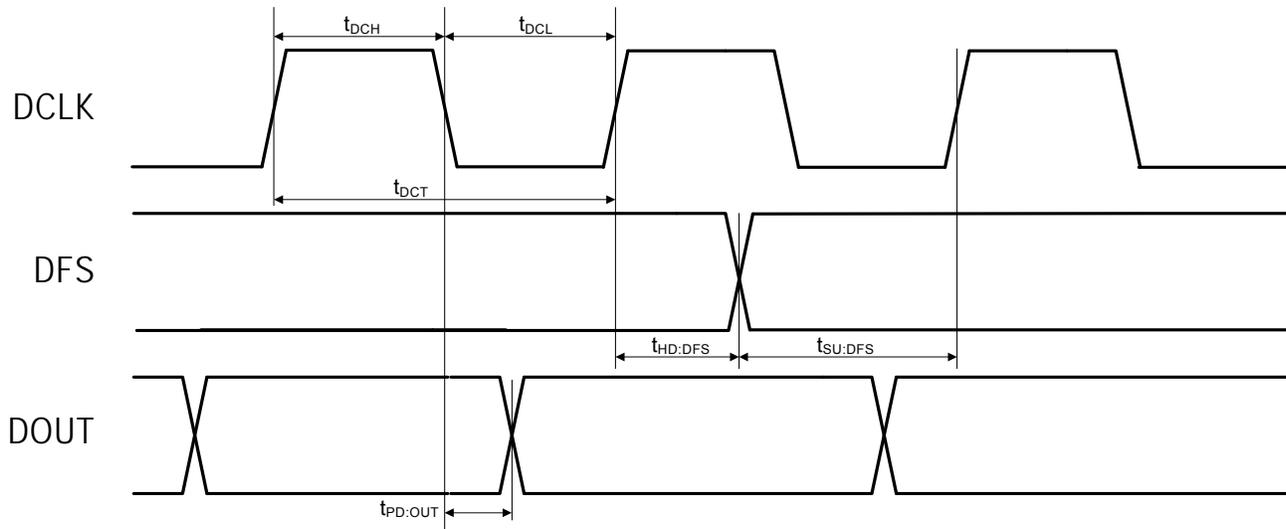


Figure 6. Digital Audio Interface Timing Parameters, I²S Mode

Table 8. FM Receiver Characteristics^{1,2}(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = -20 to 85 °C, 76–108 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}		76	—	108	MHz
Sensitivity ^{3,4,5}		(S+N)/N = 26 dB	—	2.2	3.5	μV EMF
RDS Sensitivity ⁶		Δf = 2 kHz, RDS BLER < 5%	—	11	—	μV EMF
LNA Input Resistance ^{6,7}			3	4	5	kΩ
LNA Input Capacitance ^{6,7}			4	5	6	pF
Input IP3 ^{6,8}			100	105	—	dBμV EMF
AM Suppression ^{3,4,6,7}		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection ⁶		In-band	35	—	—	dB
Audio Output Voltage ^{3,4,7}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,7,9}			—	—	1	dB
Audio Frequency Response Low ⁶		-3 dB	—	—	30	Hz
Audio Frequency Response High ⁶		-3 dB	15	—	—	kHz
Audio Stereo Separation ^{7,9}			35	42	—	dB
Audio Mono S/N ^{3,4,5,7}			55	63	—	dB
Audio Stereo S/N ^{4,5,6,7}			—	58	—	dB
Audio THD ^{3,7,9}			—	0.1	0.5	%
De-emphasis Time Constant ⁶		FM_DEEMPHASIS = 2	70	75	80	μs
		FM_DEEMPHASIS = 1	45	50	54	μs
Blocking Sensitivity ^{3,4,5,6,12,13}		Δf = ±400 kHz	—	34	—	dBμV
		Δf = ±4 MHz	—	30	—	dBμV

Notes:

- Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
- To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
- F_{MOD} = 1 kHz, 75 μs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
- Δf = 22.5 kHz.
- B_{AF} = 300 Hz to 15 kHz, A-weighted.
- Guaranteed by characterization.
- V_{EMF} = 1 mV.
- |f₂ - f₁| > 2 MHz, f₀ = 2 x f₁ - f₂. AGC is disabled.
- Δf = 75 kHz.
- At L_{OUT} and R_{OUT} pins.
- Analog audio output mode.
- Blocker Amplitude = 100 dBμV
- Sensitivity measured at (S+N)/N = 26 dB.
- At temperature (25°C).

Si4730/31-D50

Table 8. FM Receiver Characteristics^{1,2} (Continued)

($V_A = 2.7$ to 5.5 V, $V_D = 1.62$ to 3.6 V, $T_A = -20$ to 85 °C, 76 – 108 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod Sensitivity ^{3,4,5,6,12,13}		$\Delta f = \pm 400$ kHz, ± 800 kHz	—	40	—	dB μ V
		$\Delta f = \pm 4$ MHz, ± 8 MHz	—	35	—	dB μ V
Audio Output Load Resistance ^{6,10}	R_L	Single-ended	10	—	—	k Ω
Audio Output Load Capacitance ^{6,10}	C_L	Single-ended	—	—	50	pF
Seek/Tune Time ⁶		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time ⁶		From powerdown	—	—	110	ms
RSSI Offset ¹⁴		Input levels of 8 and 60 dB μ V at RF Input	-3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. $F_{MOD} = 1$ kHz, 75 μ s de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. $\Delta f = 22.5$ kHz.
5. $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. $V_{EMF} = 1$ mV.
8. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled.
9. $\Delta f = 75$ kHz.
10. At L_{OUT} and R_{OUT} pins.
11. Analog audio output mode.
12. Blocker Amplitude = 100 dB μ V
13. Sensitivity measured at $(S+N)/N = 26$ dB.
14. At temperature (25°C).

Table 9. 64–75.9 MHz Input Frequency FM Receiver Characteristics^{1,2,6}(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f _{RF}		64	—	75.9	MHz
Sensitivity ^{3,4,5}		(S+N)/N = 26 dB	—	3.5	—	μV EMF
LNA Input Resistance ⁷			3	4	5	kΩ
LNA Input Capacitance ⁷			4	5	6	pF
Input IP3 ⁸			—	105	—	dBμV EMF
AM Suppression ^{3,4,7}		m = 0.3	—	50	—	dB
Adjacent Channel Selectivity		±200 kHz	—	50	—	dB
Alternate Channel Selectivity		±400 kHz	—	70	—	dB
Audio Output Voltage ^{3,4,7}			72	80	90	mV _{RMS}
Audio Output L/R Imbalance ^{3,7,9}			—	—	1	dB
Audio Frequency Response Low		–3 dB	—	—	30	Hz
Audio Frequency Response High		–3 dB	15	—	—	kHz
Audio Mono S/N ^{3,4,5,7,10}			—	63	—	dB
Audio THD ^{3,7,9}			—	0.1	—	%
De-emphasis Time Constant		FM_DEEMPHASIS = 2	70	75	80	μs
		FM_DEEMPHASIS = 1	45	50	54	μs
Audio Output Load Resistance ¹⁰	R _L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance ¹⁰	C _L	Single-ended	—	—	50	pF
Seek/Tune Time		RCLK tolerance = 100 ppm	—	—	60	ms/channel
Powerup Time		From powerdown	—	—	110	ms
RSSI Offset ¹¹		Input levels of 8 and 60 dBμV EMF	–3	—	3	dB

Notes:

1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 μs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. V_{EMF} = 1 mV.
8. |f₂ – f₁| > 2 MHz, f₀ = 2 x f₁ – f₂. AGC is disabled.
9. Δf = 75 kHz.
10. At L_{OUT} and R_{OUT} pins.
11. At temperature (25 °C).

Si4730/31-D50

Table 10. AM Receiver Characteristics^{1,2}

($V_A = 2.7$ to 5.5 V, $V_D = 1.62$ to 3.6 V, $T_A = -20$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		520	—	1710	kHz
Sensitivity ^{3,5,6}		(S+N)/N = 26 dB	—	25	35	μ V EMF
Large Signal Voltage Handling ^{6,7}		THD < 8%	—	300	—	mV _{RMS}
Power Supply Rejection Ratio ⁶		$\Delta V_A = 100$ mV _{RMS} , 100 Hz	—	40	—	dB
Audio Output Voltage ^{3,8}			54	60	67	mV _{RMS}
Audio S/N ^{3,5,8}			50	60	—	dB
Audio THD ^{3,8}			—	0.1	0.5	%
Antenna Inductance ^{6,9}			180	—	450	μ H
Powerup Time ⁶		From powerdown	—	—	110	ms

Notes:

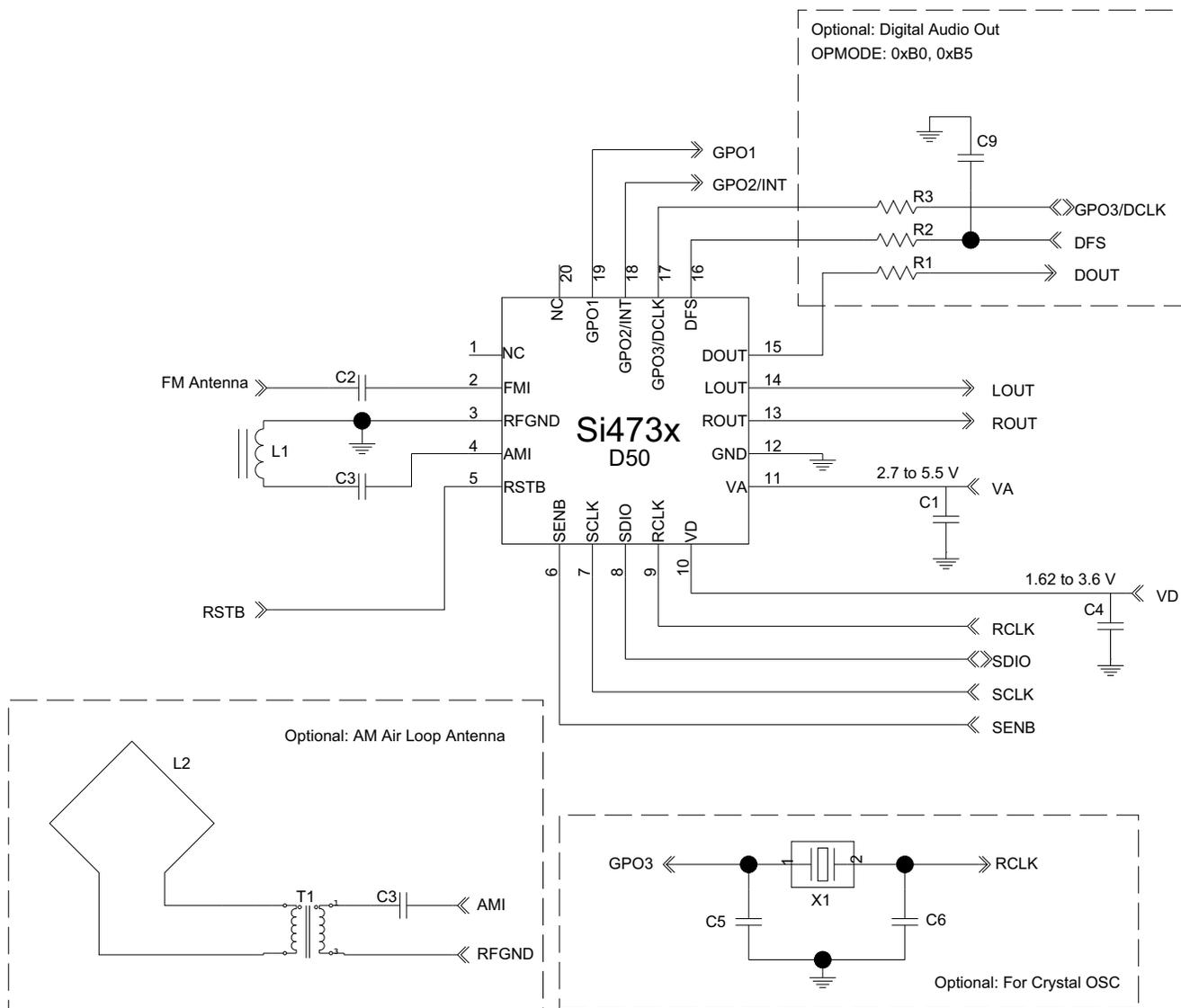
1. Additional testing information is available in “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at RF = 520 kHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. FMOD = 1 kHz, 30% modulation, 2 kHz channel filter.
4. Analog audio output mode.
5. $B_{AF} = 300$ Hz to 15 kHz, A-weighted.
6. Guaranteed by characterization.
7. See “AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure” for evaluation method.
8. $V_{IN} = 5$ mVrms.
9. Stray capacitance on antenna and board must be < 10 pF to achieve full tuning range at higher inductance levels.

Table 11. Reference Clock and Crystal Characteristics(V_A = 2.7 to 5.5 V, V_D = 1.62 to 3.6 V, T_A = -20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies ¹			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance ²			-100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance ²			-100	—	100	ppm
Board Capacitance			—	—	3.5	pF
ESR			—	40	—	Ω
C _L Single-ended			—	12	—	pF
Notes:						
1. The Si4730/31 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. For more details, see Table 6 of "AN332: Si47xx Programming Guide".						
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.						

Si4730/31-D50

2. Typical Application Schematic



Notes:

1. Place C1 close to V_A pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in "AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the FM antenna interface, and pin 4 connects to the AM antenna interface.
6. Place Si4730/31 as close as possible to antenna and keep the FMI and AMI traces as short as possible.

3. Bill of Materials

Table 12. Si4730/31-D50 Bill of Materials

Component	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, $\pm 20\%$, Z5U/X7R	Murata
C2	Coupling capacitor, 1 nF, $\pm 20\%$, Z5U/X7R	Murata
C3	Coupling capacitor, 0.47 μ F, $\pm 20\%$, Z5U/X7R	Murata
C4	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R	Murata
L1	Ferrite loop stick, 180–450 μ H	Jiaxin
U1	Si4730/31 AM/FM Radio Tuner	Silicon Laboratories
R1	Resistor, 600 Ω (Optional for digital audio)	Venkel
R2	Resistor, 2 k Ω (Optional for digital audio)	Venkel
R3	Resistor, 2 k Ω (Optional for digital audio)	Venkel
C5, C6	Crystal load capacitors, 22 pF, $\pm 5\%$, COG (Optional for crystal oscillator option)	Venkel
C9	Noise mitigating capacitor, 2~5 pF (Optional for digital audio)	Murata
L2	Air Loop, 10–20 μ H (Optional for AM Input)	Jiaxin
T1	Transformer, 1:5 turns ratio (Optional for AM Input)	Jiaxin, UMEC
X1	32.768 kHz crystal (Optional for crystal oscillator option)	Epson

4. Functional Description

4.1. Overview

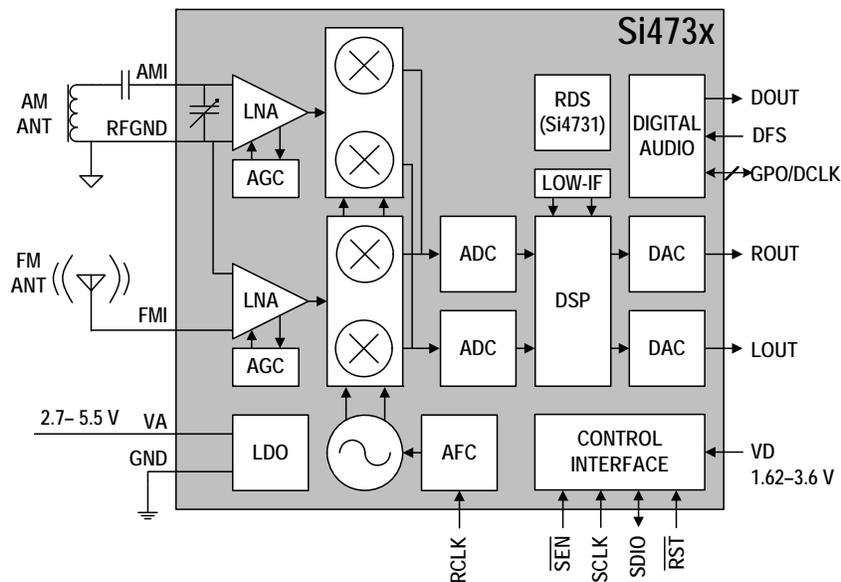


Figure 7. Functional Block Diagram

The Si4730/31-D50 is Silicon Labs' fourth generation fully integrated, 100% CMOS AM/FM radio receiver IC. Offering unmatched integration and PCB space savings, the Si4730/31 requires only two external components and less than 15 mm² of board area, excluding the antenna inputs. The Si4730/31 AM/FM radio provides the space savings and low power consumption necessary for portable devices while delivering the high performance and design simplicity desired for all AM/FM solutions.

Leveraging Silicon Laboratories' proven and patented Si4700/01 FM tuner's digital low intermediate frequency (low-IF) receiver architecture, the Si4730/31 delivers superior RF performance and interference rejection in both AM and FM bands. The high integration and complete system production test simplifies design-in, increases system quality, and improves manufacturability.

The Si4730/31 is a feature-rich solution that includes advanced seek algorithms, soft mute, auto-calibrated digital tuning, FM stereo processing, and advanced audio processing.

In addition, the Si4730/31 provides analog and digital audio outputs and a programmable reference clock. The device supports I²C-compatible 2-wire control interface, SPI, and a Si4700/01 backwards-compatible 3-wire control interface.

The Si4730/31 utilizes digital processing to achieve high

fidelity, optimal performance, and design flexibility. The chip provides excellent pilot rejection, selectivity, and unmatched audio performance, and offers both the manufacturer and the end-user extensive programmability and flexibility in the listening experience.

The Si4731 incorporates a digital processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. Using this feature, the Si4731 enables broadcast data such as station identification and song name to be displayed to the user.

4.2. Operating Modes

The Si4730/31 operates in either an FM receive or an AM receive mode. In FM mode, radio signals are received on FMI and processed by the FM front-end circuitry. In AM mode, radio signals are received on AMI and processed by the AM front-end circuitry. In addition to the receiver mode, there is an audio output mode to choose between an analog and/or digital audio output. In the analog audio output mode, ROUT and LOUT are used for the audio output pins. In the digital audio mode, DOUT, DFS, and DCLK pins are used. Concurrent analog/digital audio output mode is also available requiring all five pins.

4.3. FM Receiver

The Si4730/31 FM receiver is based on the proven Si4700/01 FM tuner. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The Si4730/31 integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (64 to 108 MHz). An AGC circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the Si4730/31 to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.4. AM Receiver

The highly-integrated Si4730/31 supports worldwide AM band reception from 520 to 1710 kHz using a digital low-IF architecture with a minimum number of external components and no manual alignment required. This digital low-IF architecture allows for high-precision filtering offering excellent selectivity and SNR with minimum variation across the AM band. The DSP also provides adjustable channel step sizes in 1 kHz increments, AM demodulation, soft mute, seven different channel bandwidth filters, and additional features, such as a programmable automatic volume control (AVC) maximum gain allowing users to adjust the level of background noise.

Similar to the FM receiver, the integrated LNA and AGC optimize sensitivity and rejection of strong interferers allowing better reception of weak stations.

The Si4730/31 provides highly-accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180–450 μ H. An air loop antenna is supported by using a transformer to increase the effective inductance from the air loop. Using a 1:5 turn ratio inductor, the inductance is increased by 25 times and easily supports all typical AM air loop antennas which generally vary between 10 and 20 μ H.

4.5. Digital Audio Interface

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I²S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si473x supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

4.5.1. Audio Data Formats

The digital audio interface operates in slave mode and supports three different audio data formats:

- I²S
- Left-Justified
- DSP Mode

In I²S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In left-justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. If preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.5.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

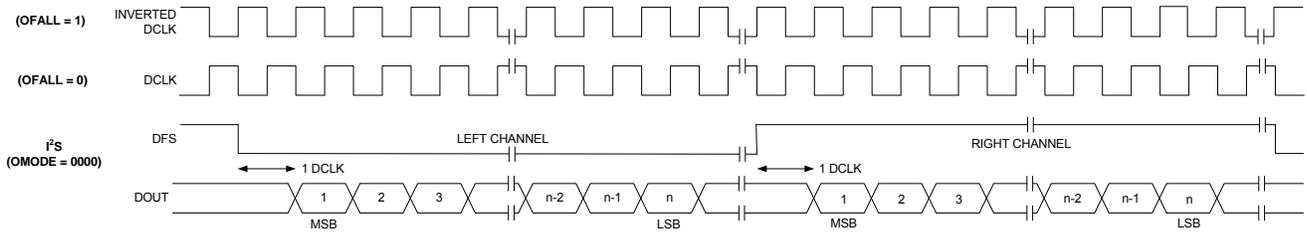


Figure 8. I²S Digital Audio Format

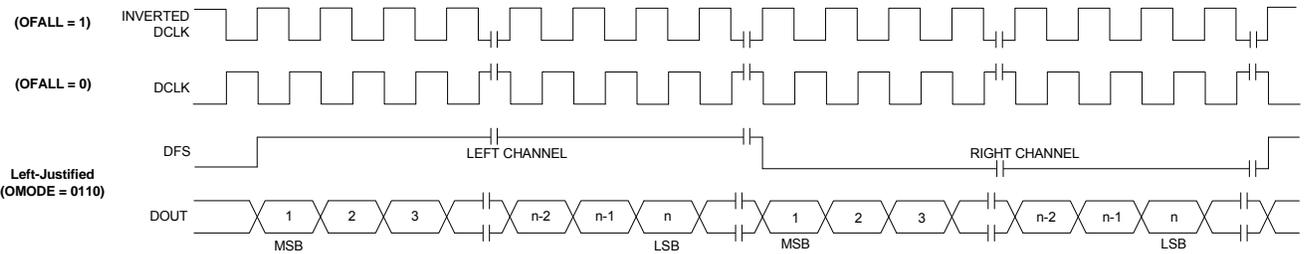


Figure 9. Left-Justified Digital Audio Format

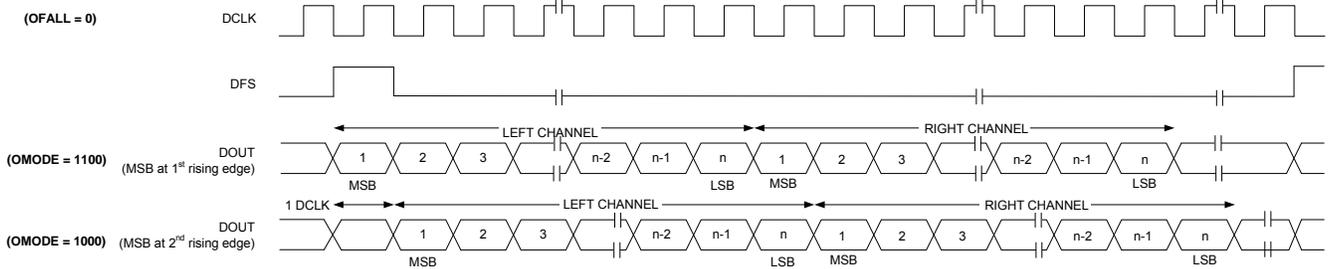


Figure 10. DSP Digital Audio Format

4.6. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 11 below.

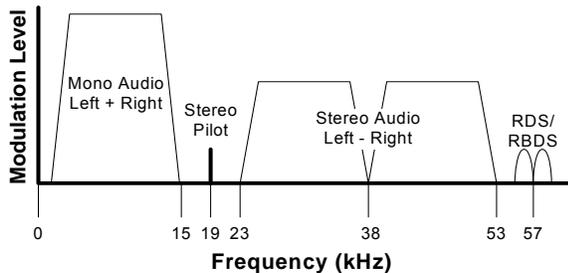


Figure 11. MPX Signal Spectrum

4.6.1. Stereo Decoder

The Si4730/31's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4731 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

4.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Three metrics, received signal strength indicator (RSSI), signal-to-noise ratio (SNR), and multipath interference, are monitored simultaneously in forcing a blend from stereo to mono. The metric which reflects the minimum signal quality takes precedence and the signal is blended appropriately.

All three metrics have programmable stereo/mono thresholds and attack/release rates detailed in "AN332: Si47xx Programming Guide." If a metric falls below its mono threshold, the signal is blended from stereo to full mono. If all metrics are above their respective stereo thresholds, then no action is taken to blend the signal. If a metric falls between its mono and stereo thresholds, then the signal is blended to the level proportional to the metric's value between its mono and stereo thresholds, with an associated attack and release rate.

4.7. Received Signal Qualifiers

The quality of a tuned signal can vary depending on many factors including environmental conditions, time of day, and position of the antenna. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si473x monitors and provides indicators of the signal quality. The Si473x monitors signal quality metrics including RSSI, SNR, and multipath interference on FM signals. These metrics are used to optimize audio and signal processing and are also reported to the host processor. The signal processing algorithms can use either Silicon Labs' optimized settings (recommended) or be customized to modify performance.

4.8. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4730/31 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 μ s.

4.9. Volume Control

The audio output may be muted. Volume is adjusted digitally by the RX_VOLUME property.

4.10. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted.

4.11. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The soft mute feature is triggered by the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and release rates.

4.12. FM Hi-Cut Control

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multipath interference. Two metrics, SNR and multipath interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metrics. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. Attack and release rates for hi-cut are programmable for both metrics from a range of 2 ms to 64 s. The level of hi-cut applied can be monitored with the FM_RSQ_STATUS command. Hi-cut can be disabled by setting the hi-cut filter to audio bandwidth of 15 kHz.

4.13. RDS/RBDS Processor (Si4731 Only)

The Si4731 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4731 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4731 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

4.14. Tuning

The tuning frequency is directly programmed using the FM_TUNE_FREQ and AM_TUNE_FREQ commands. The Si4730/31 supports channel spacing steps of 10 kHz in FM mode and 1 kHz in AM mode.

4.15. Seek

The Si4730/31 seek functionality is performed completely on-chip and will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations or, if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt. Refer to “AN332: Si47xx Programming Guide”.

The Si4730/31 uses RSSI, SNR, and AFC to qualify stations. Most of these variables have programmable thresholds for modifying the seek function according to customer needs.

RSSI is employed first to screen all possible candidate stations. SNR and AFC are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations. The Si4730/31 defaults set RSSI to a mid-level threshold and add an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations while keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire FM band with all thresholds engaged is very short depending on the band content. Seek is initiated using the FM_SEEK_START command. The RSSI, SNR, and AFC threshold settings are adjustable using properties.

4.16. Reference Clock

The Si4730/31 reference clock is programmable, supporting RCLK frequencies listed in Table 11, “Reference Clock and Crystal Characteristics,” on page 15. Refer to Table 3, “DC Characteristics,” on page 5 for switching voltage levels and Table 11 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to “2. Typical Application Schematic” on page 16. This mode is enabled using the POWER_UP command. Refer to “AN332: Si47xx Programming Guide”.

The Si4730/31 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4730/31 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4730/31 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

4.17. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4730/31 and receive responses from the device. The serial port can operate in two bus modes: 2-wire mode and 3-wire mode. The Si4730/31 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of $\overline{\text{RST}}$. The GPO1 pin includes an internal pull-up resistor, which is connected while $\overline{\text{RST}}$ is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while $\overline{\text{RST}}$ is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 13.

Table 13. Bus Mode Select on Rising Edge of $\overline{\text{RST}}$

Bus Mode	GPO1	GPO2
2-Wire	1	0
3-Wire	0 (must drive)	0

After the rising edge of $\overline{\text{RST}}$, the pins GPO1 and GPO2 are used as general purpose output (O) pins, as described in Section “4.18. GPO Outputs”. In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.17.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{\text{RST}}$, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4730/31 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4730/31 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). Refer to “AN332: Si47xx Programming Guide”

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4730/31 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4730/31 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4730/31. A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

4.17.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{\text{RST}}$.

The 3-wire bus mode uses the SCLK, SDIO, and $\overline{\text{SEN}}$ pins. A transaction begins when the user drives $\overline{\text{SEN}}$ low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 9-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4730/31 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets $\overline{\text{SEN}}$ high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while $\overline{\text{SEN}}$ is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

4.18. GPO Outputs

The Si4730/31 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-impedance. The GPO pins can be reconfigured as specialized functions. GPO2/INT can be configured to provide interrupts and GPO3 can be configured to provide external crystal support or as DCLK in digital audio output mode.

4.19. Firmware Upgrades

The Si4730/31 contains on-chip program RAM to accommodate minor changes to the firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new radio designs and those already deployed in the field.

4.20. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

4.21. Programming with Commands

To ease development time and offer maximum customization, the Si4730/31 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

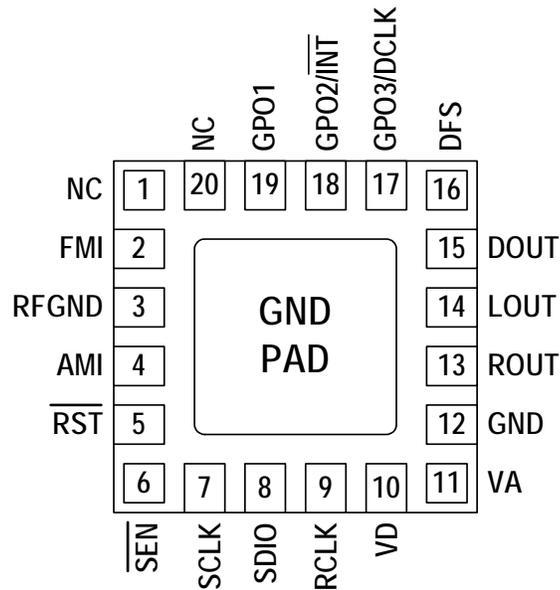
To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a 1-byte status update, indicating interrupt and clear-to-send status information.

For a detailed description of the commands and properties for the Si4730/31, see “AN332: Si47xx Programming Guide.”

5. Pin Descriptions: Si4730/31-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF inputs. FMI should be connected to the antenna trace.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	AMI	AM RF input. AMI should be connected to the AM antenna.
5	RST	Device reset (active low) input.
6	SEN	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	V _D	Digital and I/O supply voltage.
11	V _A	Analog supply voltage. May be connected directly to battery.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.
13	ROUT	Right audio line output in analog output mode.
14	LOUT	Left audio line output in analog output mode.
15	DOUT	Digital output data in digital output mode.
16	DFS	Digital frame synchronization input in digital output mode.
17	GPO3/DCLK	General purpose output, crystal oscillator, or digital bit synchronous clock input in digital output mode.
18	GPO2/INT	General purpose output or interrupt pin.
19	GPO1	General purpose output.

Si4730/31-D50

6. Ordering Guide

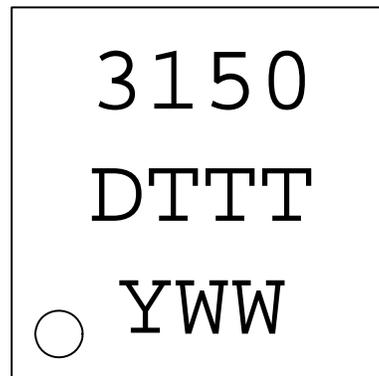
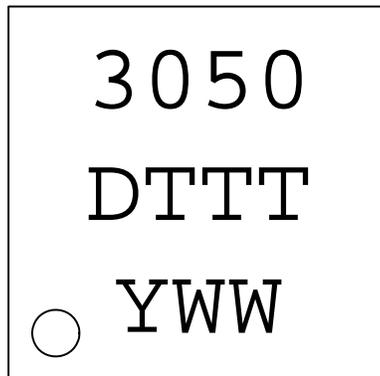
Part Number*	Description	Package Type	Operating Temperature/Voltage
Si4730-D50-GM	AM/FM Broadcast Radio Receiver	QFN Pb-free	-20 to 85 °C 2.7 to 5.5 V
Si4731-D50-GM	AM/FM Broadcast Radio Receiver with RDS/RBDS	QFN Pb-free	-20 to 85 °C 2.7 to 5.5 V

***Note:** Add an "(R)" at the end of the device part number to denote tape and reel option.

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7. Package Markings (Top Marks)

7.1. Si4730/31 Top Mark



7.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	30 = Si4730, 31 = Si4731.
	Firmware Revision	50 = Firmware Revision 5.0.
Line 2 Marking:	Die Revision	D = Revision D Die.
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier.
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and work week of the mold date.

Si4730/31-D50

8. Package Outline: Si4730/31

Figure 12 illustrates the package details for the Si4730/31. Table 14 lists the values for the dimensions shown in the illustration.

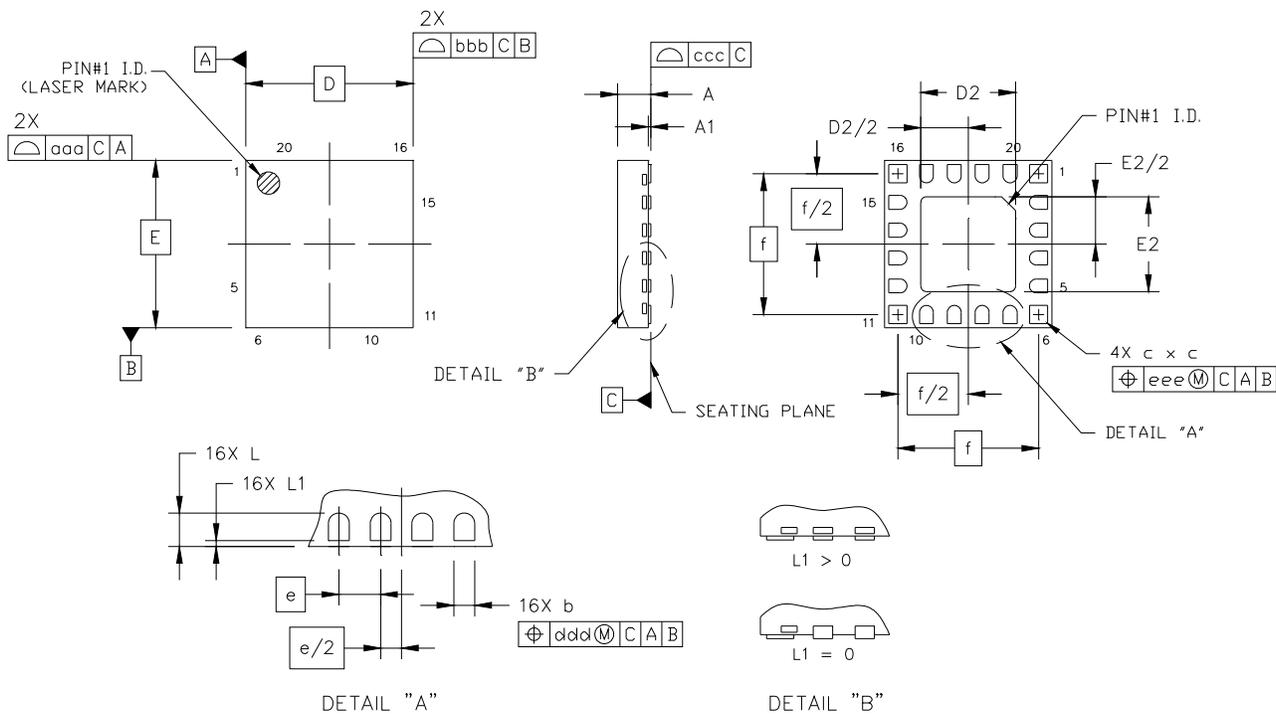


Figure 12. 20-Pin Quad Flat No-Lead (QFN)

Table 14. Package Dimensions

Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.50	0.55	0.60	f	2.53 BSC		
A1	0.00	0.02	0.05	L	0.35	0.40	0.45
b	0.20	0.25	0.30	L1	0.00	—	0.10
c	0.27	0.32	0.37	aaa	—	—	0.05
D	3.00 BSC			bbb	—	—	0.05
D2	1.65	1.70	1.75	ccc	—	—	0.08
e	0.50 BSC			ddd	—	—	0.10
E	3.00 BSC			eee	—	—	0.10
E2	1.65	1.70	1.75				

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

9. PCB Land Pattern: Si4730/31

Figure 13 illustrates the PCB land pattern details for the Si4730/31-D50-GM QFN. Table 15 lists the values for the dimensions shown in the illustration.

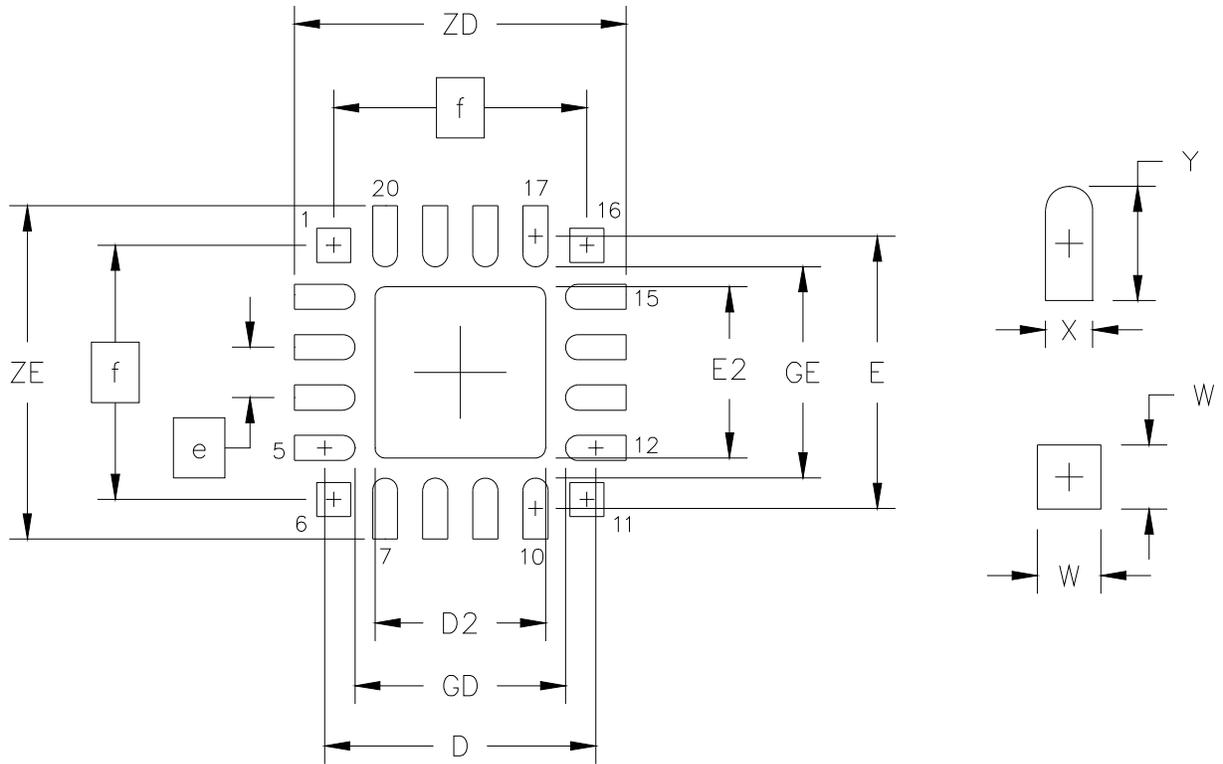


Figure 13. PCB Land Pattern

Table 15. PCB Land Pattern Dimensions

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
D	2.71 REF		GE	2.10	—
D2	1.60	1.80	W	—	0.34
e	0.50 BSC		X	—	0.28
E	2.71 REF		Y	0.61 REF	
E2	1.60	1.80	ZE	—	3.31
f	2.53 BSC		ZD	—	3.31
GD	2.10	—			

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Additional Reference Resources

Contact your local sales representatives for more information or to obtain copies of the following references:

- AN332: Si47xx Programming Guide
- AN383: Si47xx Antenna, Schematic, Layout, and Design Guidelines
- AN388: Si470x/1x/2x/3x/4x Evaluation Board Test Procedure
- Si47xx EVB User's Guide
- Customer Support Site: www.silabs.com
This site contains all application notes, evaluation board schematics and layouts, and evaluation software.
Please visit the Silicon Labs Technical Support web page:
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx> and register to submit a technical support request.

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DOCUMENT CHANGE LIST:

Revision 0.2 to Revision 1.0

- Updated functional block diagram.
- Updated specification tables.
- Updated “2. Typical Application Schematic”.
- Updated “Table 3. DC Characteristics”.
- Added Section “4.6. Stereo Audio Processing”.

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NOTES:

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CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: FMinfo@silabs.com
Internet: www.silabs.com

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