



# STE140NF20D

N-channel 200 V, 10 mΩ typ., 140 A STripFET™ II Power MOSFET (with fast diode) in an ISOTOP package

Datasheet – production data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STE140NF20D	200 V	< 0.012 Ω	140 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested

## Applications

Switching applications

## Description

This Power MOSFET is produced using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. The device offers extremely fast switching performance thanks to the intrinsic fast body diode, making the device ideal for hard switching topologies.

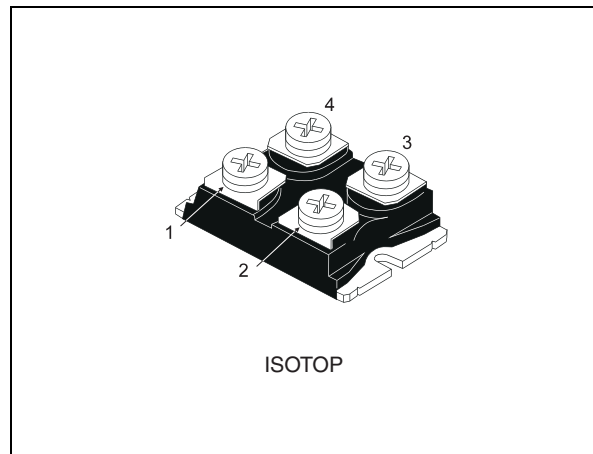


Figure 1. Internal schematic diagram

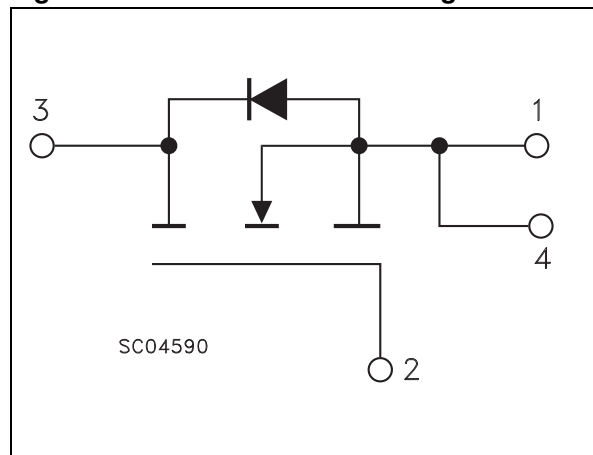


Table 1. Device summary

Order code	Marking	Package	Packaging
STE140NF20D	140NF20D	ISOTOP	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	200	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	140	A
$I_D$	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	88	A
$I_{DM}^{(1)}$	Drain current (pulsed)	560	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	500	W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not repetitive	140	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	800	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	25	V/ns
$V_{ISO}$	Insulation withstand voltage (AC-RMS)	2500	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. Pulse width limited by  $T_{jmax}$
3. Strating  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$
4.  $I_{SD} \leq 140\text{ A}$ ,  $di/dt \leq 1000\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BR)DSS}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	40	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 200\text{ V}$ , $V_{DS} = 200\text{ V}$ , $T_C = 125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 70\text{ A}$		10	12	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	11100	-	pF
$C_{oss}$	Output capacitance			2190		
$C_{rss}$	Reverse transfer capacitance			334		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }160\text{ V}$ , $V_{GS} = 0$ ,	-	1525	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			1139		
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 160\text{ V}$ , $I_D = 140\text{ A}$ , $V_{GS} = 10\text{ V}$ (see Figure 16)	-	338	-	nC
$Q_{gs}$	Gate-source charge			47		
$Q_{gd}$	Gate-drain charge			183		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$ , $I_D = 70\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 15)	-	232	-	ns
$t_r$	Rise time			218		ns
$t_{d(off)}$	Turn-off delay time			283		ns
$t_f$	Fall time			250		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		140	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		560	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 140\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 140\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	190		ns
$Q_{rr}$	Reverse recovery charge			1.4		nC
$I_{RRM}$	Reverse recovery current			14		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 140\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	257		ns
$Q_{rr}$	Reverse recovery charge			2.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			18		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

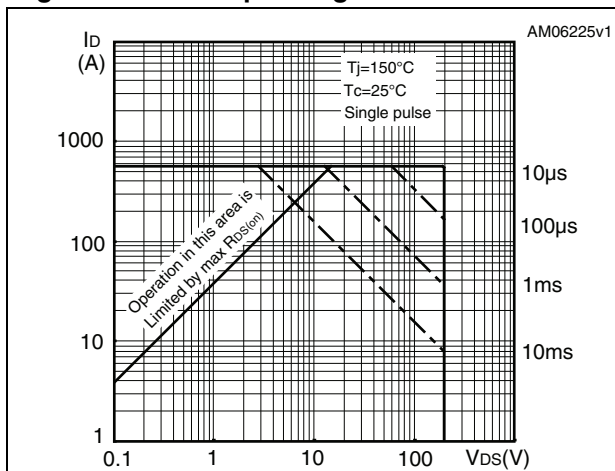


Figure 3. Thermal impedance

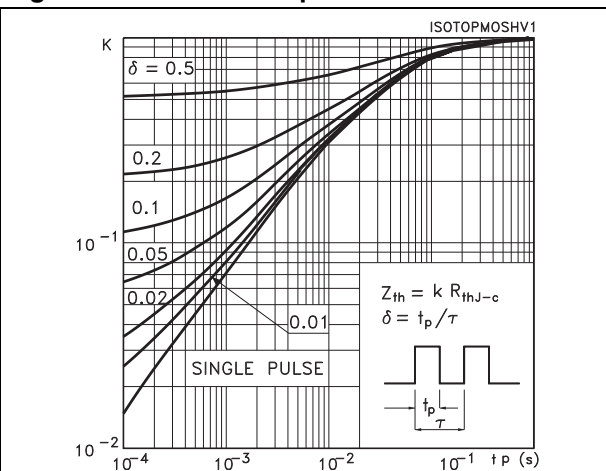


Figure 4. Output characteristics

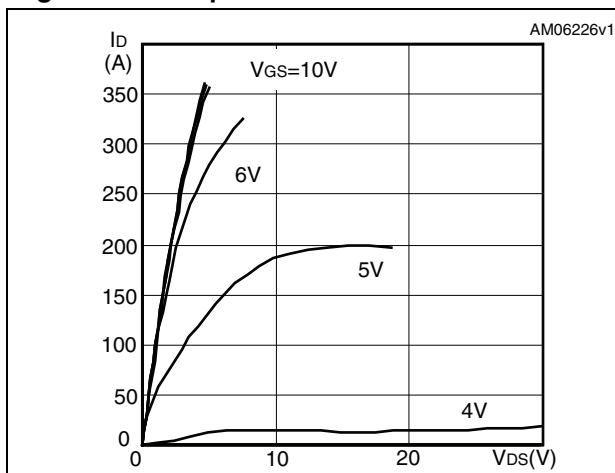


Figure 5. Transfer characteristics

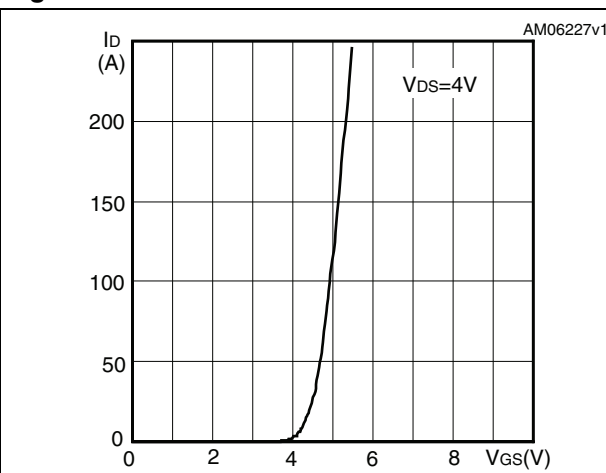


Figure 6. Gate charge vs gate-source voltage

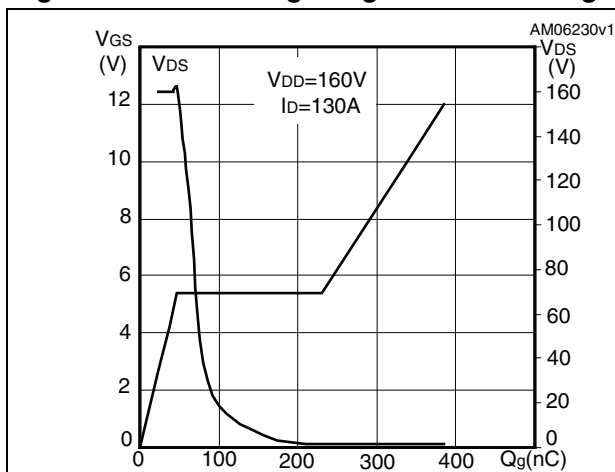


Figure 7. Static drain-source on-resistance

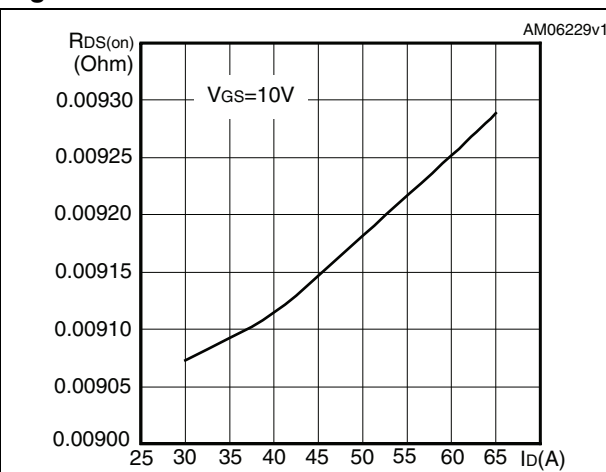


Figure 8. Capacitance variations

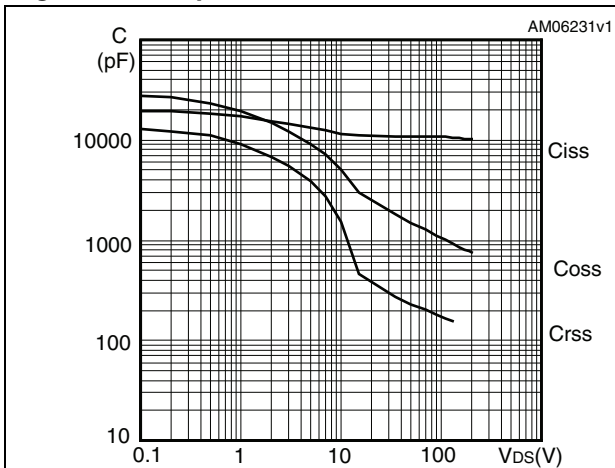


Figure 9. Output capacitance stored energy

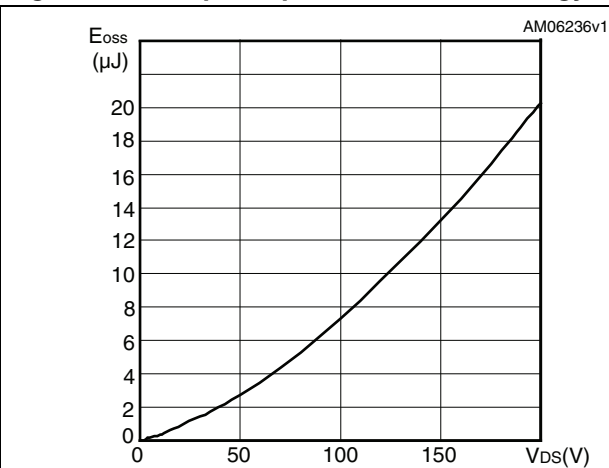


Figure 10. Normalized gate threshold voltage vs temperature

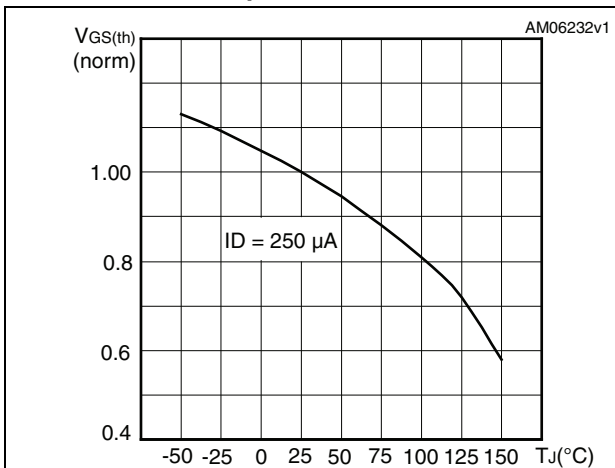


Figure 11. Normalized on resistance vs temperature

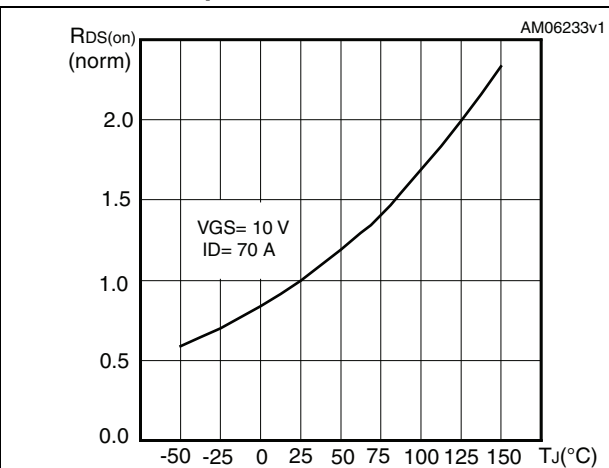


Figure 12. Source-drain diode forward characteristics

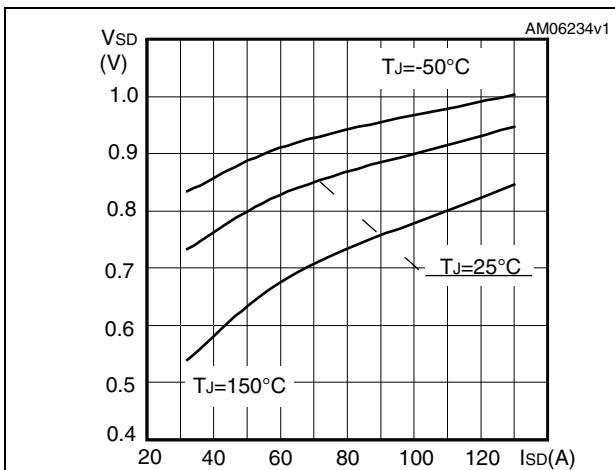


Figure 13. Normalized B<sub>VDS</sub> vs temperature

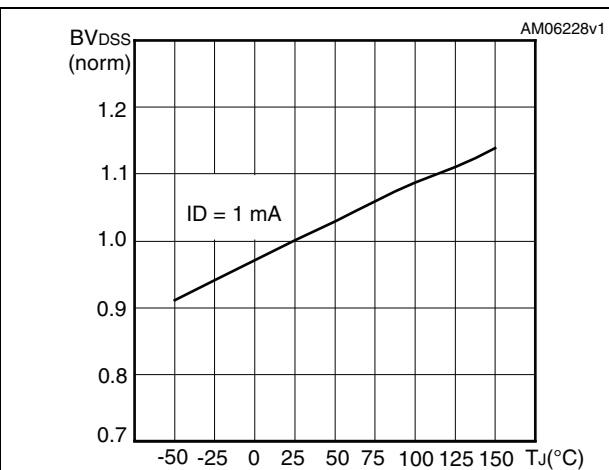
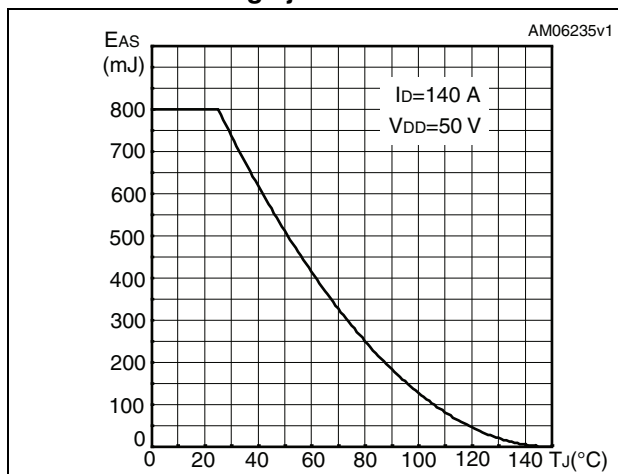


Figure 14. Maximum avalanche energy vs starting Tj





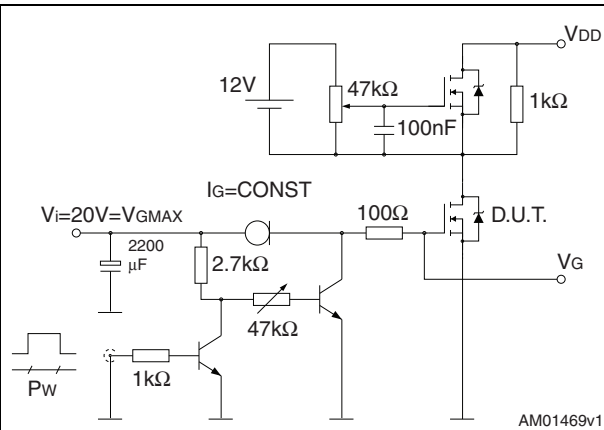
### 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**



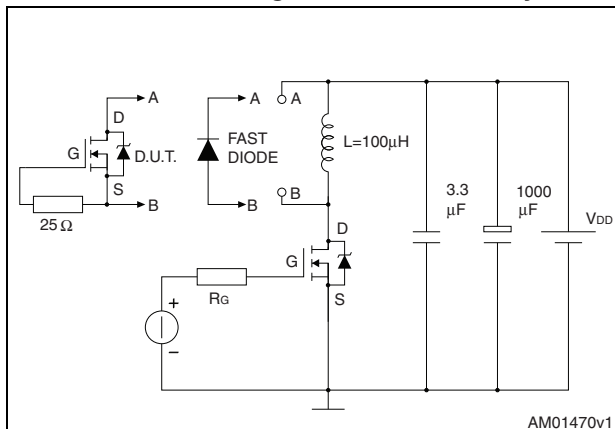
AM01468v1

**Figure 16. Gate charge test circuit**



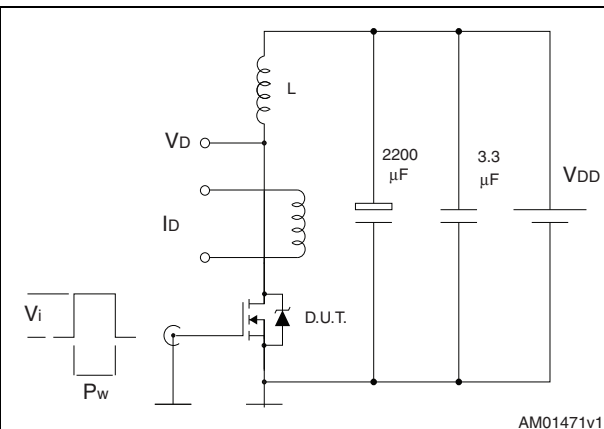
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**Figure 17. Test circuit for inductive load switching and diode recovery times**



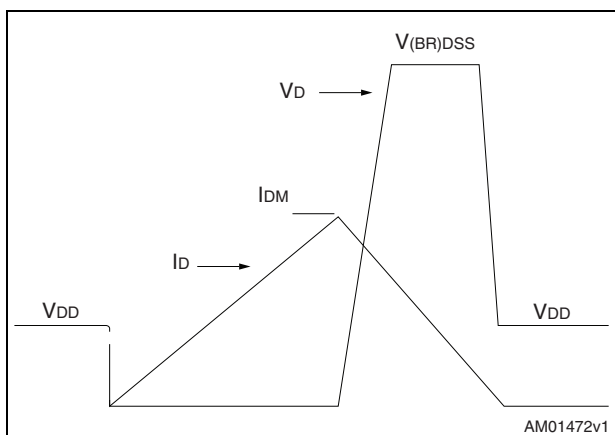
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**Figure 18. Unclamped inductive load test circuit**



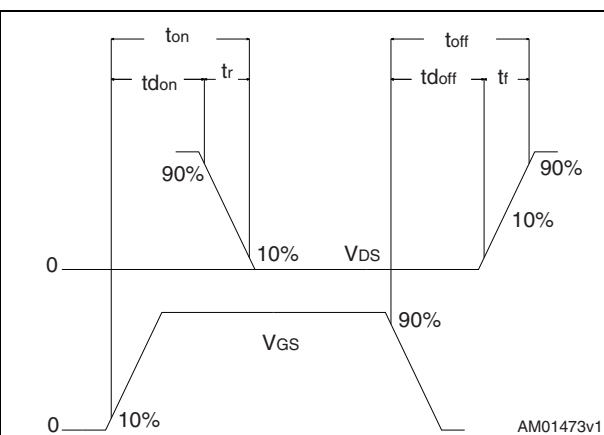
AM01471v1

**Figure 19. Unclamped inductive waveform**



AM01472v1

**Figure 20. Switching time waveform**



AM01473v1

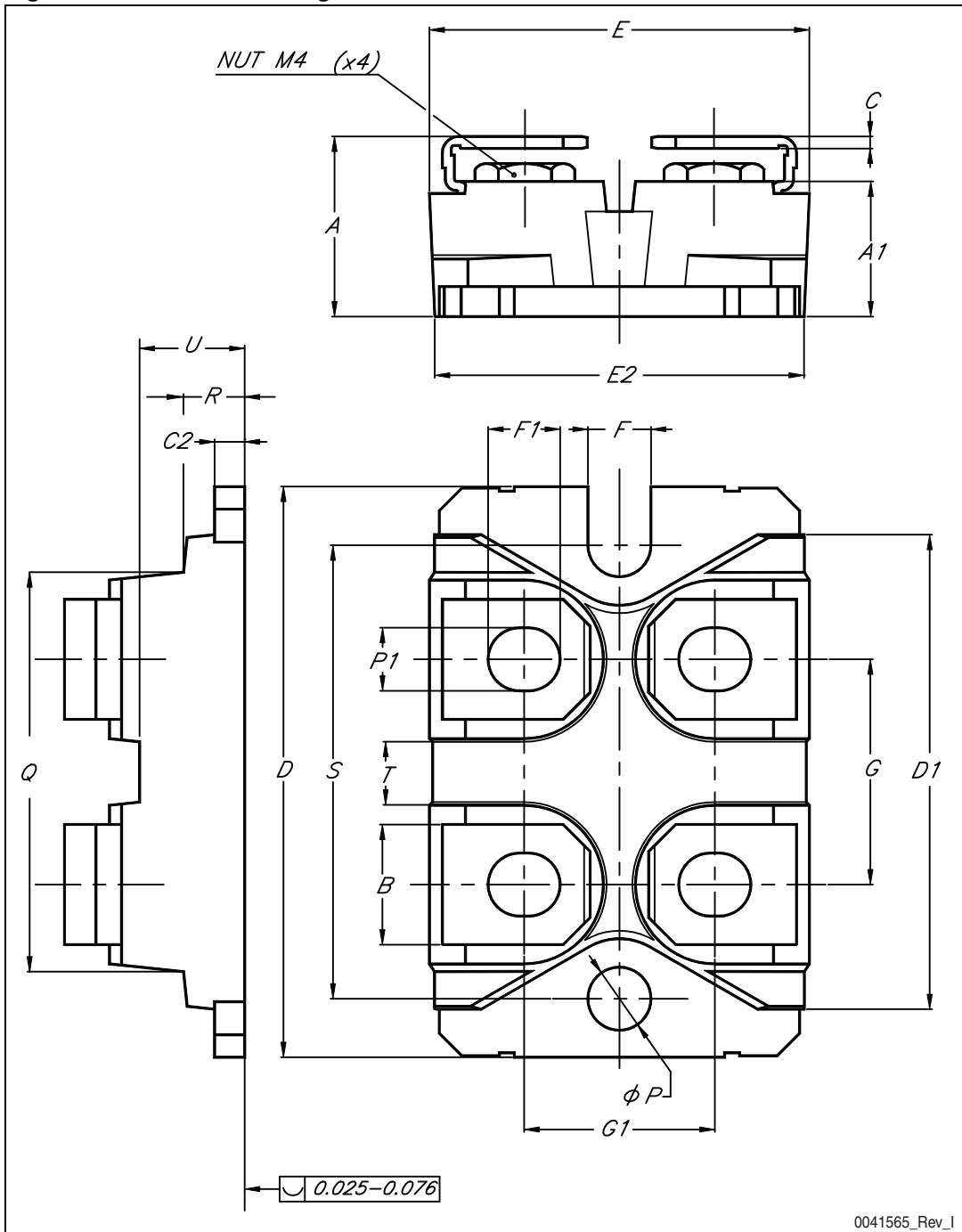
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. ISOTOP mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	11.76		12.19
A1	8.92		9.58
B	7.80		8.18
C	0.76		0.84
C2	1.98		2.13
D	38		38.20
D1	31.50		31.70
E	25.20		25.45
E2	24.59		25.07
G	14.91		15.09
G1	12.57		12.83
F	4.09		4.19
F1	4.67		4.93
ΦP	4.09		4.27
P1	4.06		4.32
Q	26.54		26.90
R	3.94		4.42
S	30.12		30.30
T	3.30		3.61
U	6.88		7.09

Figure 21. ISOTOP drawing



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
27-Jan-2009	1	First release
18-Jan-2010	2	Document status promoted from preliminary data to datasheet.
01-Jul-2010	3	Inserted $V_{ISO}$ parameter in <a href="#">Table 2: Absolute maximum ratings</a>
17-Oct-2012	4	Updated: <a href="#">Figure 1, 5, 6, 10, 11, 13</a> . Updated: $I_{SD}$ value in note 4 (below <a href="#">Table 2: Absolute maximum ratings</a> ). Updated: $I_{DSS}$ and $I_{GSS}$ values (test conditions) in <a href="#">Table 4: On/off states</a> . Updated: <a href="#">Section 4: Package mechanical data</a> . Minor text changes.

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