

<b>Title</b>	<b><i>Reference Design Report for a 10 W CV/CC USB Charger using LinkSwitch™-4 LNK4023D</i></b>
<b>Specification</b>	85 VAC – 265 VAC Input; 5 V, 2 A Output (End of USB Cable)
<b>Application</b>	Cell Phone / USB Charger
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	RDR-462
<b>Date</b>	August 02, 2016
<b>Revision</b>	1.2

### **Summary and Features**

- LinkSwitch-4
  - Primary side regulated (no optocoupler)
  - $\pm 3\%$  CV,  $\pm 5\%$  CC regulation
  - <30 mW no-load input power
  - Cable voltage drop compensation
  - Highly optimized BJT drive for low switching loss
  - Comfortably meets European CoC Tier 2, ENERGY STAR 2 and DoE-6 efficiency requirements

### PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.powerint.com](http://www.powerint.com). Power Integrations grants its customers a license under certain patent rights as set forth at <<http://www.powerint.com/ip.htm>>.

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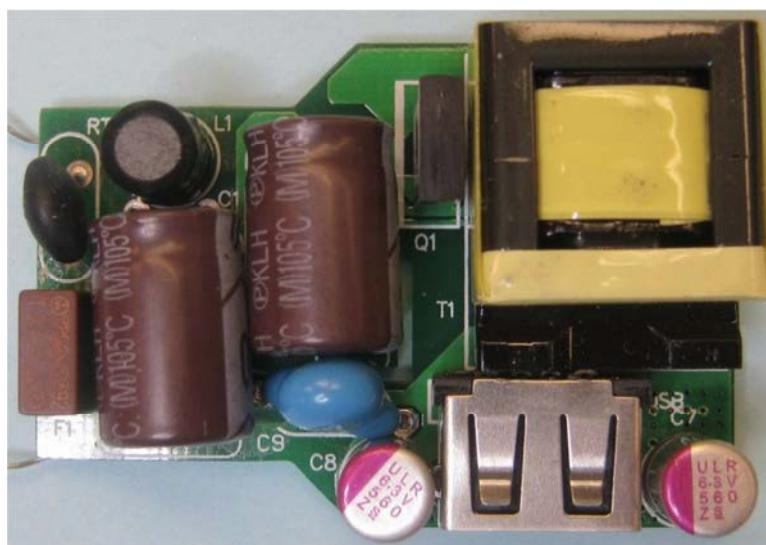
**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

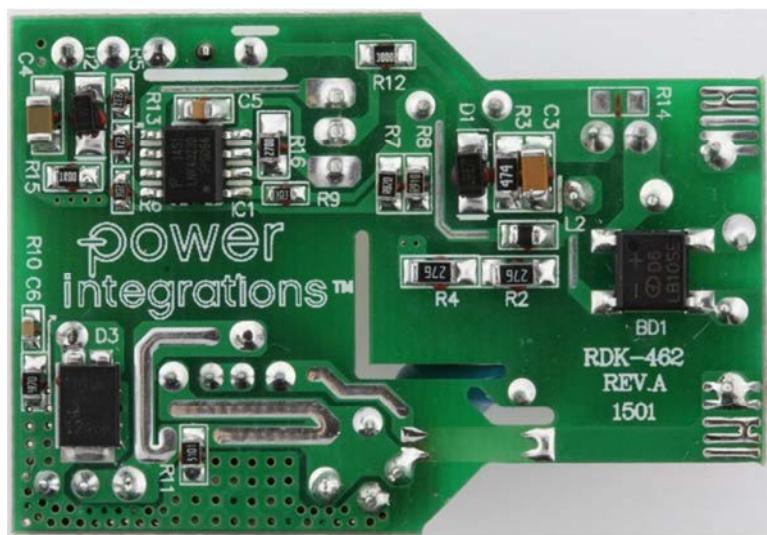
## 1 Introduction

This document is an engineering report describing a 2 A, 5.0 V USB charger utilizing a device from the LinkSwitch-4 family of ICs. This design is intended to show the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.



**Figure 1** – Populated Circuit Board Photograph, Top.



**Figure 2** – Populated Circuit Board Photograph, Bottom.



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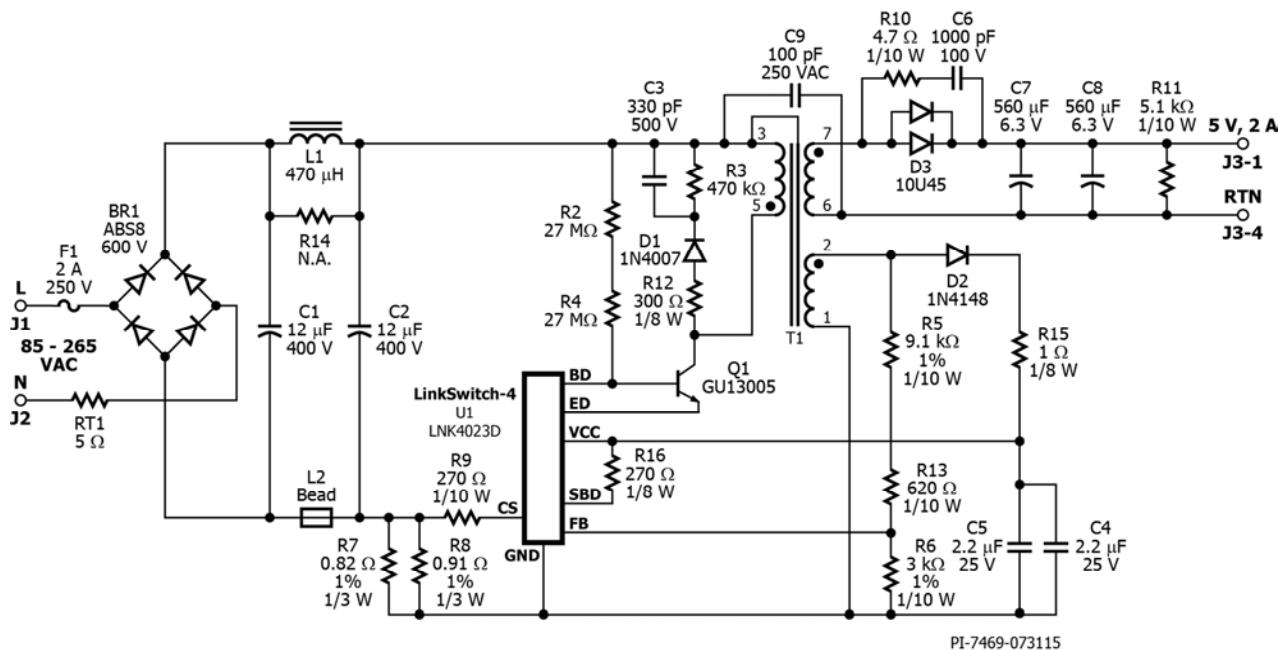
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## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	90		265	VAC	2 Wire – no P.E.
Frequency	$f_{LINE}$	50	50/60	64	Hz	
No-load Input Power				30	mW	230 VAC
<b>Output</b>						
Output Voltage	$V_{OUT}$	4.75	5.0	5.25	V	0-2 A; at end of 150 mΩ cable
Transient Output Voltage	$V_{OUT(T)}$	4.2		5.5	V	0 A - 2 A - 0 A load step end of cable
Output Ripple Voltage	$V_{RIPPLE}$	250		150	mV	At the end of the output cable
Output Cable Compensation	$V_{CBL}$	300		350	mV	At 2 A output current
Output Current CC point	$I_{OUT}$	2		2.5	A	
Auto-Restart Voltage	$V_{AR}$	2		3	V	At end of cable
Turn on Rise Time	$t_R$			10	ms	2.5 Ω load
Rated Output Power	$P_{OUT}$		10		W	
<b>Efficiency</b>						
Average	$\eta_{AVE[BRD]}$	82			%	Measured at PCB
25%, 50%, 75%, and 100% (Worst case of 115 and 230 VAC)	$\eta_{AVE[CBL]}$	79			%	With 0.30 V cable resistance drop
10%	$\eta_{10\%}$	75			%	
<b>Environmental</b>						
Output Cable Impedance	$R_{CBL}$		150		mΩ	
Conducted EMI			CISPR22B / EN55022B Load floating or grounded via artificial hand			Resistive load, 5 dB Margin
Safety			Connected to mobile phone and TV (MHL connection enabled)			5 dB Margin
Audible Noise			IEC950 / UL1950 Class II			Designed to meet
Line Surge: Common Mode (L1/L2-PE) Differential Mode (L1, L2)				35	dB	Measured at 3 cm, open frame
ESD		$\pm 16.5$		6	kV	Ring Wave, Common Mode: 12 Ω Combination wave, 2 Ω
		$\pm 8$		1	kV	Air discharge Contact discharge No degradation in performance
Ambient Temperature	$T_{AMB}$	0		40	°C	Free convection, sea level in sealed enclosure

### 3 Schematic



**Figure 3 – Schematic.**



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## 4 Circuit Description

### 4.1 Input EMI Filtering

Fuse F1 provides protection against catastrophic failure of components on the primary side.

An inrush-current limiting thermistor (RT1) protects bridge rectifier BR1 and limits inrush current.

Capacitor C1 and C2 provide filtering of the rectified AC input and together with inductor L1 and ferrite bead L2 attenuate differential mode EMI. A low value Y capacitor (C9) reduces common mode EMI.

#### 4.1 Primary

Component U1 is the controller IC and driver for the main high voltage switch, Q1, which is a very low-cost 700 V BJT.

A low cost RCD clamp formed by D1, R3, R12 and C3 limits the peak drain voltage due to the effects of transformer leakage inductance, and secondary trace inductances.

The IC and BJT together are self-starting. Resistor R2 and R4 provide a very low current into the base of Q1. This current is amplified at the emitter. The emitter current flows into the ED pin which during startup, charges up the VCC pin capacitor. When the VCC pin voltage reaches ~13.5 volts, the IC will go from sleep to initialize mode. In this mode a single short switching pulse is periodically applied to Q1 so as to enable the FB pin to sense the bulk capacitor voltage through the auxiliary winding and the combination of resistors R5 and R13. If the voltage is such that the current magnitude sensed is >1.05 mA, the IC will enter run mode and will switch Q1 continuously for the output to power up and run normally.

During normal operation, the VCC pin is powered by the auxiliary winding on the transformer. Output of the auxiliary winding is rectified by diode D2 and capacitor C4. Resistor R15 and capacitors C4 and C5 form a low pass filter that filters out any narrow voltage spikes.

Output voltage is sensed by the FB pin, through the auxiliary winding voltage, sampled at the end of the secondary conduction time, via voltage divider resistors R5, R13, and R6.

The primary current is sensed by the paralleled current sense resistors R7 and R8, through R9.

Output current regulation is achieved by sensing primary current and secondary conduction time.

---

Resistor R16 sets the supplementary base drive magnitude. This is extra base current at the beginning of the gate turn-on pulse to speed up turn-on of transistor Q1.

#### **4.2 Secondary**

The secondary of the transformer is rectified by diode D3 and filtered by capacitors C7 and C8. Peak voltage stress of diode D3 is reduced by snubber components R10 and C6 which damp the high frequency ringing during switching transients. This also reduces radiated EMI.

Resistor R11 provides a small (5 mW) pre-load to reduce the output voltage rise when load is < 10 mA.

The unit enters auto-restart when the sensed output voltage is lower than ~2.8 V.

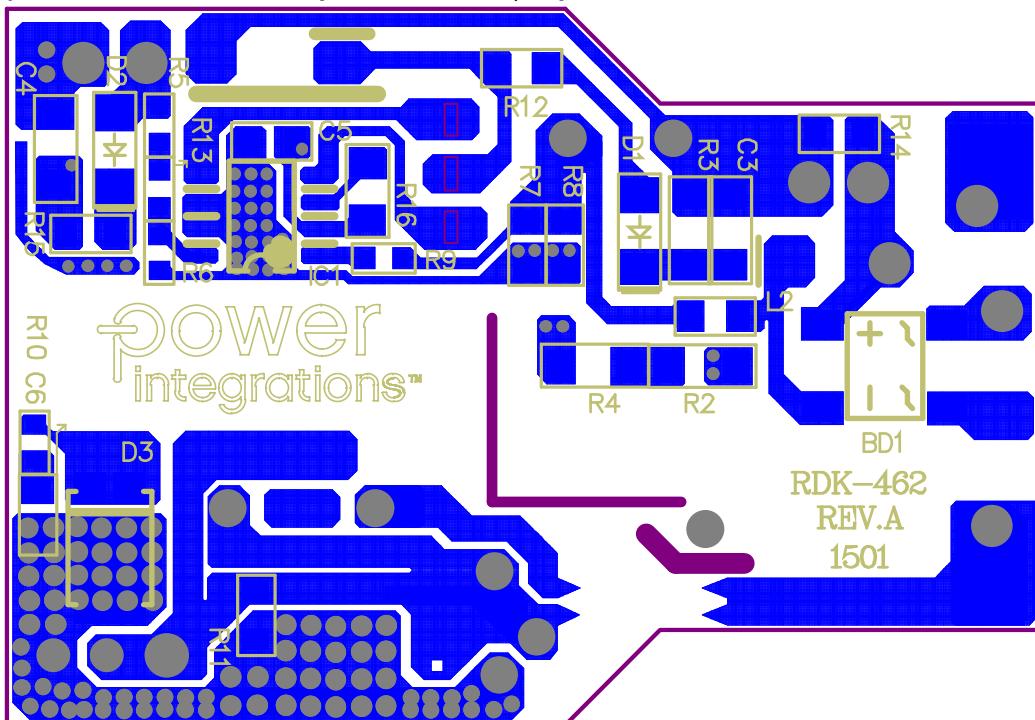


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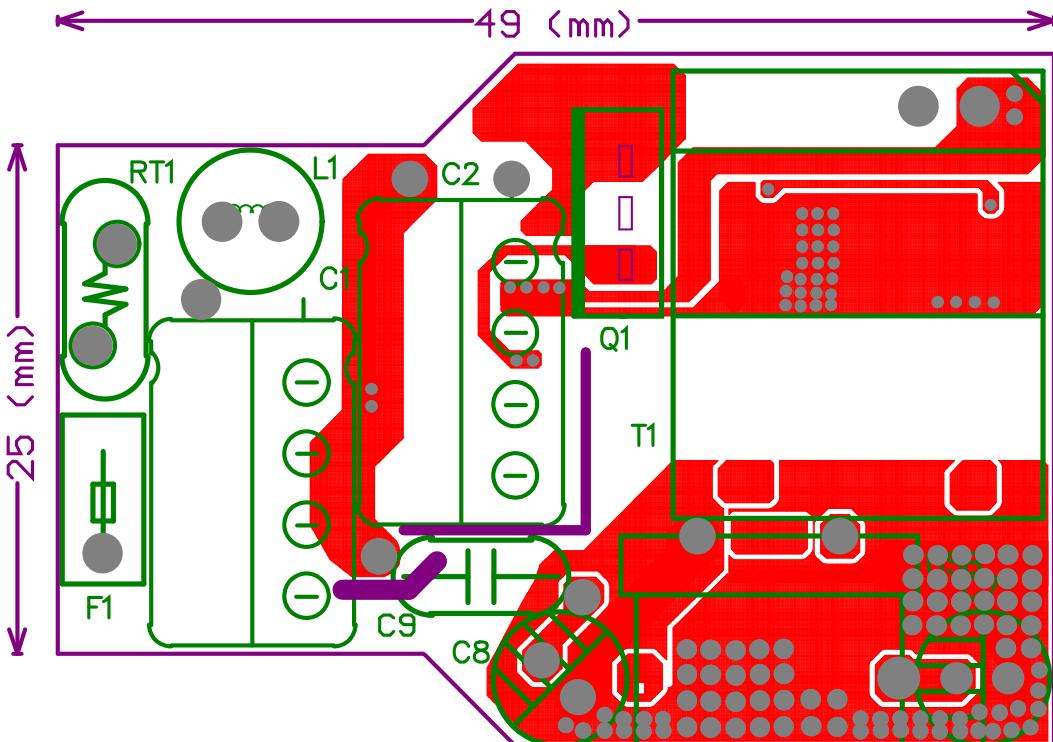
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## 5 PCB Layout

PCB copper thickness is 1 oz. (1.4 mils / 35 µm) unless otherwise stated.



**Figure 4** – Printed Circuit Layout, Top.



**Figure 5** – Printed Circuit Layout, Top.

## 6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, SMD, DFS	ABS8	Vishay
2	2	C1 C2	12 $\mu$ F, 400 V, Electrolytic, (8 x 16)	EKM126M2GF16RRS1P	Man-Yue Electronics
3	1	C3	330 pF, 500 V, Ceramic, X7R, 0805	C0805C331KCRACTU	Panasonic
4	1	C5	2.2 $\mu$ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
5	1	C4	2.2 $\mu$ F, 25 V Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
6	1	C6	1000 pF, 100 V, Ceramic, NPO, 0603	C1608COG2A102J	TDK
7	2	C7 C8	560 $\mu$ F, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
8	1	C9	100 pF, Ceramic, Y1	440LT10-R	Vishay
9	1	D1	1000 V, 1 A, Standard Recovery, SOD-123FL	1N4007	Micro Commercial
10	1	D2	75 V, 0.15 A, Switching, SOD-323	1N4148	Diodes, Inc.
11	1	D3	45 V, 10 A, Schottky, SMD, POWERD15	10U45	Diodes, Inc.
12	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
13	2	J1 J2	PCB Terminal Hole, #30 AWG	N/A	N/A
14	1	J3	CONN USB FEMALE TYPE A	USB-AF-DIP-094-H	GOLDCONN
15	1	L1	470 $\mu$ H, 0.120 A, 20%	RL-5480-1-470	Renco
16	1	L2	FERRITE CHIP 120 OHM 500 mA 0805	MMZ2012D121B	TDK
17	1	Q1	NPN, 450 V, 3.2 A, TO126	GU13005	Diodes, Inc.
18	2	R2 R4	27 M $\Omega$ , 5%, 1/4 W, Thick Film, 1206	RV1206JR-0727ML	Yageo
19	1	R3	470 k $\Omega$ , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic
20	1	R5	9.1 k $\Omega$ , 1%, 1/0 W, Thick Film, 0603	ERJ-3EKF9101V	Panasonic
21	1	R6	3 k $\Omega$ , 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3001V	Panasonic
22	1	R7	.82 $\Omega$ 1/3 W, 1%, Thick Film, 0805	RL1220S-R82-F	Susumu
23	1	R8	.91 $\Omega$ 1/3 W, 1%, Thick Film, 0805	RL1220S-R91-F	Susumu
24	1	R9	270 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ271V	Panasonic
25	1	R10	4.7 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R7V	Panasonic
26	1	R11	5.1 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ512V	Panasonic
27	1	R12	300 $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
28	1	R13	620 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ621V	Panasonic
29	1	R14	Not Populated		
30	1	R15	1 $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ1R0V	Panasonic
31	1	R16	270 $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ271V	Panasonic
32	1	RT1	NTC Thermistor, 5 $\Omega$ , 1.0 A	SL05 5R001	Ametherm
33	1	T1	Bobbin: EPC1716D – Horizontal- 7 pins (5/2) Transformer	EPC1716D PNK-40230	SunTech Premier Magnetics
34	1	U1	LNK4023D	LinkSwitch-4	Power Integrations

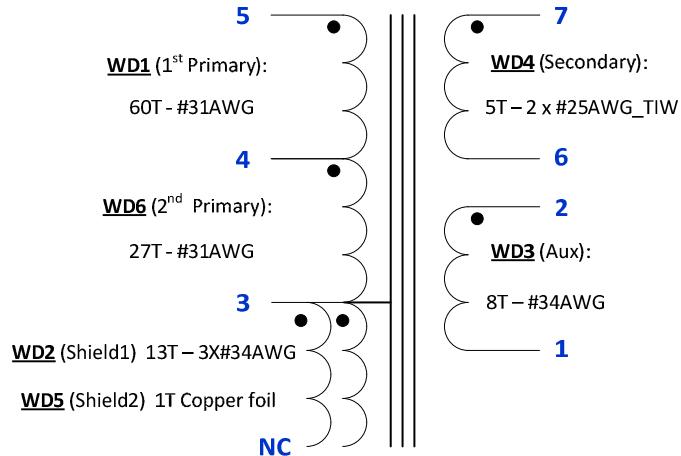


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## 7 Transformer Specification

### 7.1 Electrical Diagram



**Figure 6** –Transformer Electrical Diagram.

### 7.2 Electrical Specifications

<b>Electrical Strength</b>	1 second, 60 Hz, from pins 1- 5 to pins 6-7.	3000 VAC
<b>Primary Inductance</b>	Pins 3-5, all other open, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	1.05 mH ±5%
<b>Resonant Frequency</b>	Pins 3-5, all other open.	700 kHz (min.)
<b>Primary Leakage</b>	Pins 3-5, with 8-6-7 shorted, measured at 100 KHz, 0.4 V <sub>RMS</sub> .	25 µH (max.)

### 7.3 Materials

Item	Description
[1]	Core: EPC1716D.
[2]	Bobbin: EPC1716D – Horizontal- 7 pins (5/2).
[3]	Magnet wire: #31 AWG Solderable Double Coated.
[4]	Magnet wire: #34 AWG Solderable Double Coated.
[5]	Magnet wire: #25 AWG Heavy Nyleze – Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mil thick, 8.0 mm wide.
[7]	Copper Foil: 2 mils thick, 7.5 mm wide.
[8]	Bus wire: #24 AWG, Belden Electronics Div.
[9]	Varnish: Dolph BC-359.

## 7.4 Transformer Build Diagram

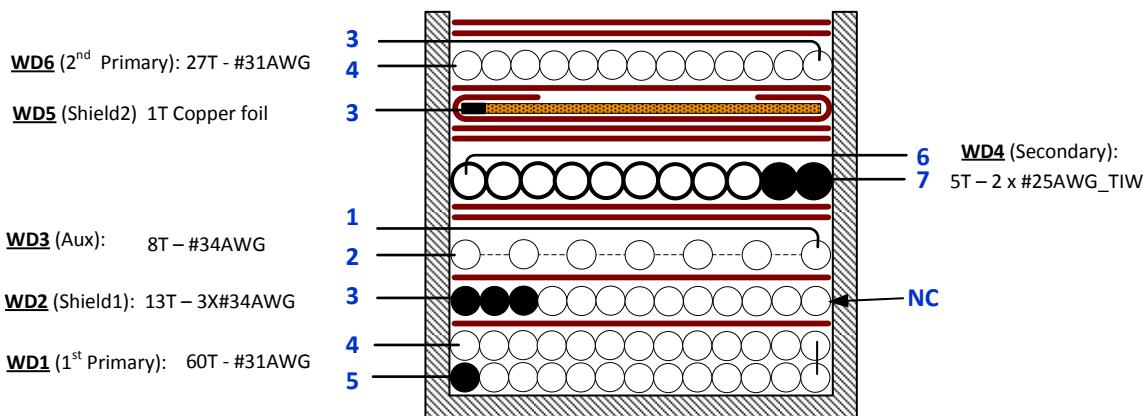


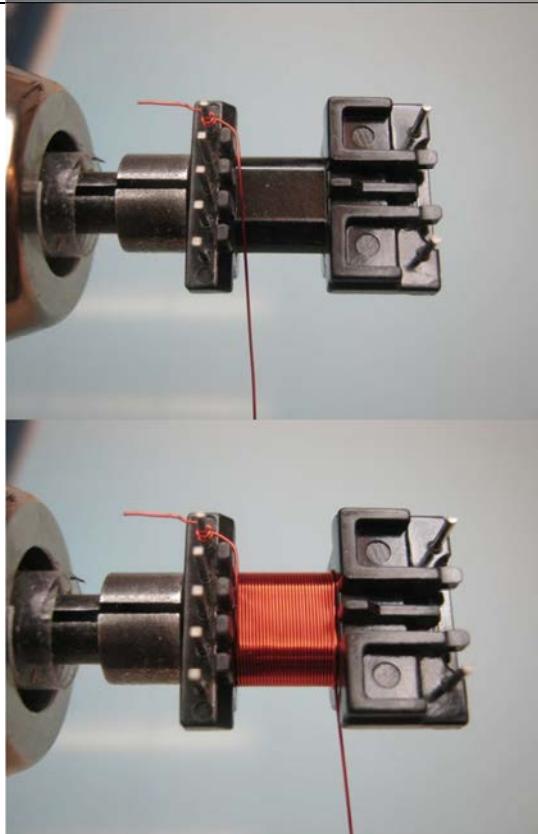
Figure 7 – Transformer Build Diagram.

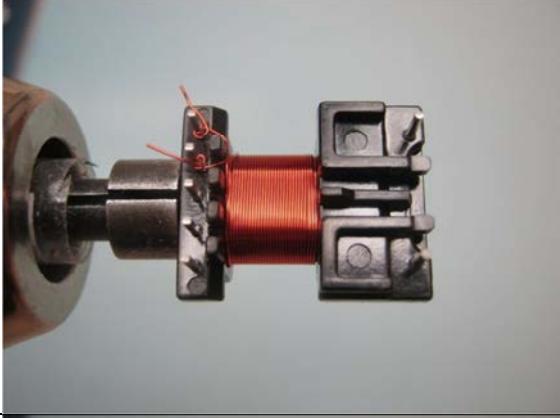
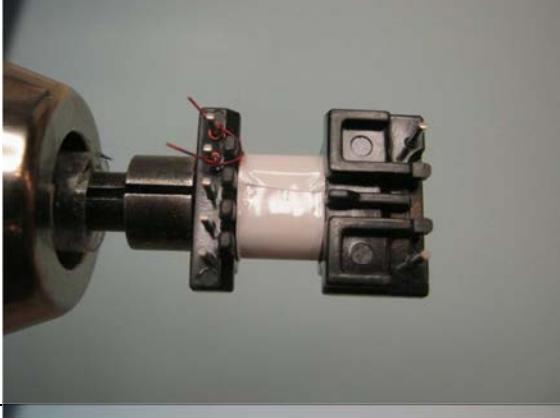
## 7.5 Transformer Construction

<b>Winding Preparation</b>	Position the bobbin item [2] on the mandrel such that the pin side is on the left side of bobbin mandrel. Winding direction is clock-wise direction.
<b>WD1 1<sup>st</sup> Primary</b>	Start at pin 5, wind 60 turns of wire item [3] in 2 layers with tight tension, and finish at pin 4.
<b>Insulation</b>	Place 1 layer of tape item [6].
<b>WD2 Shield 1</b>	Start at pin 3, wind 13 tri-filar turns of wire item [4] in 1 layer. At the last turn, cut short for non-connection.
<b>Insulation</b>	Place 1 layer of tape item [6].
<b>WD3 Aux</b>	Start at pin 2, wind 8 turns of wire item [4] in 1 layer, spread the wire evenly on the bobbin, and bring the wire back to terminate at pin 1.
<b>Insulation</b>	Place 2 layers of tape item [6].
<b>WD4 Secondary</b>	Start at pin 7, wind 5 bi-filar turns of wire item [5] in 1 layer with tight tension and bring the wire back to finish at pin 6.
<b>Insulation</b>	Place 2 layers of tape item [6].
<b>WD5 Shield 2</b>	Use copper foil item [7] to prepare for shield winding, (see illustration below). Start at pin 3, wind 1turn, and leave no connect at the end.
<b>Insulation</b>	Place 1 layer of tape item [6].
<b>WD6 2<sup>nd</sup> Primary</b>	Start at pin 4, wind 27 turns of wire item [3] in 1 layer with tight tension, and bring the wire back to finish at pin 3.
<b>Insulation</b>	Place 2 layers of tape item [6] to secure windings and for insulation.
<b>Finish</b>	Gap core halves for 1.05 mH inductance. Wrap core halves and bus wire item [8] which connected to pin 3 with tape, (see illustration below). Varnish with item [9].

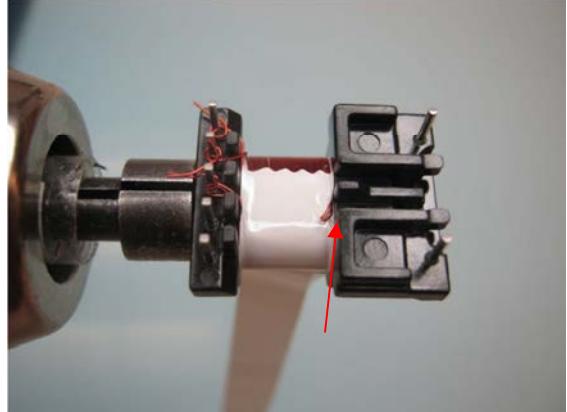
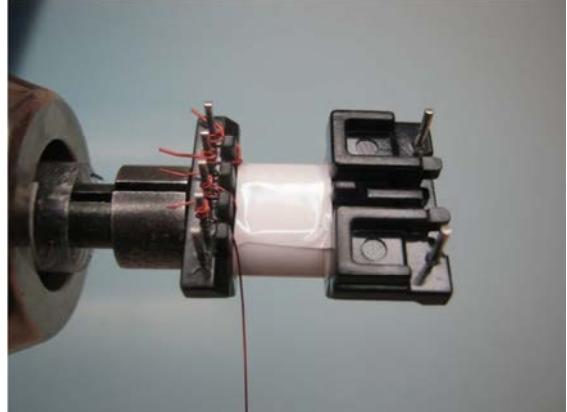


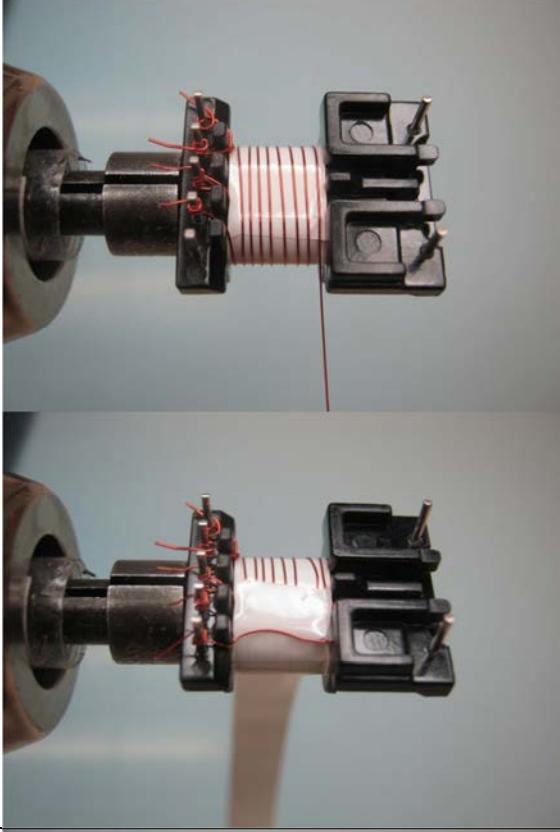
## 7.6 Transformer Illustrations

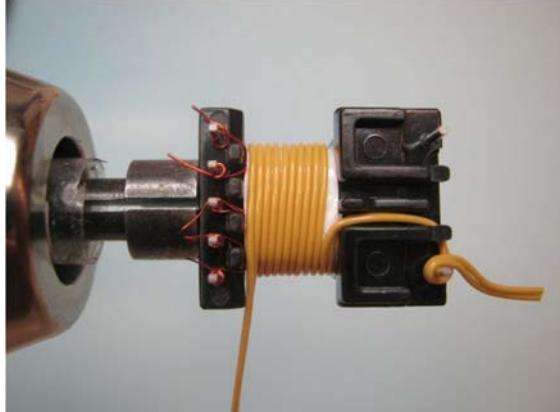
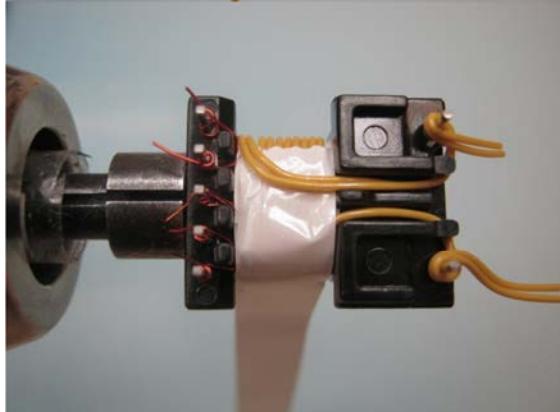
<b>Winding Preparation</b>	 A photograph showing a transformer bobbin mounted on a mandrel. A yellow curved arrow points downwards from the right side of the bobbin, indicating the clockwise winding direction.	Position the bobbin item [2] on the mandrel such that the pin side is on the left side of bobbin mandrel. Winding direction is clockwise direction as viewed from the right.
<b>WD1 1<sup>st</sup> Primary</b>	 Two photographs illustrating the primary winding process. The top image shows the start of the winding at pin 5. The bottom image shows the completed primary winding with 60 turns of red wire wound in two layers on the bobbin.	Start at pin 5, wind 60 turns of wire item [3] in 2 layers with tight tension, and finish at pin 4.

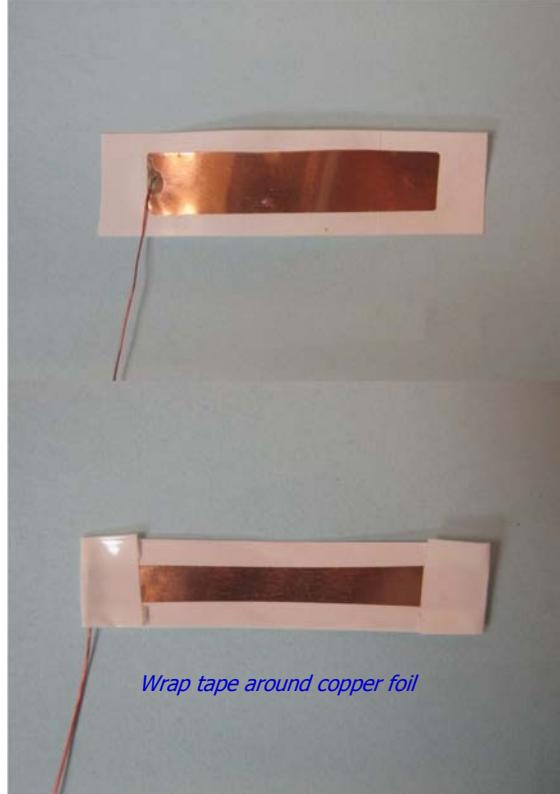
		
<b>Insulation</b>		Place 1 layer of tape item [6].
<b>WD2 Shield 1</b>	 	Start at pin 3, wind 13 trifilar turns of wire item [4] in 1 layer. At the last turn, cut short for non-connection.

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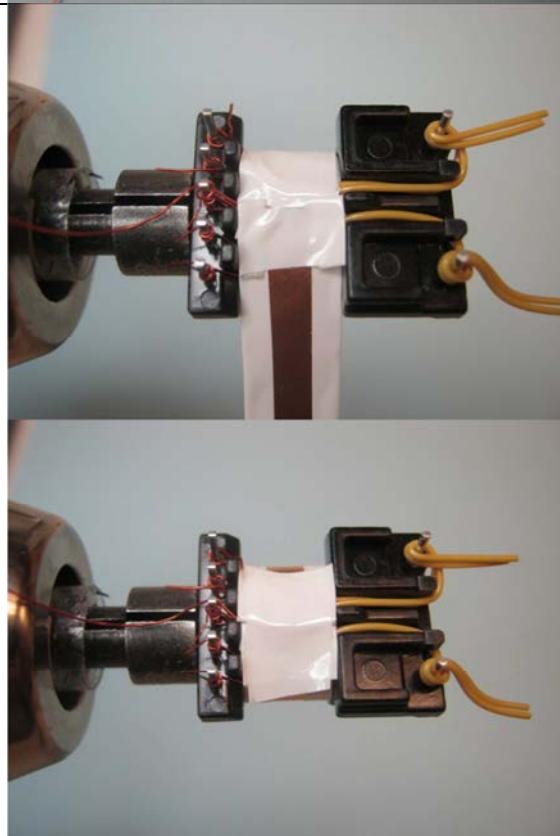
	 cut end of winding (arrow)	
<b>Insulation</b>		Place 1 layer of tape item [6].
<b>WD3 Aux</b>		Start at pin 2, wind 8 turns of wire item [4] in 1 layer, spread the wire evenly on the bobbin, and bring the wire back to terminate at pin 1.

		
<b>Insulation</b>		Place 2 layers of tape item [6].
<b>WD4 Secondary</b>		Start at pin 7, wind 5 bi-filar turns of wire item [5] in 1 layer with tight tension and bring the wire back to finish at pin 6.

		
		<p>Place 2 layers of tape item [6].</p>
<b>Insulation</b>		
<b>WD5 Shield 2</b>		<p>Use copper foil item [7] to prepare for shield winding, (see illustration).</p>

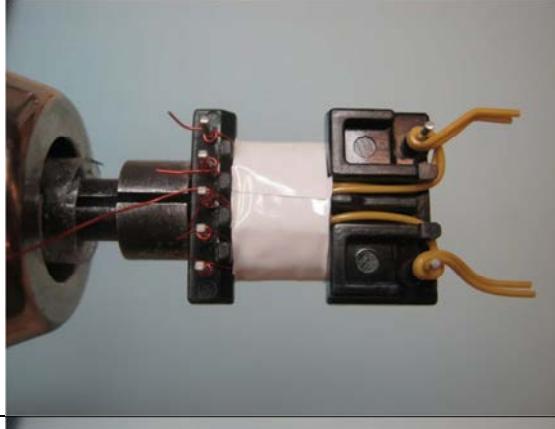
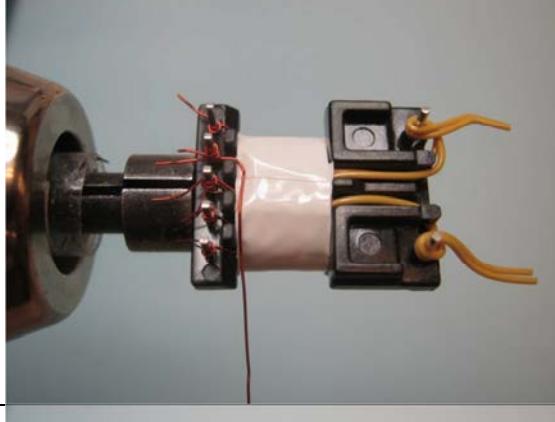
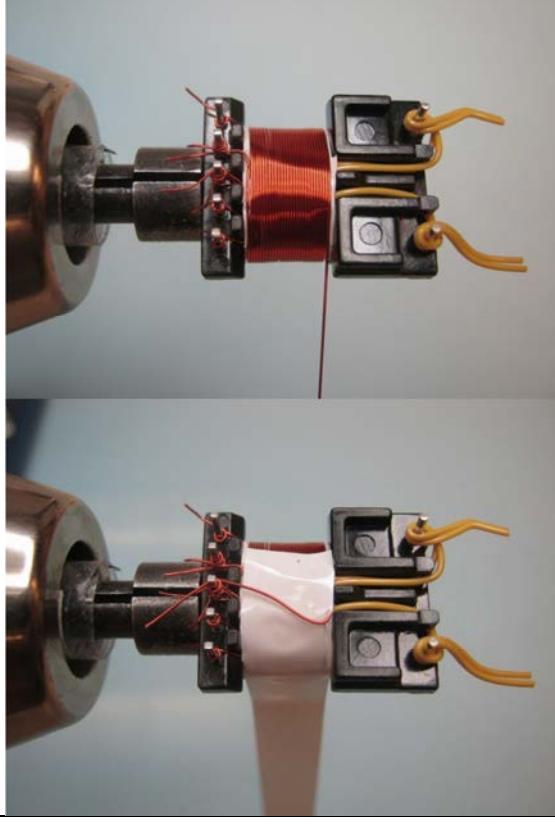


**WD5  
Shield 2  
(Cont'd)**



Start at pin 3, wind 1 turn,  
and leave no connect at  
the end.



<b>Insulation</b>		Place 1 layer of tape item [6].
<b>WD6 2<sup>nd</sup> Primary</b>		Start at pin 4,
<b>WD6 2<sup>nd</sup> Primary (Cont'd)</b>		wind 27 turns of wire item [3] in 1 layer with tight tension, and bring the wire back to finish at pin 3.

<b>Insulation</b>		Place 2 layers of tape item [6] to secure windings and for insulation.
<b>Finish</b>		Gap core halves for 1.05mH inductance. Wrap 2 layers of tape item [9] around the bottom of secondary core half.
		Wrap core halves and <u>bus wire item [8]</u> which connected to pin 3 with tape, (see illustration below). Varnish with item [10].



## 8 Transformer Design Spreadsheet

LinkSwitch-4_121914: LinkSwitch-4 Discontinuous Flyback Transformer Design Spreadsheet					
<b>ENTER APPLICATION VARIABLES</b>					
VACMIN	90		90	Volts	Minimum AC Input Voltage
VACMAX			265	Volts	Maximum AC Input Voltage
fL			50	Hertz	AC Mains Frequency
VO			5.00	Volts	Output Voltage at the end of the cable
VO_PCB			5.30	Volts	Output Voltage at PCB
IO	2.25		2.25	Amps	Nominal output current during CC
PO			11.93	Watts	Typical output power including cable drop compensation
n			0.80	%/100	Efficiency Estimate
Z			0.50		Loss allocation factor
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	24.0		24.0	uFarads	Total input bulk Capacitance
<b>ENTER LINKSWTCH-4 VARIABLES</b>					
LinkSwitch-4	LNK40X3D				Select LNK-4
Cable drop compensation option	6%		6%		Select level of cable drop compensation
DEVICE		Info	LNK4023D		Output Power is greater than datasheet PO for this part number. Please verify performance on bench or select a bigger part
VCS_MIN	73		73	mV	Selection of Vcsmin
RCS2			270	Ohm	Resistance that corresponds to the selected Vcsmin
FSW			65000	Hertz	LinkSwitch-4 typical switching frequency
FSW_MIN			60000	Hertz	LinkSwitch-4 minimum switching frequency
FSW_MAX			70000	Hertz	LinkSwitch-4 maximum switching frequency
ILIM_MAX			0.90	A	Maximum emitter pin sink current
VCS_TARGET	0.288		0.288	Volts	Target Vcs under normal operation at VMIN (leave as default if no better info available)
RCS			0.432	Ohm	Calculated RCS value
<b>Transistor</b>					
PART_NUMBER			TS13005		Example transistor for the current application
HFE_NOLOAD	40		40		Minimum DC current gain at no load
HFE	20		20		Minimum DC current gain for load transient
VSWMAX			700	Volts	Switch Breakdown voltage
v_CGND_ON			3.0	Volts	BJT + LNK-4 on-state Collector to ground Voltage (3V if no better information available)
<b>Additional Parameters</b>					
<b>Startup</b>					
STARTUP_TIME			1.00	second	Desired startup time
R_STARTUP	54.00		54.00	MOhm	Startup resistor (default calculation assumes a standard resistor for 1 second desired startup)
STARTUP_TIME_FINAL			0.98	second	Final startup time assuming resistor value Rstartup
<b>Dummy load and no load</b>					
R_PRELOAD	5100		5100	Ohm	Pre load resistor (1%)
P_PRELOAD			5.51	mW	Preload resistor power consumption at no load
FSW_NOLOAD			1121	Hz	Estimated switching frequency at no load
<b>Load step and undershoot</b>					
RCABLE_EST			0.133	Ohm	Estimated charger cable resistance
I_LOADSTEP	2.00		2.00	A	Required maximum current load step from zero load
V_UNDERSHOOT			4.20	V	Accepted undershoot during maximum load step

FSW_UNDERSHOOT		<i>Info</i>	3348	Hz	Fsw_noload may be lower than the minimum frequency required to fulfill the undershoot specification. This test does not include standard 47uF capacitance at end of cable. Verify performance or try to increase the pre load, increase Cout, or lower VCSmin
<b>Feedback Resistors</b>					
V_UV+	115.00		115.00	V	DC voltage at which power supply will start up
RFB1			10000	Ohm	Initial estimate for top feedback resistor (std value, use 1% tolerance)
RFB2			2800	Ohm	Initial estimate for bottom feedback resistor (std value, use 1% tolerance)
<b>Output Capacitor</b>					
LOAD_TYPE	<b>Resistive Load</b>		Resistive Load		Select load type for startup testing. This will help estimate the maximum output capacitance that will allow proper startup under any normal operating conditions
IONOM		<i>Info</i>	1.91	A	Input is not applicable for this load type
R_LOAD			2.36	Ohm	Equivalent resistive load placed at the end of PCB for simulating load and cable
COUT ADVISED			854	uF	Maximum Cout to guarantee proper startup and stability
COUT_FINAL	1120	<i>Warning</i>	1120	uF	Output capacitance may be too high for proper startup. Please verify on bench
<b>ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES</b>					
<b>Core Type</b>	<b>EPC17</b>		EPC17		Core Type
Custom Core (Optional)					If Custom core is used - Enter Part number here
Bobbin		EPC17_BOBBIN		P/N:	BEPC-17-1110CPH
AE			0.23	cm^2	Core Effective Cross Sectional Area
LE			4.02	cm	Core Effective Path Length
AL			1150	nH/T^2	Ungapped Core Effective Inductance
BW			9.55	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of Primary Layers
F_RES			400	kHz	Anticipated resonant frequency on the primary side (180<Ftrf<1200)
<b>Turns Ratio / Secondary turns</b>					
VOR	99.00		99.00	Volts	Reflected Output Voltage
NS	5		5		Number of Secondary Turns
<b>Bias/Feedback Winding</b>					
NB			8	Turns	Suggested number of turns for the bias / feedback winding
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
VB_NOLOAD	7.50		7.50	Volts	Desired Bias voltage at no load
PB_NOLOAD			4.43	mW	Bias winding power consumption estimate at no load
VB_NOLOAD_MEASUR ED			7.50	Volts	Measured Bias voltage at no load
<b>Bias Capacitor</b>					
CBIAS	2.20		2.20	uF	Auxiliary capacitor. Default value assumes 1V of ripple on bias winding.
DELTAV_BIAS			243	mV	Voltage ripple on bias winding capacitor (should be between 0.05V and 1.6V)
<b>DC INPUT VOLTAGE PARAMETERS</b>					
VMIN	100		100	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
<b>CURRENT WAVEFORM SHAPE PARAMETERS</b>					
DMAX			0.41		Maximum Duty Cycle (calculated at VMIN)
IAVG			0.15	Amps	Average Primary Current (calculated at VMIN)



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IP			0.67	Amps	Peak Primary Current (calculated at full load, VMIN)
IP_TRANSIENT			0.81	Amps	Max Peak Primary Current during a load transient
IRMS			0.27	Amps	Primary RMS Current (calculated at VMIN)
KDP			1.45		Average ratio of primary switch off time to secondary output diode conduction time (1.0 < KDP < 6.0)
<b>TRANSFORMER PRIMARY DESIGN PARAMETERS</b>					
LP			1050	uHenries	Typical Primary Inductance
LP Tolerance	5		5		Tolerance of Primary Inductance
NP			87		Primary Winding Number of Turns
ALG			139	nH/T^2	Gapped Core Effective Inductance
BM		Warning	3544	Gauss	Operating flux density should be below 3000 Gauss, Increase turns OR increase core size
BP		Warning	4507	Gauss	!!! REDUCE BP < 4200 (increase NS, smaller LINKSwitch, larger Core, increase KP)
BAC			1772	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1614		Relative Permeability of Ungapped Core
LG			0.18	mm	Gap Length (Lg > 0.1 mm)
BWE			19.1	mm	Effective Bobbin Width
OD	0.23		0.23	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.18	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			51	Cmils	Bare conductor effective area in circular mils
CMA		Warning	190	Cmils/A mp	!!! INCREASE CMA > 200 (increase L(primary layers), decrease NS, larger Core)
Primary Current Density (J)			10.48	Amps/m m^2	!!! Decrease current density Use larger wire diameter, increase L or increase core size.
<b>SECONDARY DESIGN PARAMETERS</b>					
VO			5.30	Volts	Output Voltage (at PCB)
IO			2.25	Amps	Average Power Supply Output Current
VD			0.40	Volts	Output Winding Diode Forward Voltage Drop
PIVS			27	Volts	Output Rectifier Maximum Peak Inverse Voltage
ISP			11.65	Amps	Peak Secondary Current
ISRMS			4.61	Amps	Secondary RMS Current
IRIPPLE			4.03	Amps	Output Capacitor RMS Ripple Current
CMS			922	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.81	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.91	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.55	mm	Maximum Secondary Insulation Wall Thickness
<b>VOLTAGE STRESS PARAMETERS</b>					
SWITCH_DERATING			0.10	%/100	Desired derating factor for switch
VDRAIN			603	Volts	Maximum Collector Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			36	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			56	Volts	Bias Rectifier Maximum Peak Inverse Voltage
<b>NO LOAD POWER ESTIMATOR</b>					
EFF_NOLOAD			0.60	%/100	Assumed efficiency at no load (0.6 if no better data available)
VAC_INPUT			230	Volts	AC input voltage for no load power estimation

PB_NOLOAD			4.43	mW	Bias winding power consumption estimate at no load
P_PRELOAD			5.51	mW	Preload resistor power consumption at no load
P_STARTUPRES			1.96	mW	Energy dissipated by the startup resistor
C_CLAMP				nF	Clamp capacitor (if clamp capacitor not defined then it will be assumed that clamp dissipation is 10% of estimated switching losses)
C_PARASITIC				pF	Estimated primary side parasitic capacitance. If no value entered the primary resonant frequency will be used to estimate this parameter assuming LPTYP
PSW			6.96	mW	Power losses of the switch and clamp
P_NOLOAD_TOTAL			25.47	mW	Estimated no load power consumption



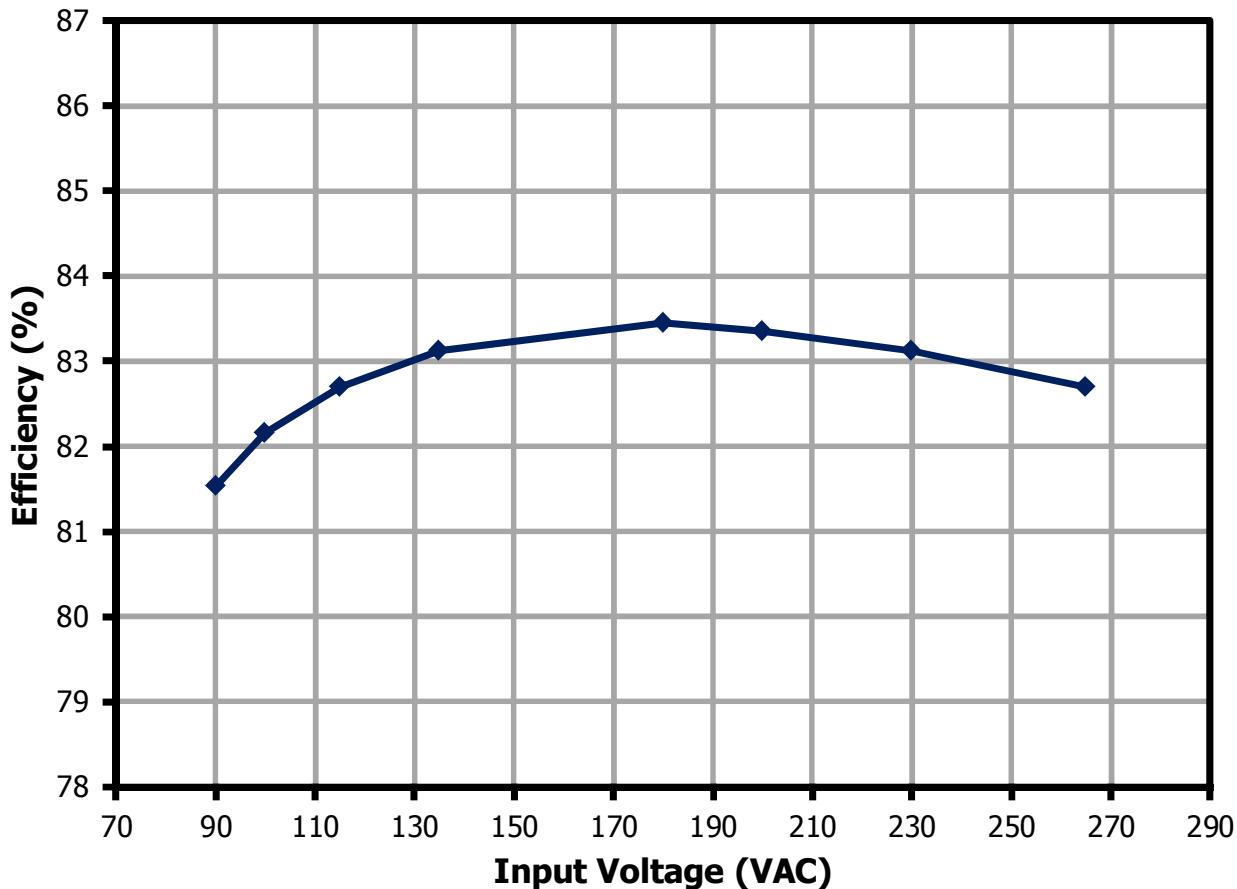
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## 9 Performance Data

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

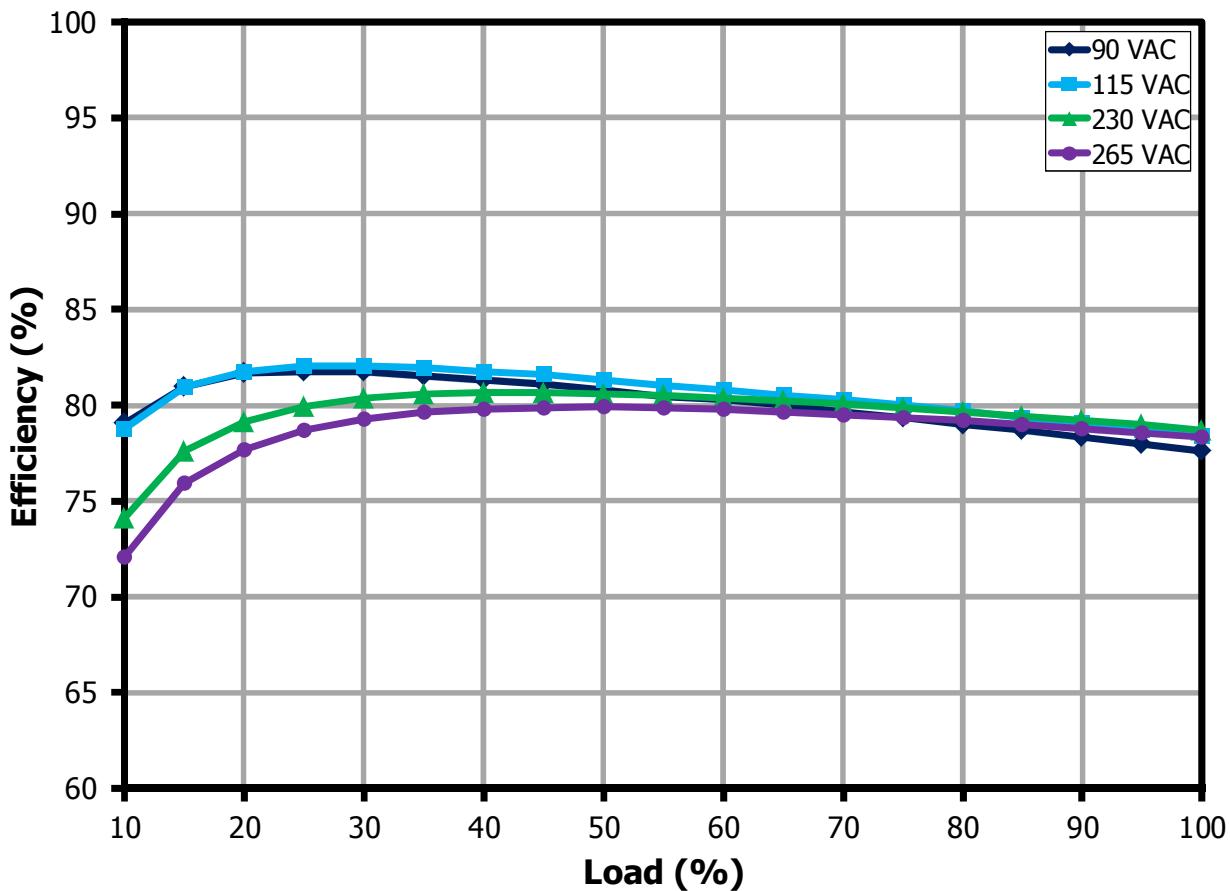
### 9.1 *Active Mode Efficiency (at PCB) vs. Line Voltage*



**Figure 8 – Full Load Efficiency vs. Line Voltage, Room Temperature.**

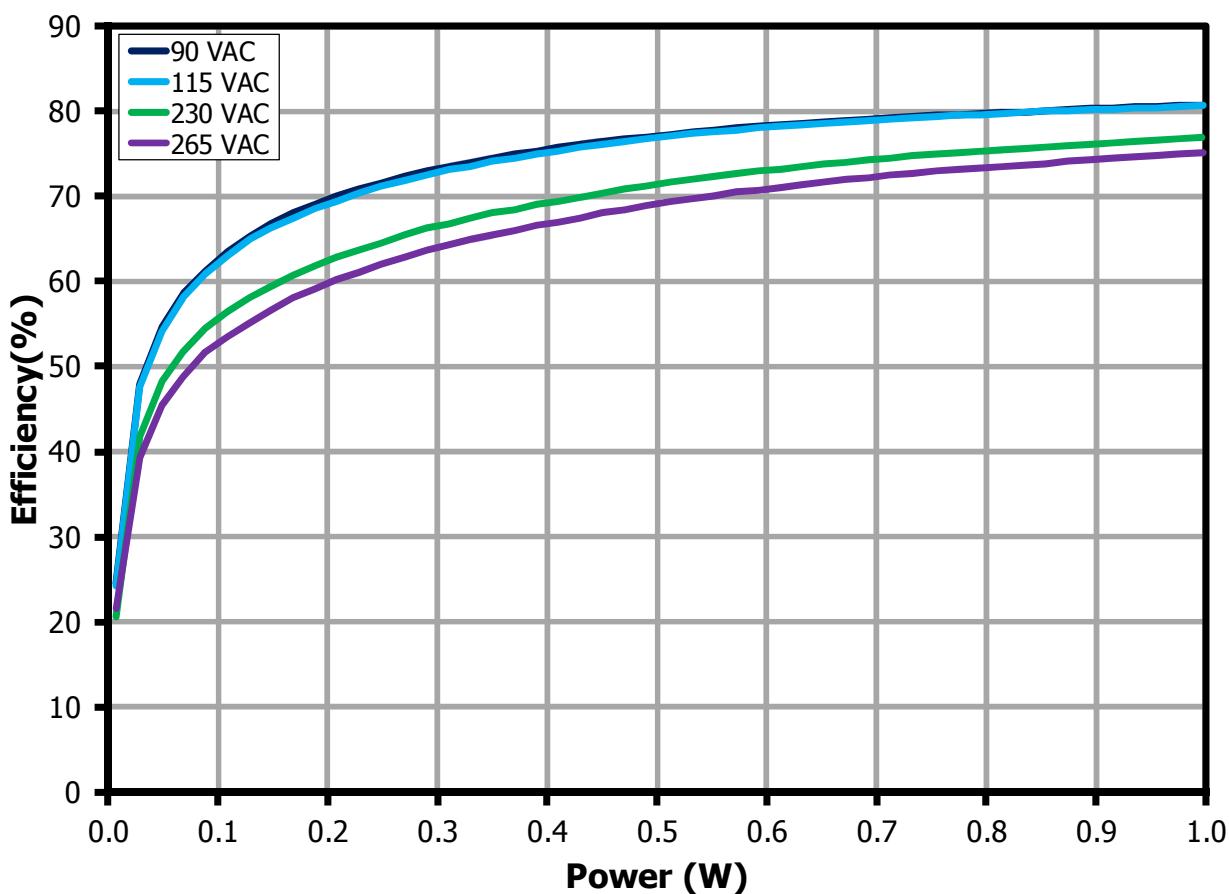
## 9.2 Active Mode Efficiency (at End of Cable) vs. Load

### 9.2.1 Efficiency vs. Load



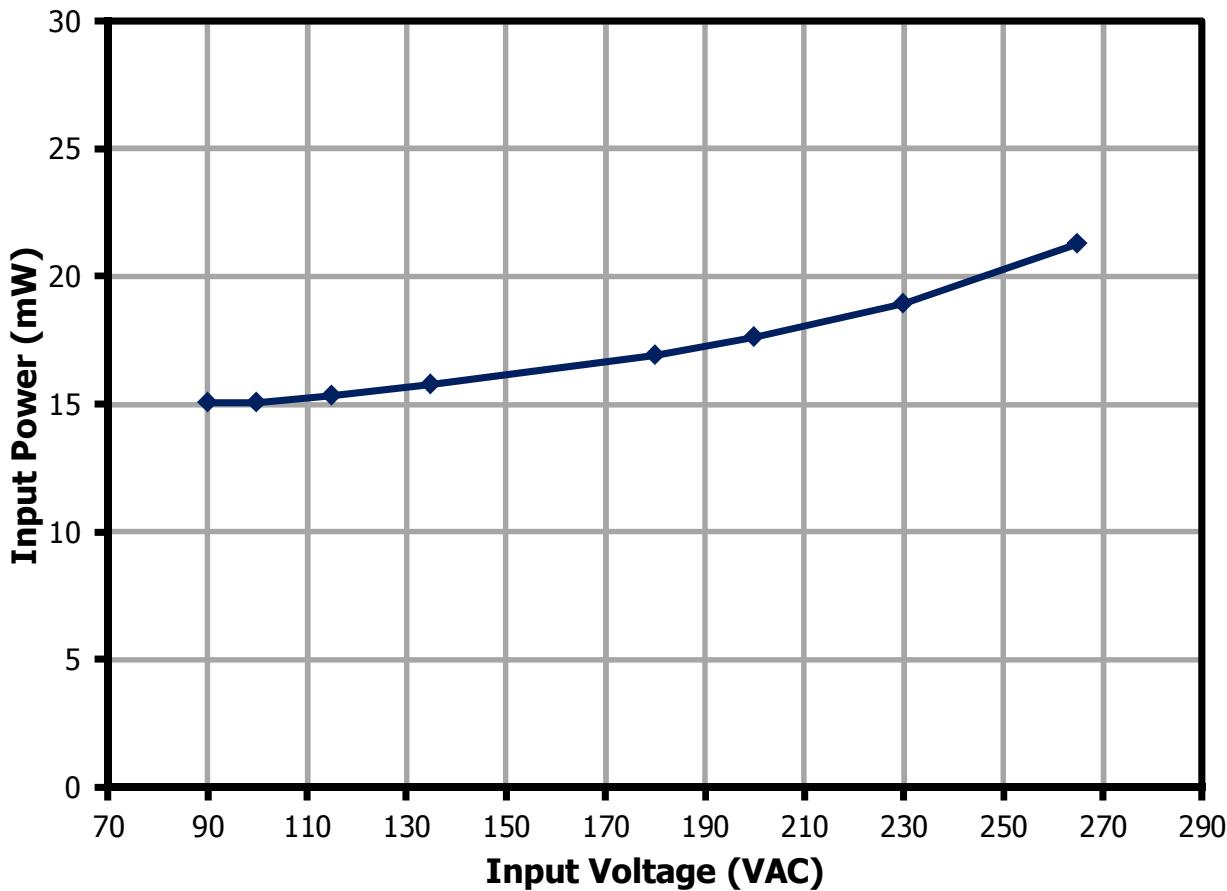
**Figure 9 – Efficiency vs. Load, Room Ambient.**

### 9.2.2 *Efficiency vs. Light Load (at PCB)*



**Figure 10** – Efficiency vs. Load (Expanded to Show Light Load Performance).

### 9.3 *No-Load Input Power*



**Figure 11** – No Load Input Power vs. Input Line Voltage, Room Temperature.

## 9.4 Average Efficiency

### 9.4.1 Average Efficiency at PCB

#### 9.4.1.1 Average Efficiency at PCB at 115 VAC Input

Load (%)	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>OUT</sub> (W)	P <sub>IN</sub> (W)	Efficiency (%)	Average Efficiency (%)
100	2.001	5.116	10.232	12.381	82.64	
75	1.502	5.081	7.622	9.166	83.15	
50	1.001	5.048	5.048	6.054	83.38	
25	0.500	5.008	2.504	3.013	83.11	<b>83.07</b>
<b>10</b>	0.200	4.988	0.9976	1.236	<b>80.71</b>	

#### 9.4.1.2 Average Efficiency at PCB at 230 VAC Input

Load (%)	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>OUT</sub> (W)	P <sub>IN</sub> (W)	Efficiency (%)	Average Efficiency (%)
100	2.001	5.115	10.23	12.289	83.25	
75	1.502	5.081	7.622	9.157	83.23	
50	1.001	5.046	5.046	6.091	82.84	
25	0.5	5.012	2.506	3.081	81.34	<b>82.66</b>
<b>10</b>	0.2	4.991	.9982	1.296	<b>77.02</b>	

## 9.4.2 Average Efficiency at End of Cable

### 9.4.2.1 Efficiency Requirements at End of Cable

Test	Average	Average	Average	Average	10% Load	10% Load
<b>Model</b>	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
<b>Effective</b>	Now	2016	Now	2016	Now	2016
<b>Standard</b>	<b>Energy Star 2</b>	<b>New IESA2007</b>	<b>CoC v5 Tier 1</b>	<b>CoC v5 Tier 2</b>	<b>CoC v5 Tier 1</b>	<b>CoC v5 Tier 2</b>
<b>Efficiency</b>	<b>74.2%</b>	<b>78.7%</b>	<b>76.0%</b>	<b>79.0%</b>	<b>66.6%</b>	<b>69.7%</b>

### 9.4.2.2 Average Efficiency at End of 6% Cable at 115 VAC Input

Load (%)	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>OUT</sub> (W)	P <sub>IN</sub> (W)	Efficiency (%)	Average Efficiency (%)
100	2.001	4.778	9.556	12.393	77.11	
75	1.502	4.825	7.238	9.175	78.88	
50	1.001	4.877	4.877	6.060	80.48	
25	0.500	4.927	2.464	3.017	81.65	<b>79.53</b>
<b>10</b>	0.200	4.958	0.992	1.238	<b>80.10</b>	

### 9.4.2.3 Average Efficiency at End of 6% Cable at 230 VAC Input

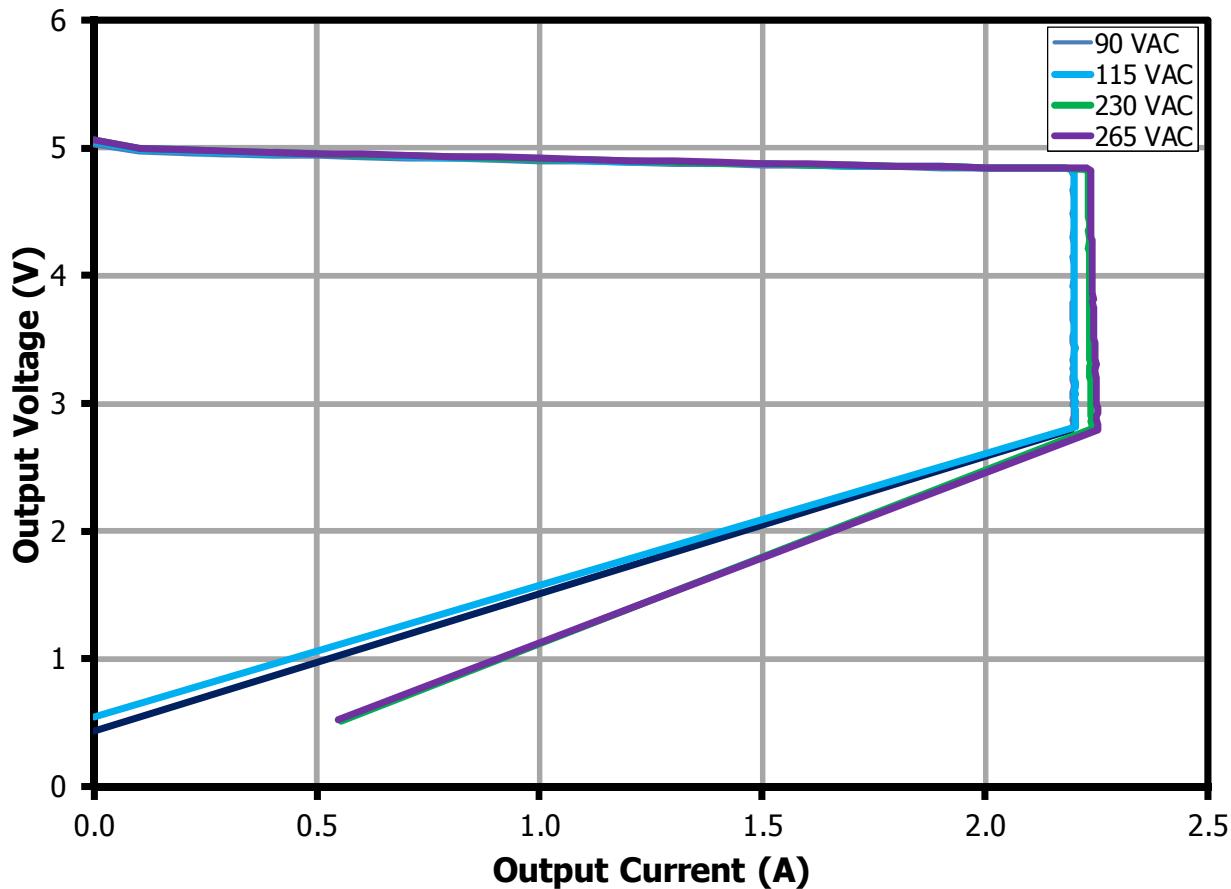
Load (%)	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>OUT</sub> (W)	P <sub>IN</sub> (W)	Efficiency (%)	Average Efficiency (%)
100	2.001	4.786	9.572	12.312	77.75	
75	1.502	4.834	7.251	9.188	78.92	
50	1.001	4.879	4.879	6.103	79.94	
25	0.5	4.925	2.463	3.084	79.85	<b>79.11</b>
<b>10</b>	0.2	4.953	0.991	1.298	<b>76.32</b>	



### 9.5 CV/CC Regulation Measured at the End of Cable

Measured at end of simulated 6% cable using 150 mΩ resistor

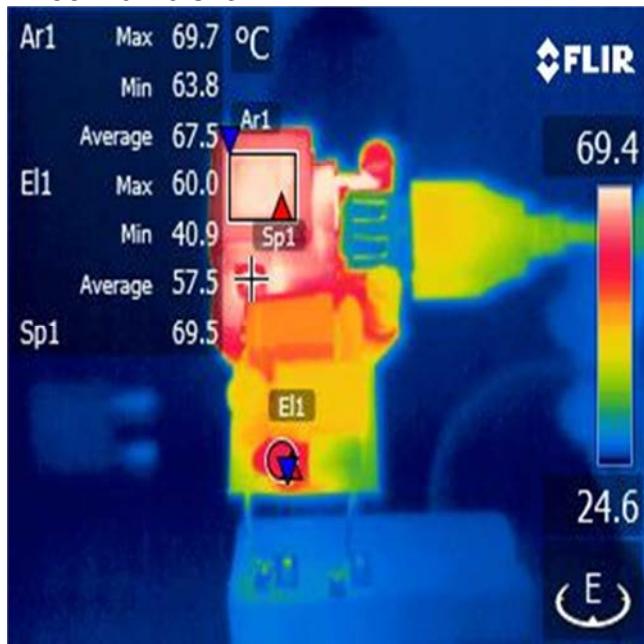
NOTE: Unit auto-restarts < ~2.8 V.



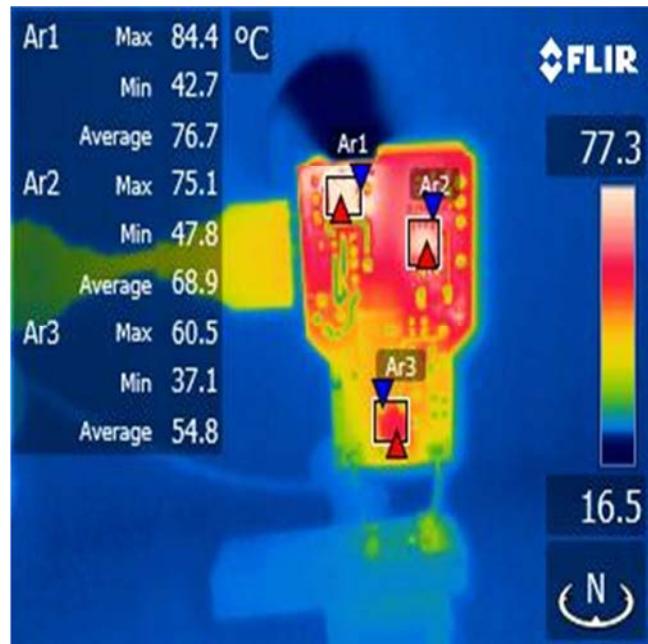
**Figure 12 –** Output Voltage vs, Output current, Room Temperature.

## 10 Open Case Thermal Performance

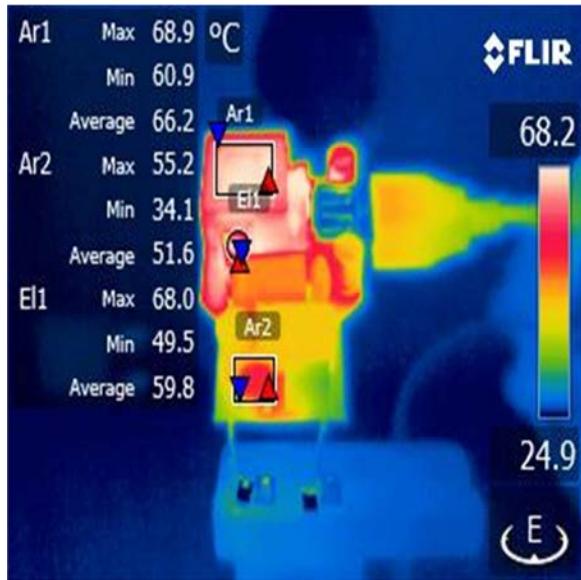
Room ambient.



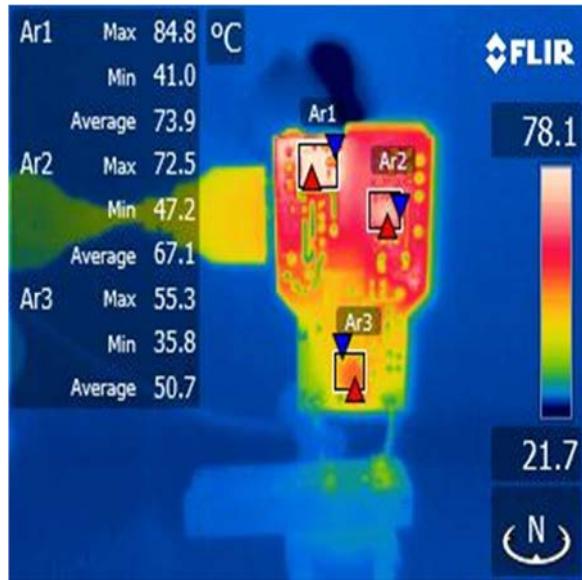
**Figure 13 – Transformer Side. 90 VAC, 2 A Load.**  
Ambient 24.8 °C, Transformer 69.7 °C,  
BJT 69.5 °C, Thermistor 60 °C.



**Figure 14 – LinkSwitch-4 Side. 90 VAC, 2 A Load.**  
Ambient 24.8 °C, Schottky 84.4 °C,  
LinkSwitch-4 75.1 °C, Bridge Rectifier  
60.5 °C.

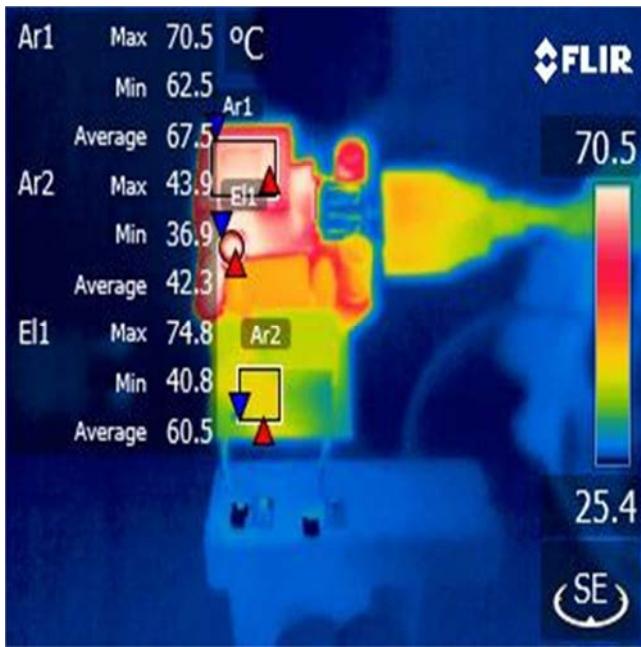


**Figure 15 – Transformer Side. 115 VAC, 2 A Load.**  
Ambient 25.9 °C, BJT 68 °C, Transformer  
68.9 °C, Thermistor 55.2 °C.

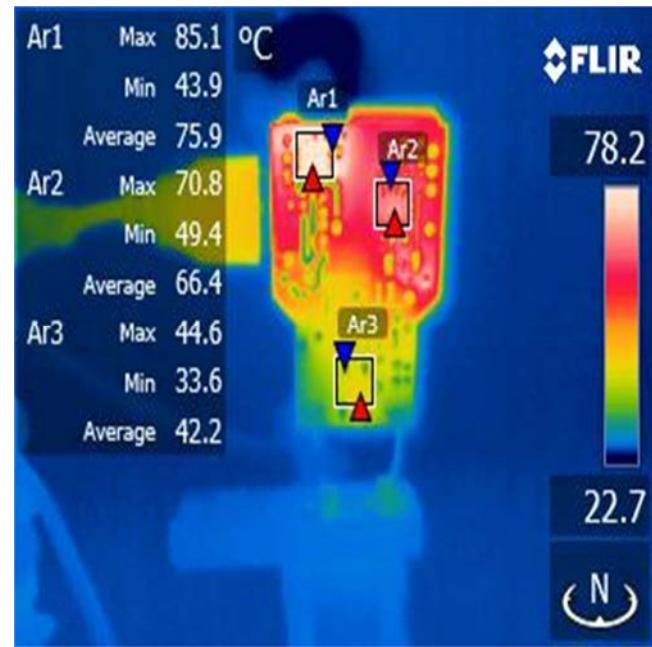


**Figure 16 – LinkSwitch-4 Side. 115 VAC, 2 A Load.**  
Ambient 25.9 °C, Diode 84.8 °C,  
LinkSwitch-4 72.5 °C, Bridge 55.3 °C.

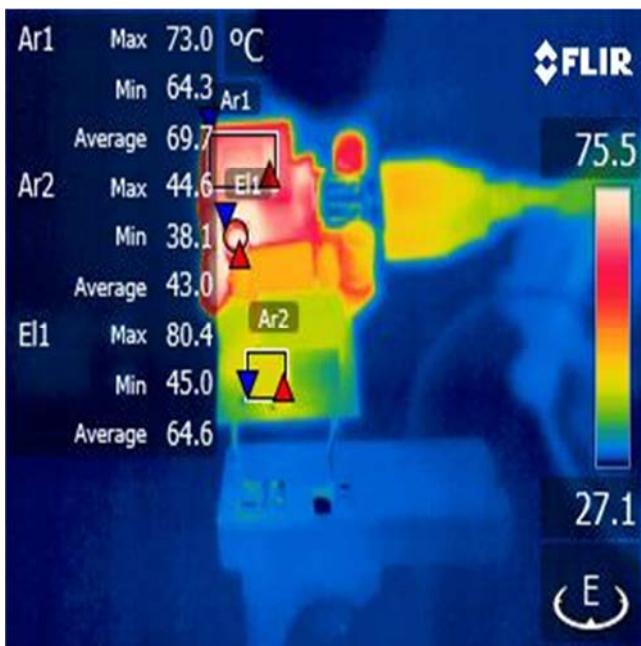




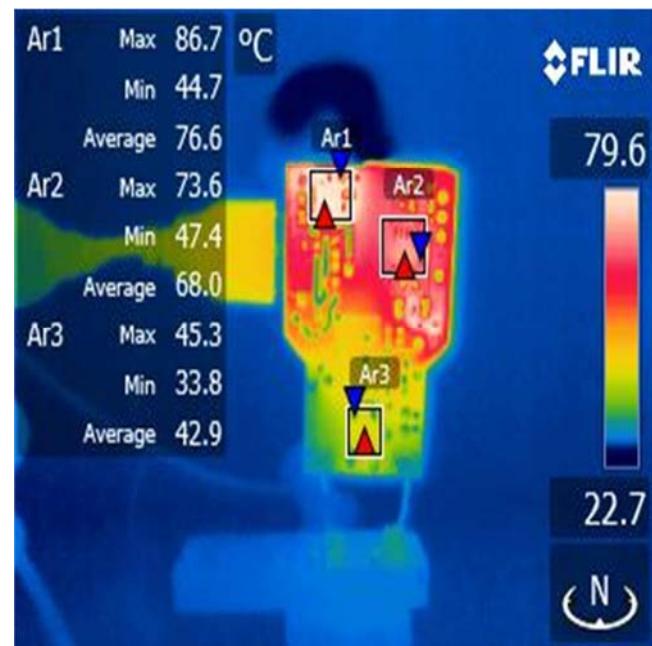
**Figure 17** – Transformer Side. 230 VAC, 2 A Load.  
Ambient 25.7 °C, Transformer 70.5 °C,  
BJT 74.8 °C, Thermistor 43.9 °C.



**Figure 18** – LinkSwitch-4 Side. 230 VAC, 2 A Load.  
Ambient 25.7 °C, Schottky 85.1 °C,  
LinkSwitch-4 70.8 °C, Bridge 44.6 °C.



**Figure 19** – Transformer Side. 265 VAC, 2 A Load.  
Ambient 25.7 °C, Transformer 73 °C,  
BJT 80.4 °C, Thermistor 44.6 °C.



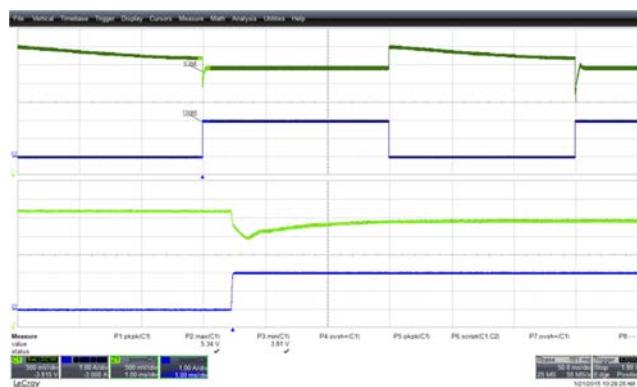
**Figure 20** – LinkSwitch-4 Side. 265 VAC, 2 A Load.  
Ambient 25.7 °C, Schottky 86.7 °C,  
Link4 73.6 °C, Bridge 45.3 °C.

## 11 Waveforms

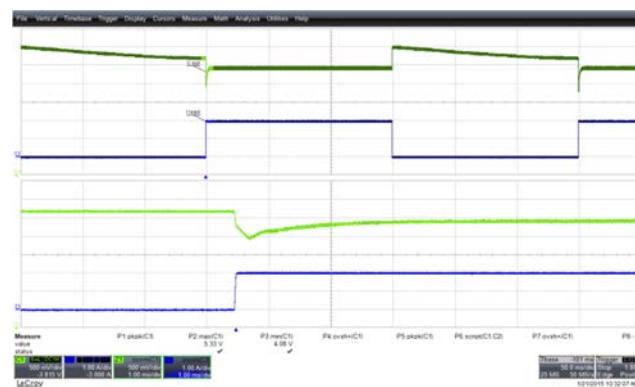
### 11.1 Load Transient Response (End of Cable)

Results were measured with 47  $\mu\text{F}$  at end of simulated cable (150 m $\Omega$  resistor) which is the typical specified measurement condition for mobile phone chargers.

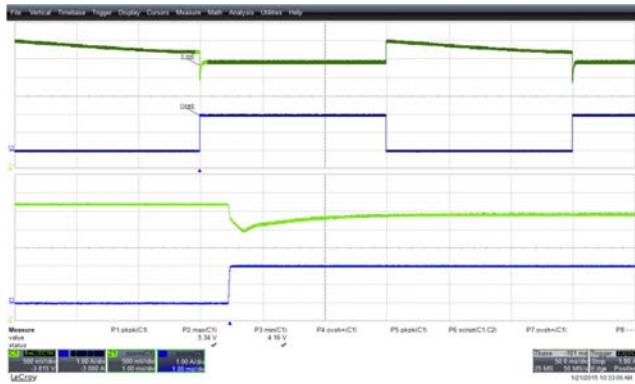
*Note: Transient performance can be optimized by changing output capacitors and also by changing the no-load operating frequency. Although increased no-load operating frequency helps to improve transient response (reduced undershoot), it typically results in a slight increase in no-load input power.*



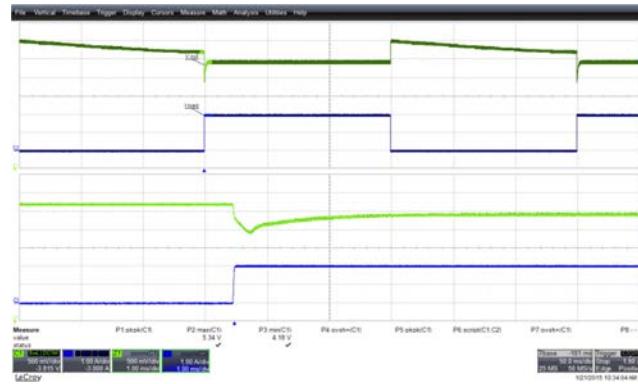
**Figure 21 – Transient Response**  
Min = 3.81 V, Max = 5.34 V.  
90 VAC, 0-2 A Load Step.  
Upper:  $I_{LOAD}$ , 1 A / div.  
Lower:  $V_{OUT}$ , 500 mV, 50 ms / div.



**Figure 22 – Transient Response**  
Min = 4.08 V, Max = 5.33 V.  
115 VAC, 0-2 A Load Step.  
Upper:  $I_{LOAD}$ , 1 A / div.  
Lower:  $V_{OUT}$ , 500 mV, 50 ms / div.



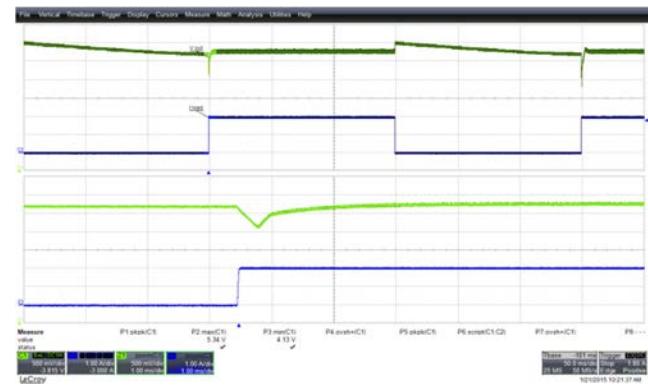
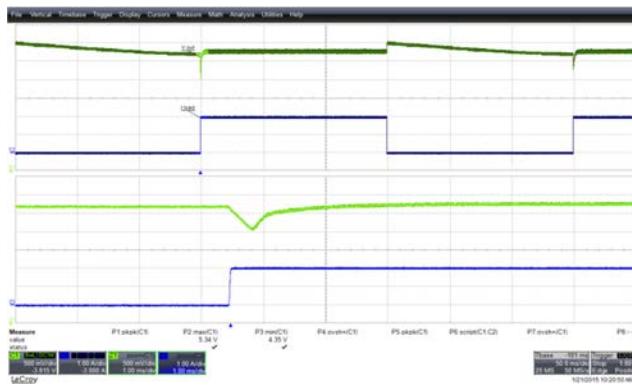
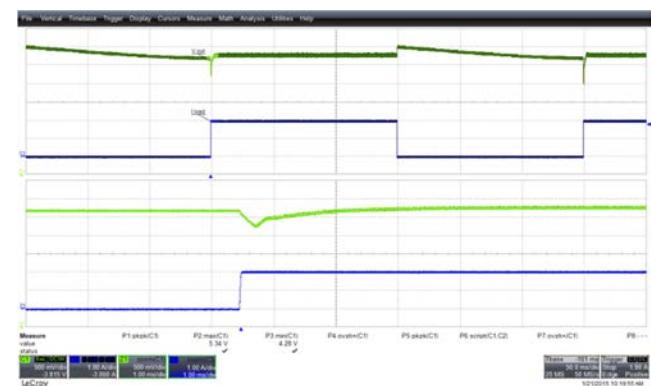
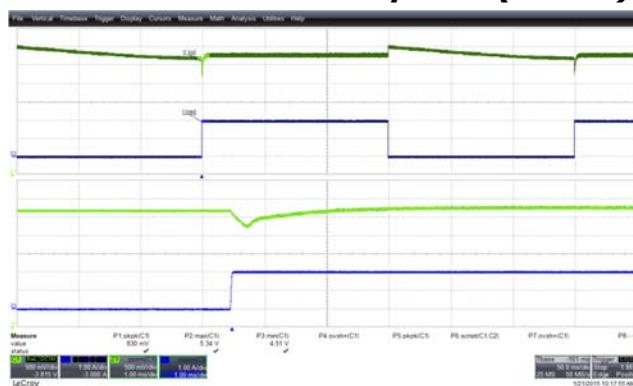
**Figure 23 – Transient Response**  
Min = 4.16 V, Max = 5.34 V.  
230 VAC, 0-2 A Load Step.  
Upper:  $I_{LOAD}$ , 1 A / div.  
Lower:  $V_{OUT}$ , 500 mV, 50 ms / div.



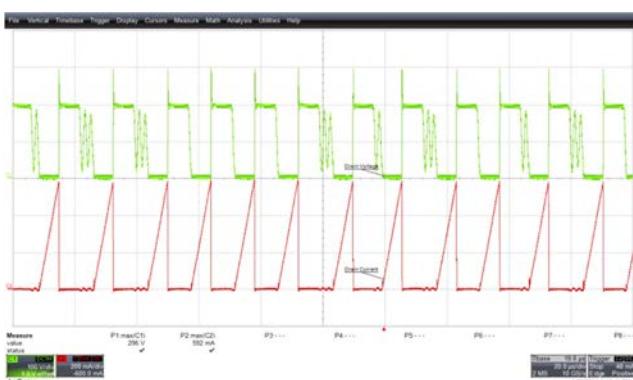
**Figure 24 – Transient Response**  
Min = 4.18 V, Max = 5.34 V.  
265 VAC, 0-2 A Load Step.  
Upper:  $I_{LOAD}$ , 1 A / div.  
Lower:  $V_{OUT}$ , 500 mV, 50 ms / div.



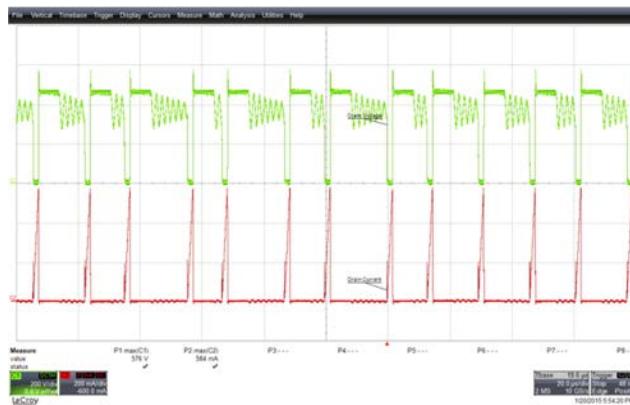
## 11.2 Load Transient Response (at PCB)



### 11.3 Switching Waveforms



**Figure 29 – Drain Voltage and Current Waveforms.**  
90 VAC, 2 A Load, 296 V<sub>MAX</sub>.  
Upper: V<sub>DRAIN</sub>, 100 V, 20  $\mu$ s / div.  
Lower: I<sub>DRAIN</sub>, 200 mA / div.

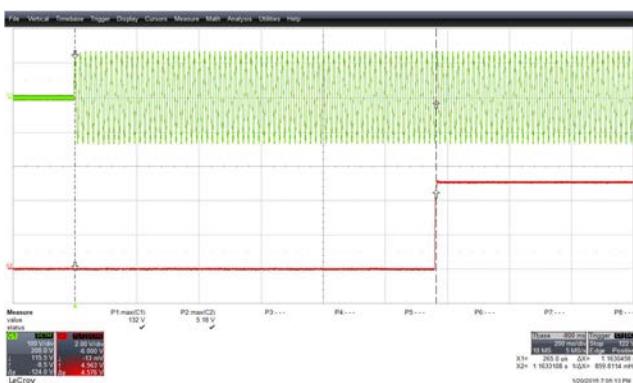


**Figure 30 – Drain Voltage and Current Waveforms.**  
265 VAC, 2 A Load, 584 V<sub>MAX</sub>.  
Upper: V<sub>DRAIN</sub>, 200 V, 20  $\mu$ s / div.  
Lower: I<sub>DRAIN</sub>, 200 mA / div.

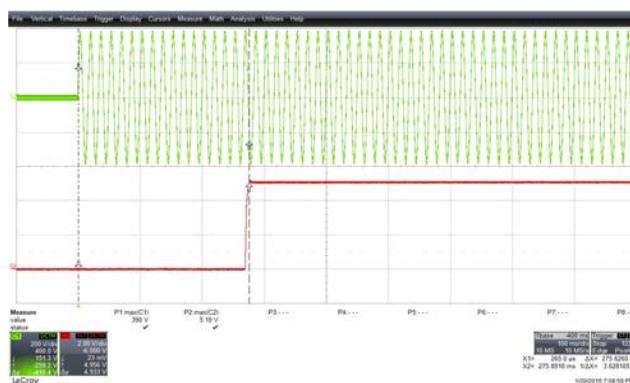
### 11.4 Start-up Waveform and Delay

Note: Delay is maximized by discharging the bulk capacitors completely before testing.  
Unit is at room temperature.

#### 11.4.1 Full Load



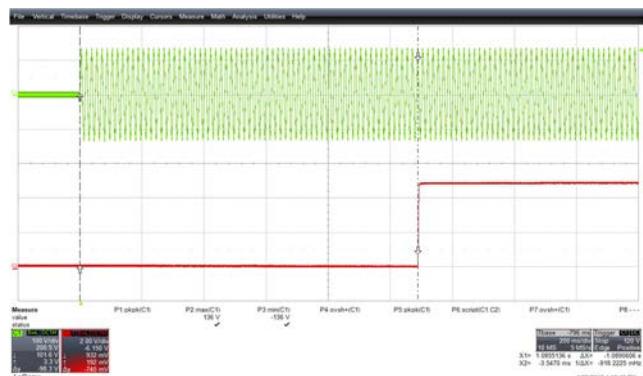
**Figure 31 – Input AC and Output Waveforms.**  
Start-up Time = 1.16 s  
90 VAC, 2.5  $\Omega$  load  
Upper: V<sub>AC</sub>, 100 V, 200 ms / div.  
Lower: V<sub>OUT</sub>, 2 V / div.



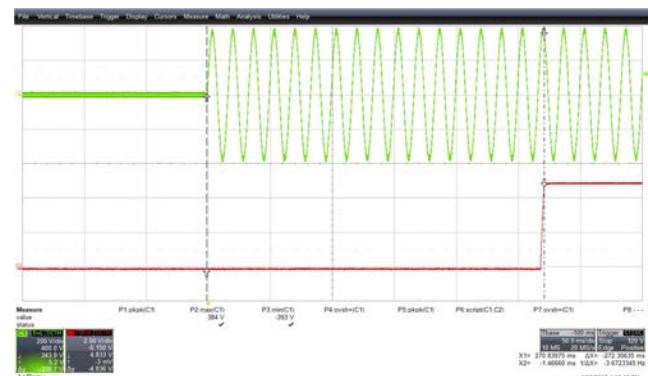
**Figure 32 – Input AC and Output Waveforms.**  
Start-up Time = 275.6 ms  
265 VAC, 2.5  $\Omega$  Load.  
Upper: V<sub>AC</sub>, 200 V, 100 ms / div.  
Lower: V<sub>OUT</sub>, 2 V / div.



### 11.4.2 Zero Load



**Figure 33 – Input AC and Output Waveforms.**  
Start-up Time = 1.1 s.  
90 VAC, Zero Load.  
Upper:  $V_{AC}$ , 100 V, 200 ms / div.  
Lower:  $V_{OUT}$ , 2 V / div.



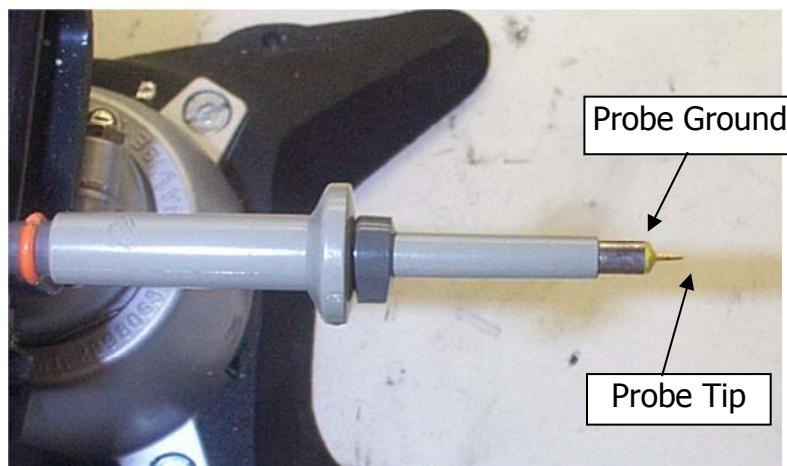
**Figure 34 – Input AC and Output Waveforms.**  
Start-up Time = 272.3 ms.  
265 VAC, Zero Load.  
Upper:  $V_{AC}$ , 200 V, 50 ms / div.  
Lower:  $V_{OUT}$ , 2 V / div.

## 11.5 Output Ripple Measurements

### 11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1  $\mu\text{F}$ /50 V ceramic type and one (1) 47  $\mu\text{F}$ /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).



**Figure 35** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

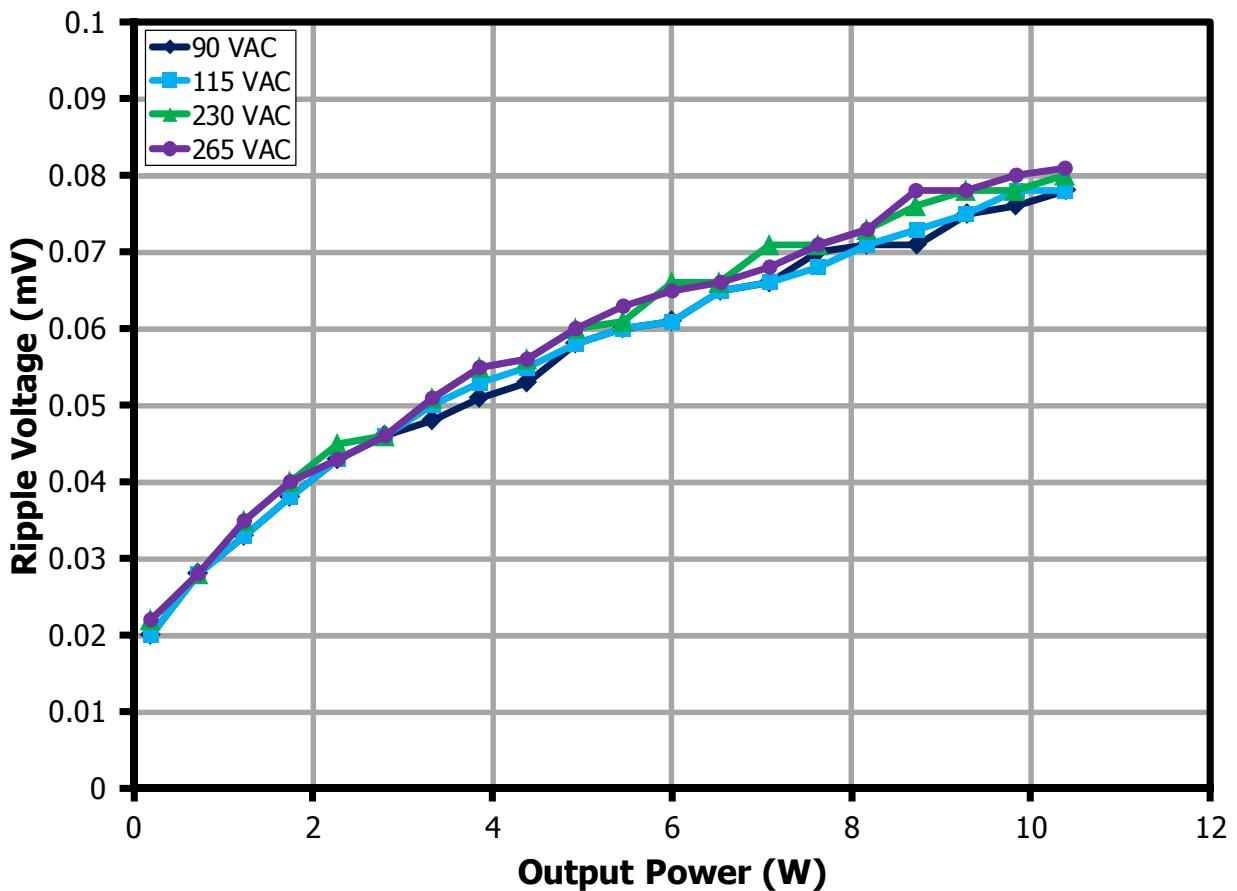


**Figure 36** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

---

### 11.5.2 Measurement Results

Measured at the end of USB cable.



**Figure 37** – Output Ripple Voltage vs. Load Current

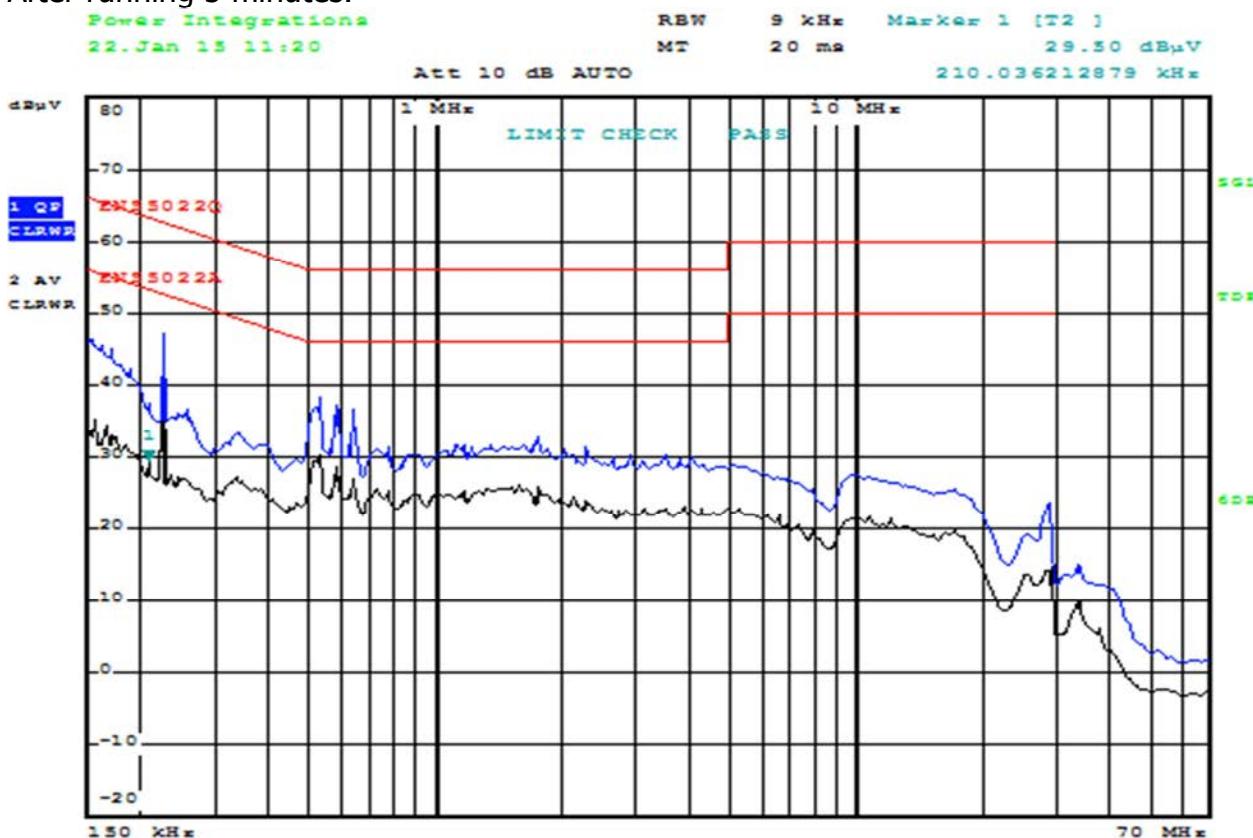
### 11.5.3 Full Load Ripple Voltage (mV p-p)

90 V	115 V	230 V	265 V
78	78	80	81

## 12 Conductive EMI

### 12.1 2 A Resistive Load, Floating Output (QP / AV)

After running 5 minutes.



**Figure 38** – Floating Ground EMI at 115 VAC.



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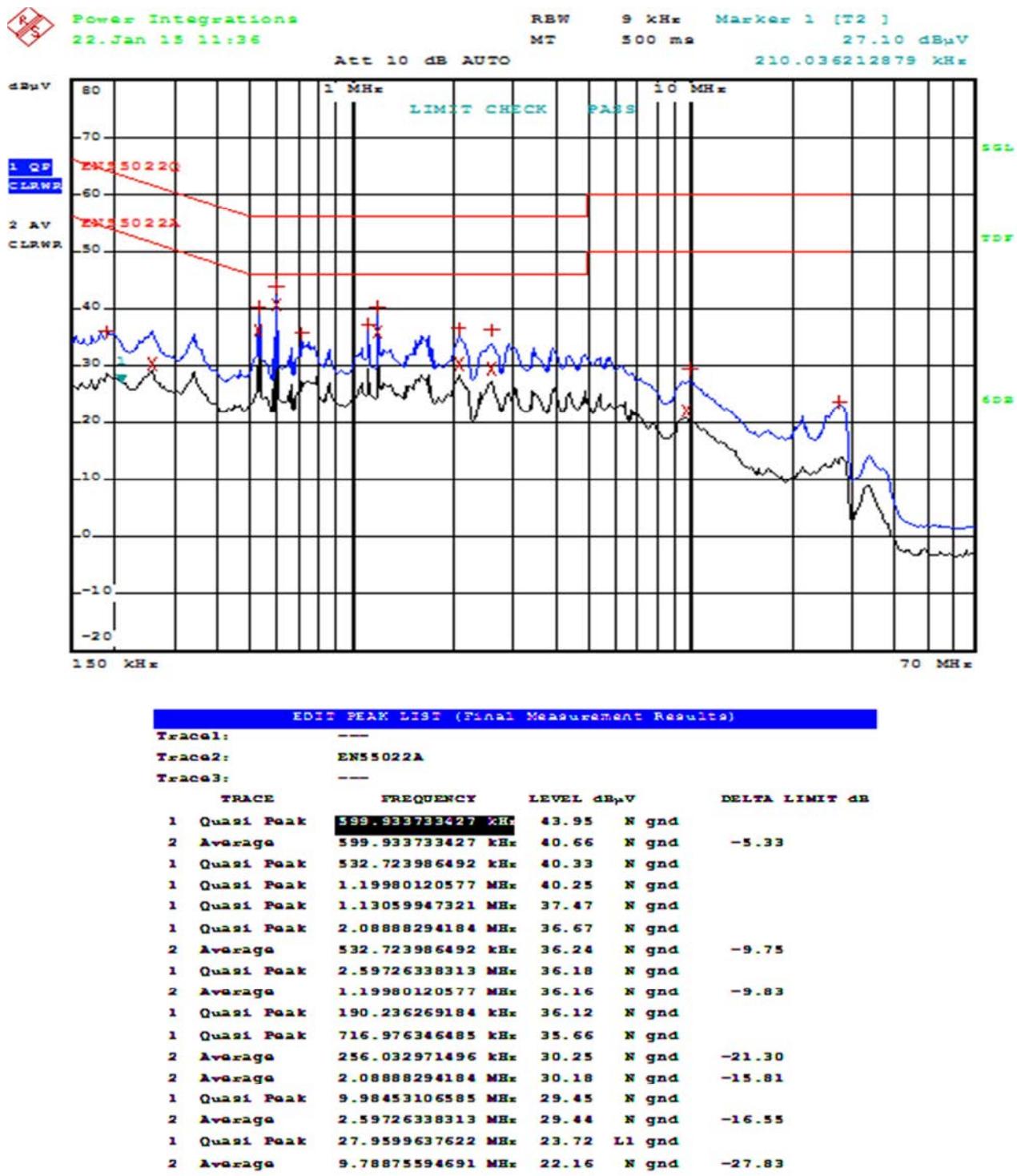


Figure 39 – Floating Ground at 230 VAC.

## 12.2 2 A Resistive Load, Artificial Hand Ground (QP / AV)

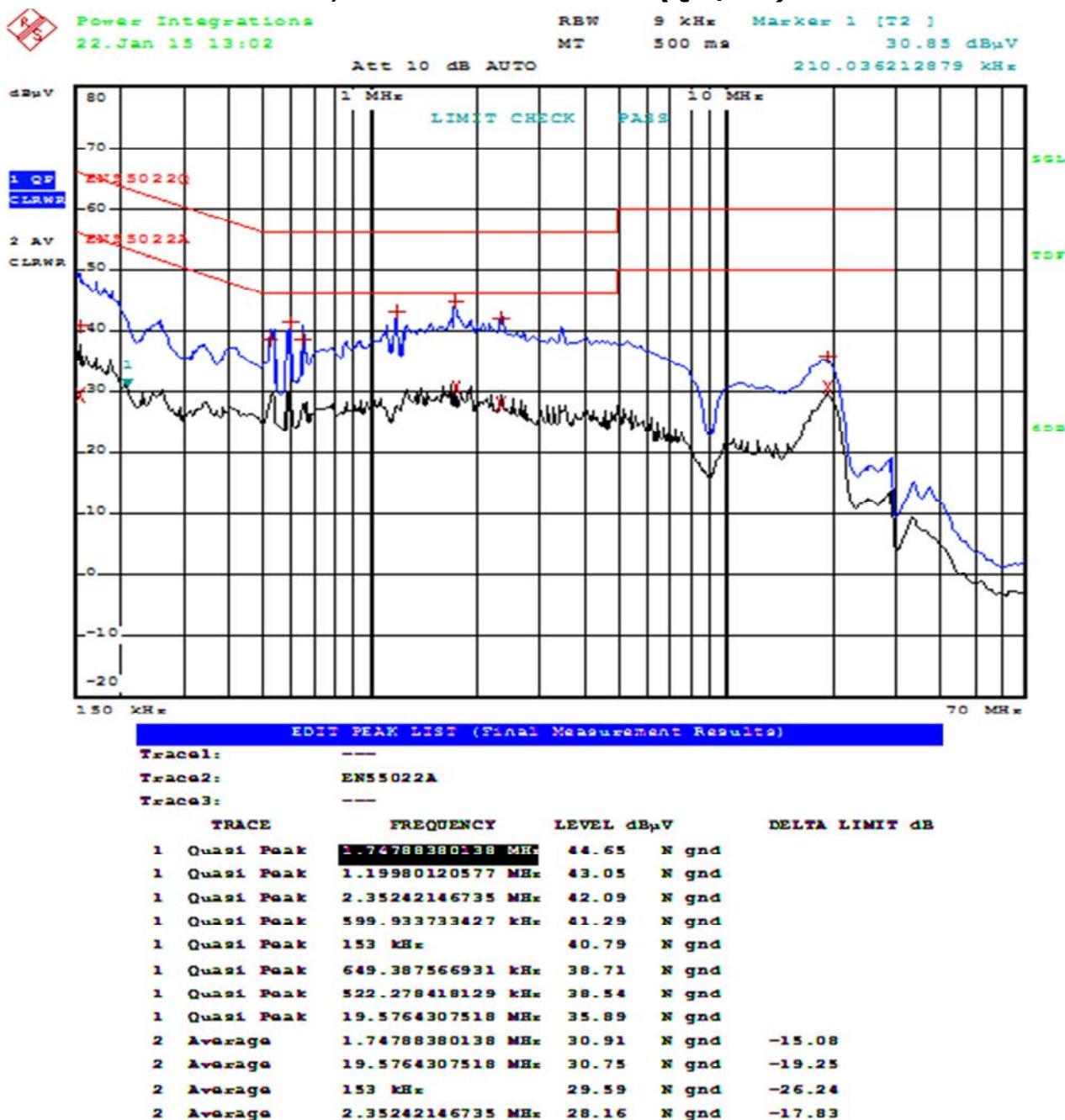


Figure 40 – Artificial Ground at 115 VAC.



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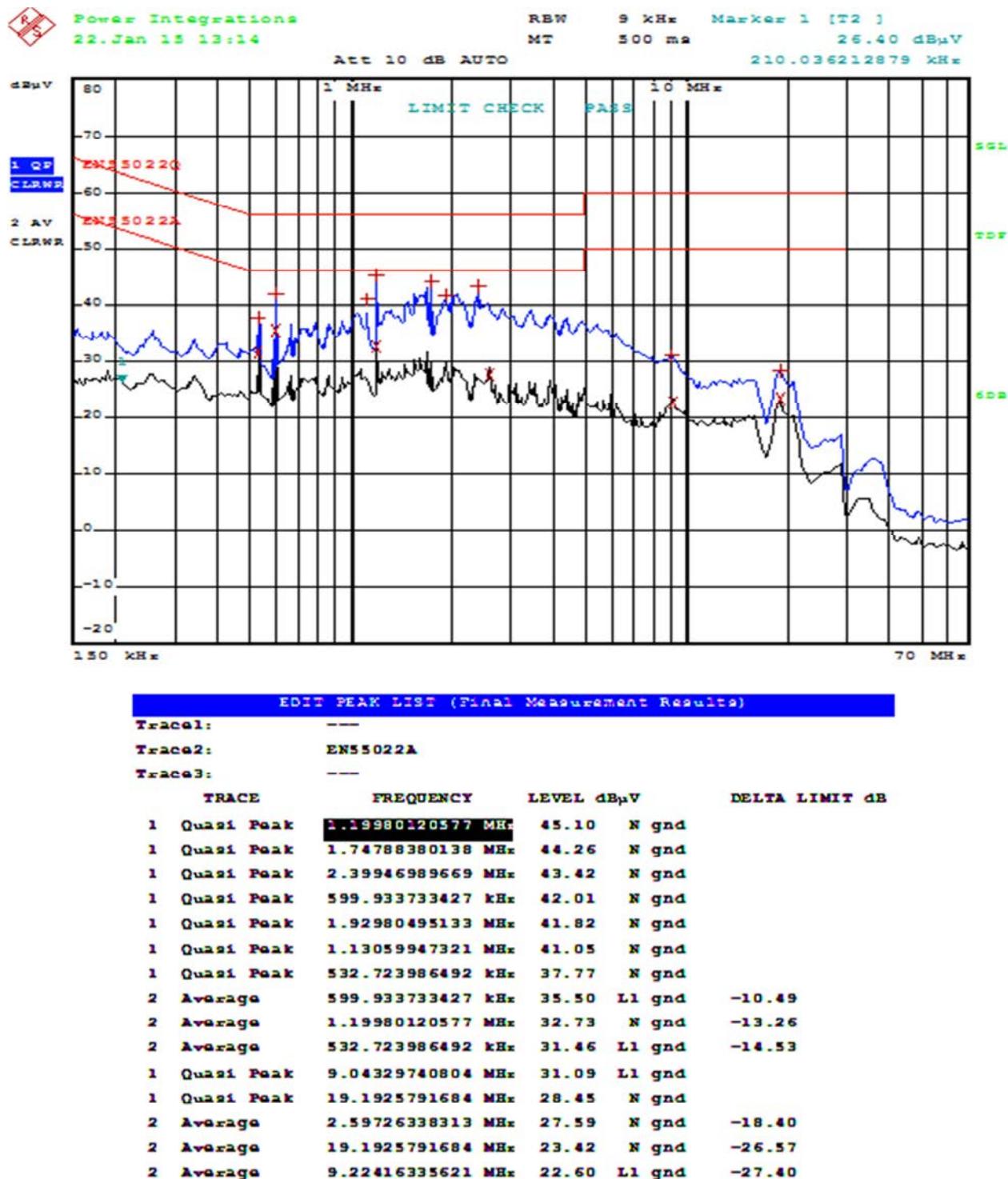


Figure 41 – Artificial Ground at 230 VAC.

## 12.3 Smartphone with Monitor Set-up (HDMI) (QP / AV)

Phone is connected to charger and LCD monitor. The monitor connection increases capacitance to earth ground.

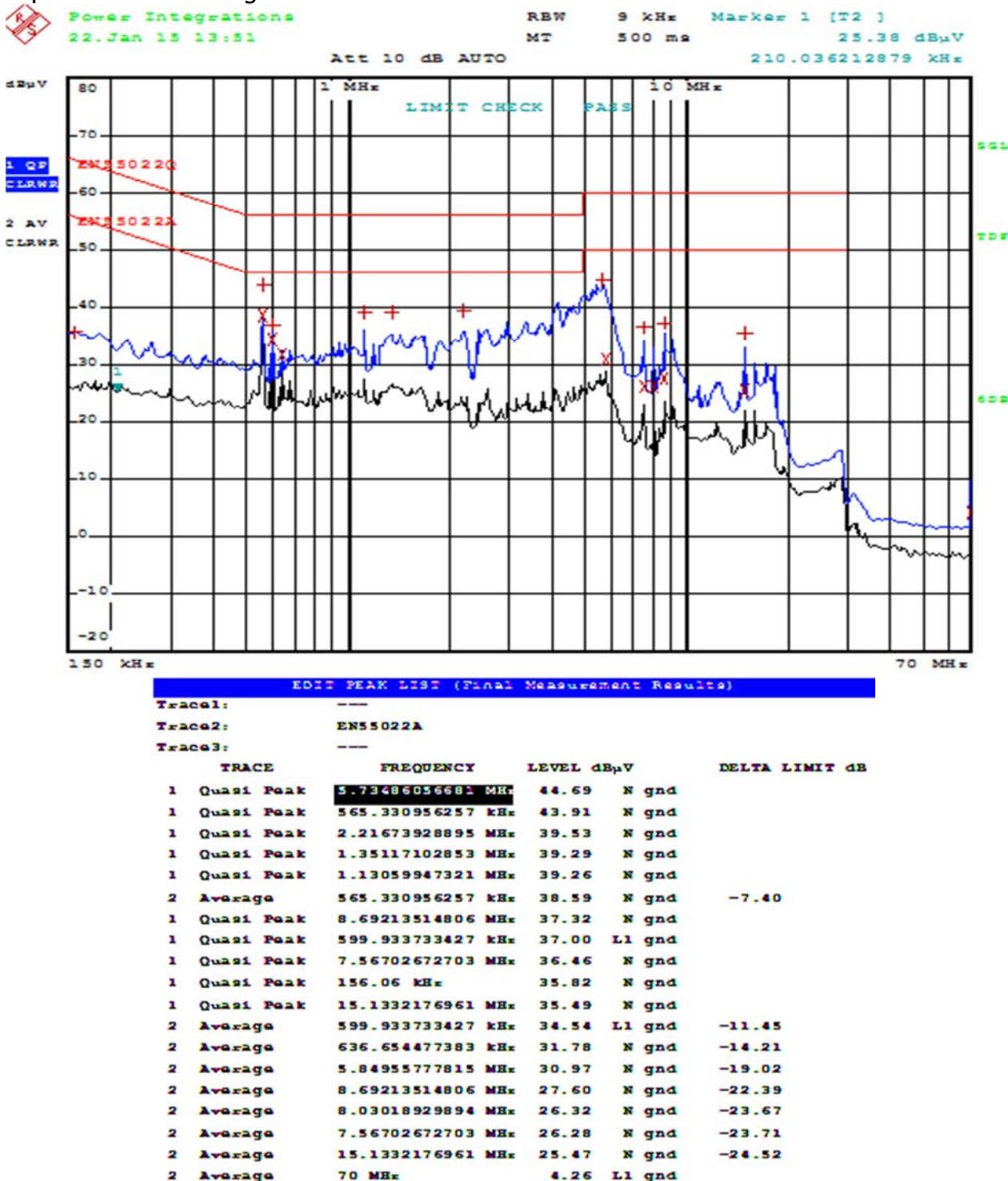


Figure 42 – HDMI at 115 VAC.



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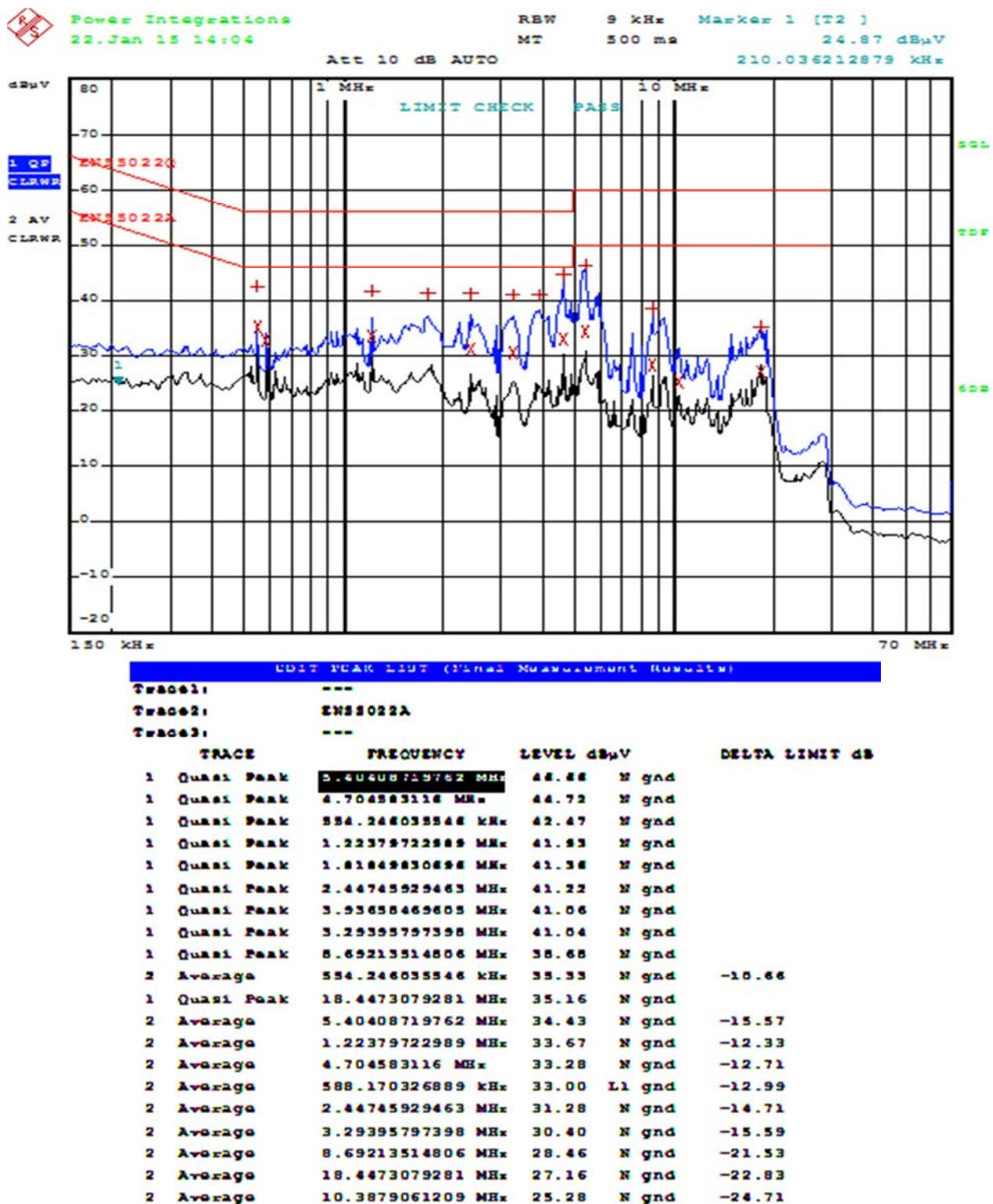
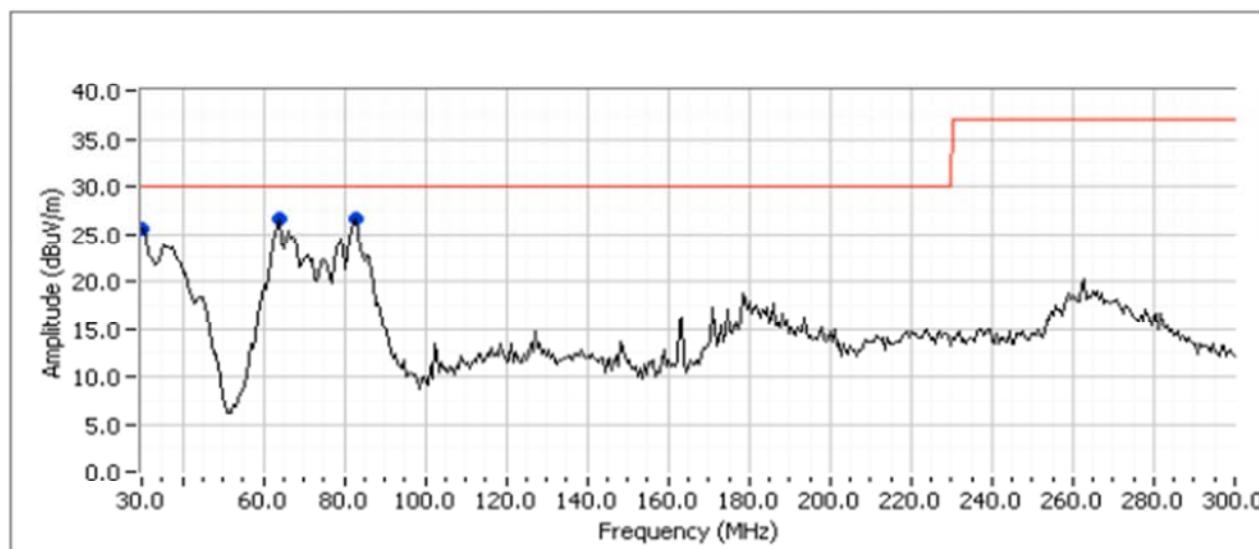


Figure 43 – HDMI at 230 VAC.

## 13 Radiated EMI

### 115 VAC



**Figure 44 – PEAK radiation scan at 115 VAC.**

Preliminary quasi-peak readings (no manipulation of EUT interface cables)

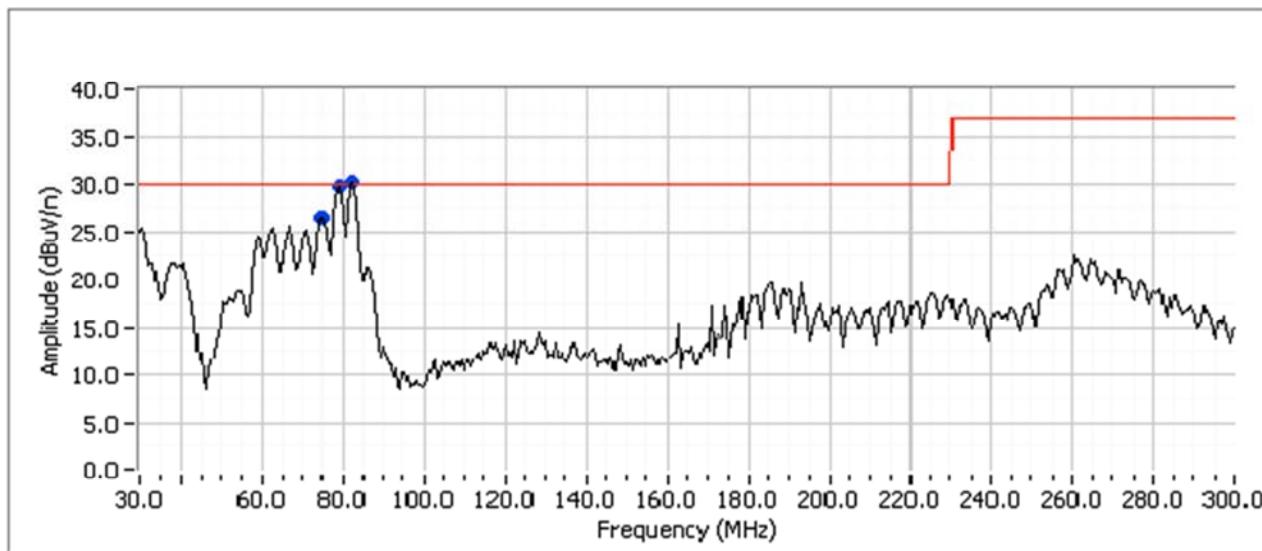
Frequency MHz	Level dBμV/m	Pol v/h	CISPR22 Class B Limit	Margin	Detector	Azimuth degrees	Height meters	Comments
82.586	25.0	V	30.0	-5.0	QP	224	1.1	QP (1.00s)
30.021	23.5	V	30.0	-6.5	QP	316	1.0	QP (1.00s)
64.258	22.6	V	30.0	-7.4	QP	342	2.1	QP (1.00s)

**Figure 45 – Quasi-Peak radiation at 115 VAC.**



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**230 VAC****Figure 46** – PEAK radiation scan at 230 VAC.**Preliminary quasi-peak readings (no manipulation of EUT interface cables)**

Frequency MHz	Level dB $\mu$ V/m	Pol v/h	CISPR22 Class B		Detector	Azimuth degrees	Height meters	Comments
			Limit	Margin	Pk/QP/Avg			
79.529	27.6	V	30.0	-2.4	QP	70	1.7	QP (1.00s)
82.354	27.4	V	30.0	-2.6	QP	221	1.0	QP (1.00s)
75.238	24.2	V	30.0	-5.8	QP	97	2.0	QP (1.00s)

**Figure 47** – Quasi-Peak radiation at 230 VAC.

## 14 Lighting Surge and ESD Test

### 14.1 Differential Mode Test

Passed  $\pm 1$  kV, 500 A surge test, no output test LED blink.

**Result: PASS**

### 14.2 Common Mode Ring Wave Test

240 strikes - 10 strikes each of all 24 combinations of 6 kV, 12  $\Omega$ :

Polarity: + and -

Line phase angle: 0°, 90°, 180°, 270°

Applied voltage: L/PE, N/PE, L,N/PE

**Result : PASS**

### 14.3 ESD Test

Passed  $\pm 16.5$  kV air,  $\pm 8$  kV contact, 10x each (40 total).

An LED across the 2.5  $\Omega$  load shows no blinking.

**Result: PASS**



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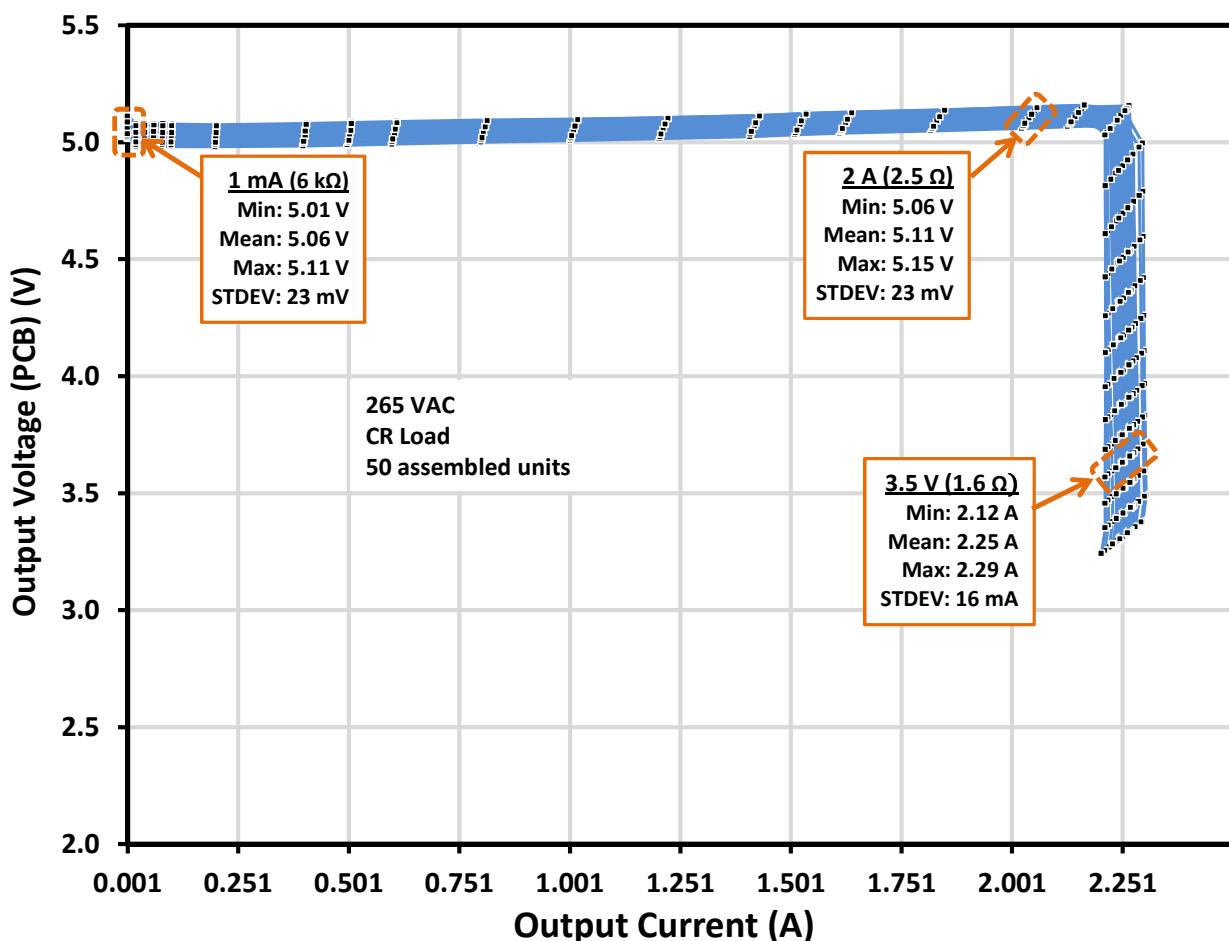
## 15 Appendix – Production Data

50 production units of the RD-462 were characterized and the results summarized below. This data includes variation of all components, including the LinkSwitch-4 IC and demonstrates the production tolerance and variability that can be achieved in high volume production.

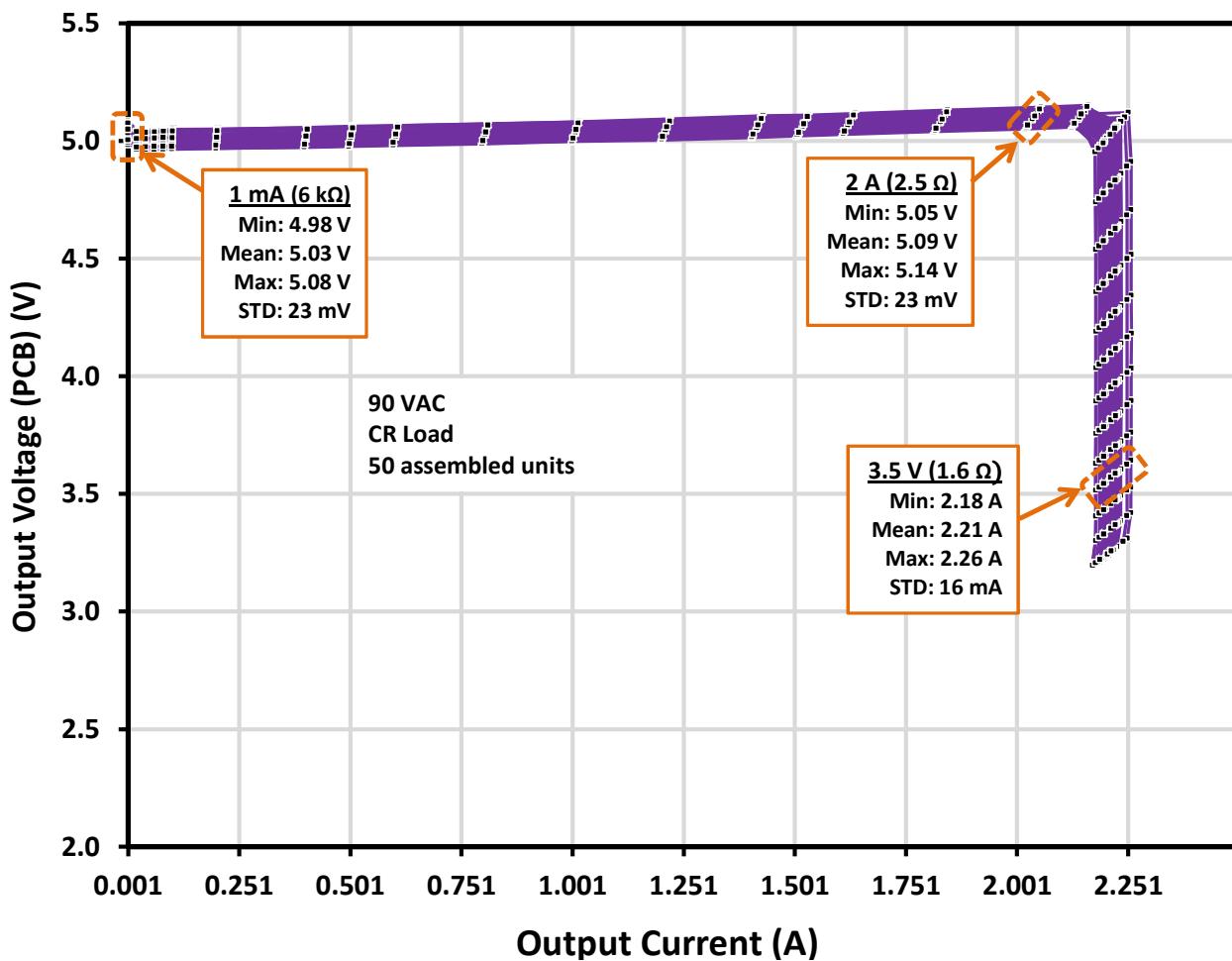
### 15.1 Output CV/CC Characteristic

Measured on NHR production test system, CR load 90 VAC and 265 VAC.

Note: Minimum voltage in CC operation does not represent the auto-restart point.



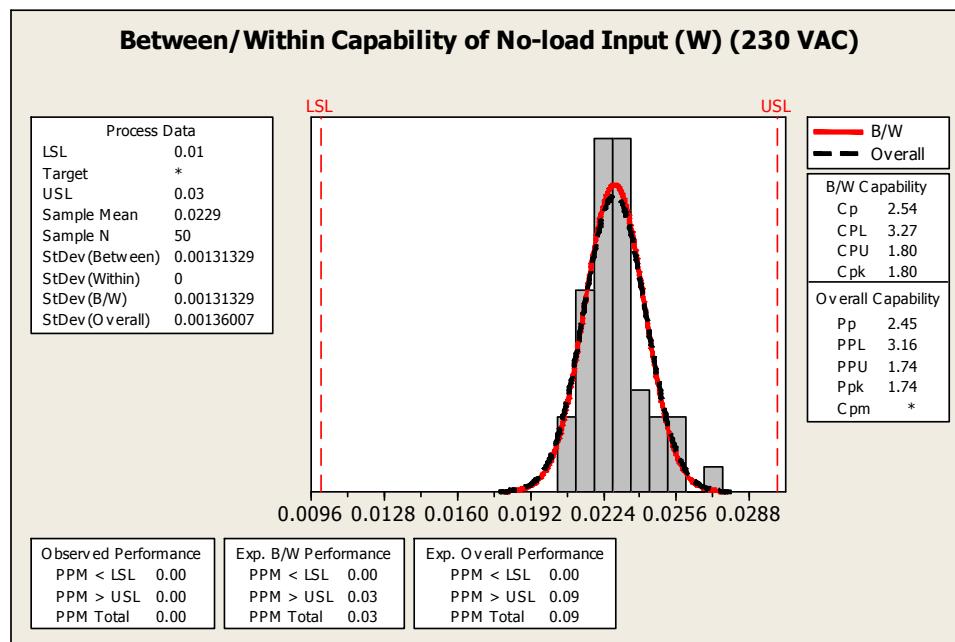
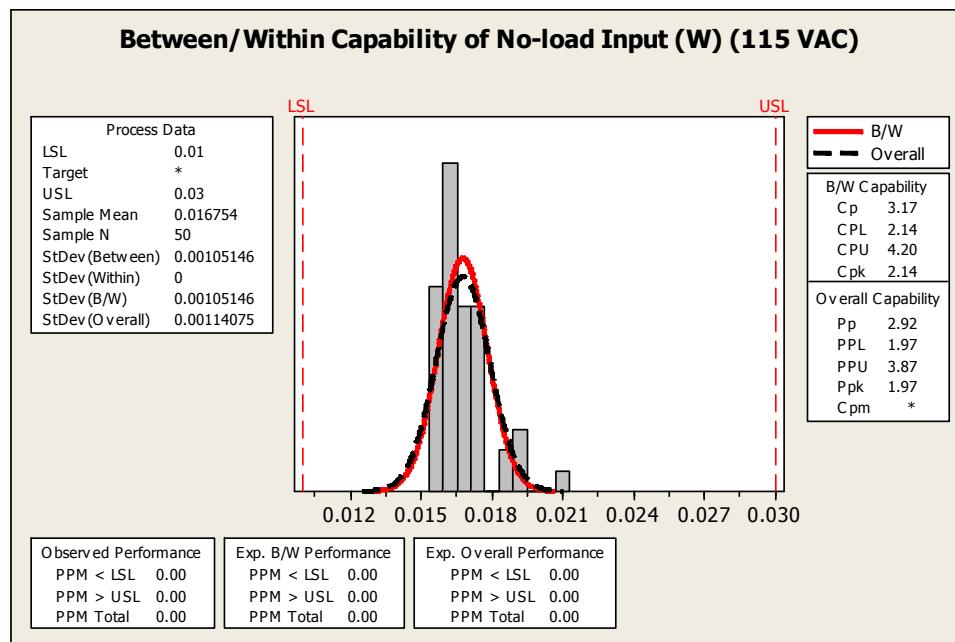
**Figure 48** – CV/CC Characteristic, 50 production units, 265 VAC.



**Figure 49 – CV/CC Characteristic, 50 Production Units, 90 VAC.**

## 15.2 No-Load Input Power

Data indicates sufficient repeatability to guarantee <30 mW at 115 VAC and 230 VAC.



## 16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
28-Jan-15	TD	1.0	Initial Release	Apps & Mktg
31-Jul-15	KM	1.1	Fixed Schematic Error.	
02-Aug-16	Km	1.2	Added Magnetics Supplier	

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