International
IOR Rectifier

IRF8513PbF

HEXFET® Power MOSFET

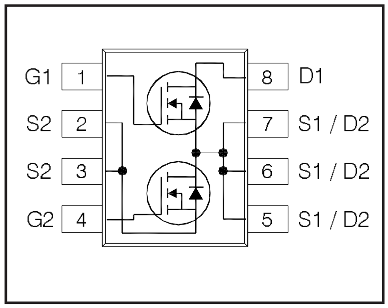
Applications

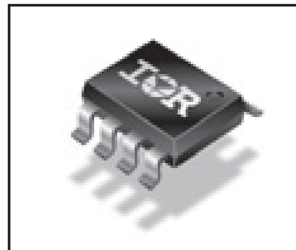
- Dual SO-8 MOSFET for POL Converters in Notebook Computers, Servers, Graphics Cards, Game Consoles and Set-Top Box

V_{DSS}		$R_{DS(on)}$ max	I_D
30V	Q1	15.5mΩ@V_{GS} = 10V	8.0A
	Q2	12.7mΩ@V_{GS} = 10V	11A

Benefits

- Low Gate Charge and Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating
- 100% Tested for R_G
- Lead-Free (Qualified to 260°C Reflow)
- RoHS Compliant (Halogen Free)





SO-8

Description

The IRF8513PbF incorporates the latest HEXFET Power MOSFET Silicon Technology into the industry standard SO-8 package. The IRF8513PbF has been optimized for parameters that are critical in synchronous buck operation including Rds(on) and gate charge to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors for notebook and Netcom applications.

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	30		V
V_{GS}	Gate-to-Source Voltage	± 20		
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	8.0	11	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	6.2	9.0	
I_{DM}	Pulsed Drain Current ①	64	88	
P_D @T_A = 25°C	Power Dissipation	1.5	2.4	W
P_D @T_A = 70°C	Power Dissipation	1.05	1.68	
	Linear Derating Factor	0.01	0.02	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	42	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	100	62.5	

Notes ① through ⑤ are on page 11

ORDERING INFORMATION:
See detailed ordering and shipping information on the last page of this data sheet.

11/05/08

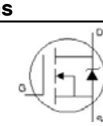
Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	—	0.021	—	V/°C	Reference to 25°C, I_D = 1mA
		Q2	—	0.021	—		
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	—	12.5	15.5	mΩ	V_{GS} = 10V, I_D = 8.0A ③
			—	18.1	22.2		V_{GS} = 4.5V, I_D = 6.4A ③
		Q2	—	10.2	12.7		V_{GS} = 10V, I_D = 11A ③
			—	14.2	16.9		V_{GS} = 4.5V, I_D = 8.6A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1&Q2	1.35	1.8	2.35	V	Q1: V_{DS} = V_{GS}, I_D = 25μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	—	-6.5	—	mV/°C	Q2: V_{DS} = V_{GS}, I_D = 25μA
		Q2	—	-6.9	—		
I_{DSS}	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V_{DS} = 24V, V_{GS} = 0V
		Q1&Q2	—	—	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	Q1	19	—	—	S	V_{DS} = 15V, I_D = 6.4A
		Q2	24	—	—		V_{DS} = 15V, I_D = 8.6A
Q_g	Total Gate Charge	Q1	—	5.7	8.6	nC	
		Q2	—	7.6	11.4		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	—	1.2	—		Q1
		Q2	—	1.7	—		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	—	0.68	—		V_{GS} = 4.5V, I_D = 6.4A
		Q2	—	1.0	—		
Q_{gd}	Gate-to-Drain Charge	Q1	—	2.2	—		Q2
		Q2	—	3.1	—		V_{DS} = 15V
Q_{godr}	Gate Charge Overdrive	Q1	—	1.6	—		V_{GS} = 4.5V, I_D = 8.6A
		Q2	—	1.9	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	—	2.9	—		See Fig. 31a &31b
		Q2	—	4.0	—		
Q_{oss}	Output Charge	Q1	—	3.9	—	nC	V_{DS} = 16V, V_{GS} = 0V
		Q2	—	5.2	—		
R_G	Gate Resistance	Q1	—	2.1	3.2	Ω	
		Q2	—	1.4	3.1		
$t_{d(on)}$	Turn-On Delay Time	Q1	—	8.0	—	ns	Q1
		Q2	—	8.9	—		V_{DD} = 15V, V_{GS} = 4.5V
t_r	Rise Time	Q1	—	8.5	—		I_D = 6.4A
		Q2	—	10.7	—		R_G = 1.8Ω See Fig.30a & 30b
$t_{d(off)}$	Turn-Off Delay Time	Q1	—	8.8	—		Q2
		Q2	—	9.3	—		V_{DD} = 15V, V_{GS} = 4.5V
t_f	Fall Time	Q1	—	5.7	—		I_D = 8.6A
		Q2	—	5.0	—		RG = 1.8W
C_{iss}	Input Capacitance	Q1	—	766	—	pF	
		Q2	—	1024	—		V_{GS} = 0V
C_{oss}	Output Capacitance	Q1	—	172	—		V_{DS} = 15V
		Q2	—	238	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	Q1	—	83	—		
		Q2	—	116	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	49	70	mJ
I_{AR}	Avalanche Current ①	—	6.4	8.6	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	Q1	—	—	1.9	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		Q2	—	—	3.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	Q1	—	—	64	A	
		Q2	—	—	88		
V_{SD}	Diode Forward Voltage	Q1	—	—	1.0	V	T_J = 25°C, I_S = 6.4A, V_{GS} = 0V ③
		Q2	—	—	1.0		T_J = 25°C, I_S = 8.6A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	Q1	—	15	23	ns	Q1 T_J = 25°C, I_F = 6.4A, V_{DD} = 15V, di/dt = 100A/μs ③
		Q2	—	17	26		
Q_{rr}	Reverse Recovery Charge	Q1	—	7.2	11	nC	Q2 T_J = 25°C, I_F = 8.6A, VDD = 15V, di/dt = 100A/μs ③
		Q2	—	9.3	14		
t_{on}	Forward Trun-On Time	Intrinsic turn -on time is negligible (turn -on is dominated by LS+LD)					

Typical Characteristics

Q1 - Control FET

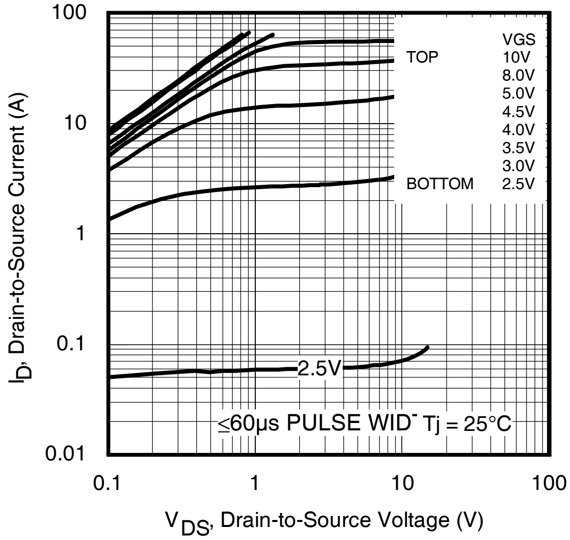


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET

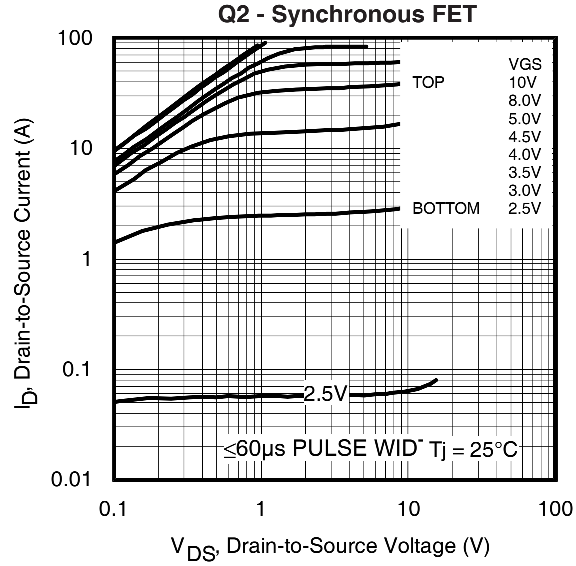


Fig 2. Typical Output Characteristics

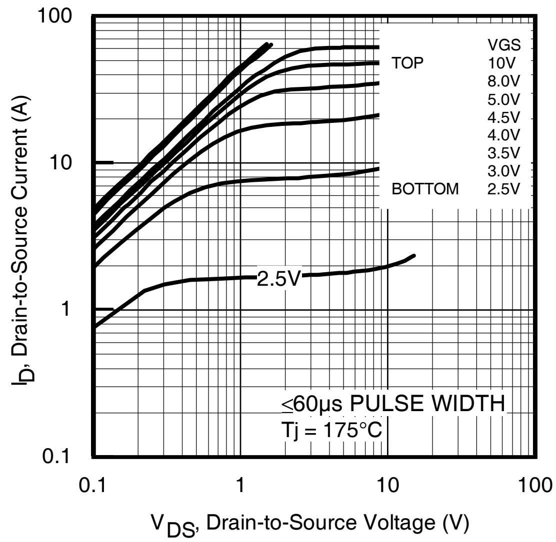


Fig 3. Typical Output Characteristics

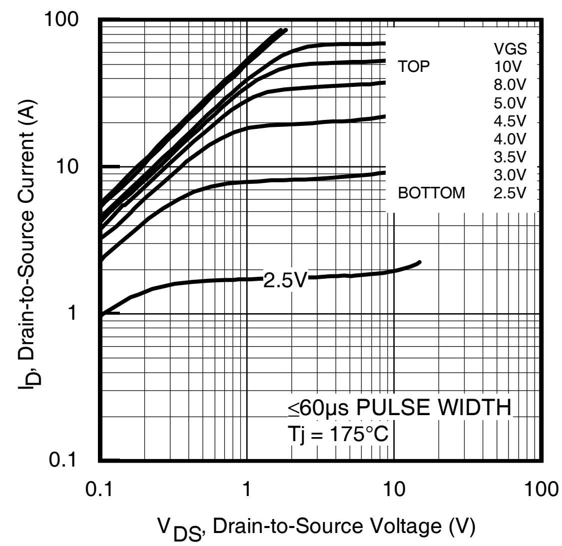


Fig 4. Typical Output Characteristics

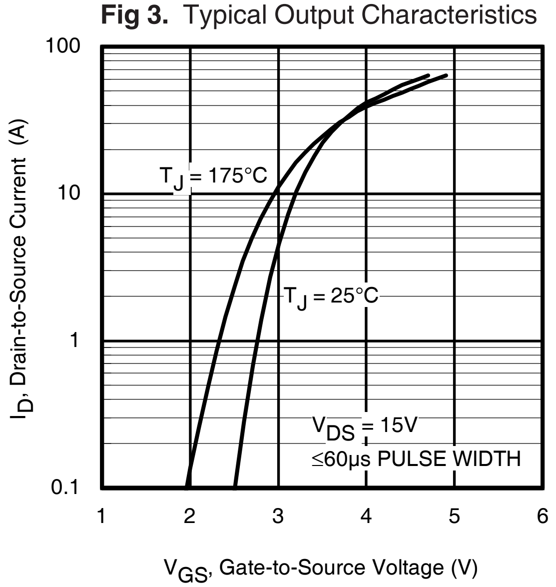


Fig 5. Typical Transfer Characteristics

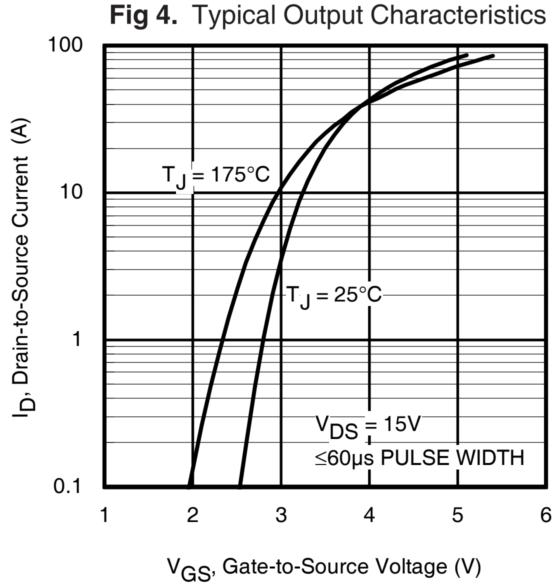


Fig 6. Typical Transfer Characteristics

Typical Characteristics

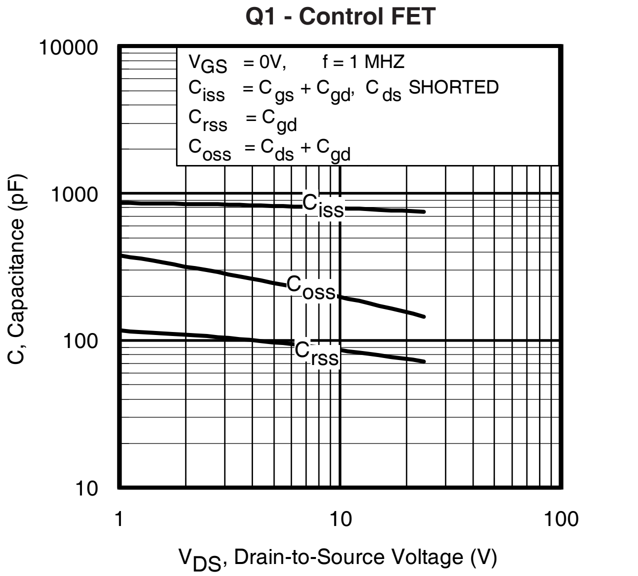


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

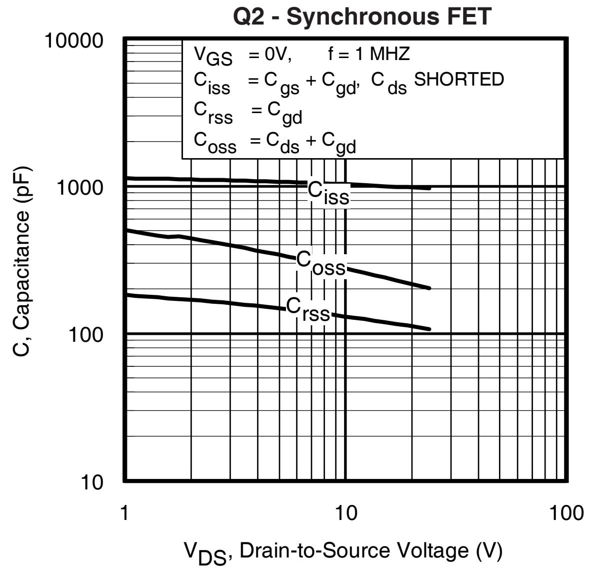


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

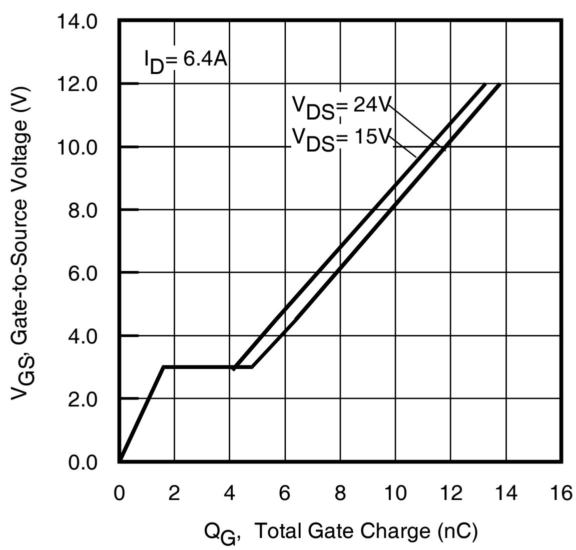


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

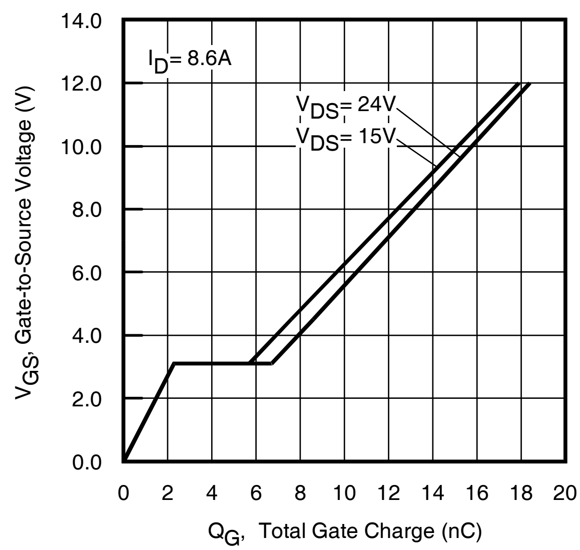


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

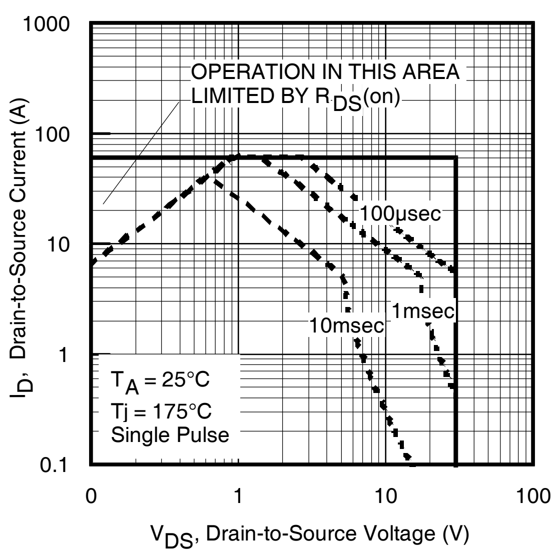


Fig 11. Maximum Safe Operating Area

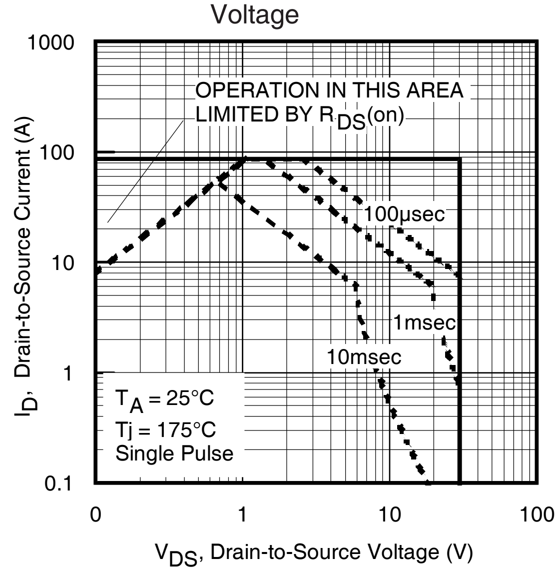


Fig 12. Maximum Safe Operating Area

Typical Characteristics

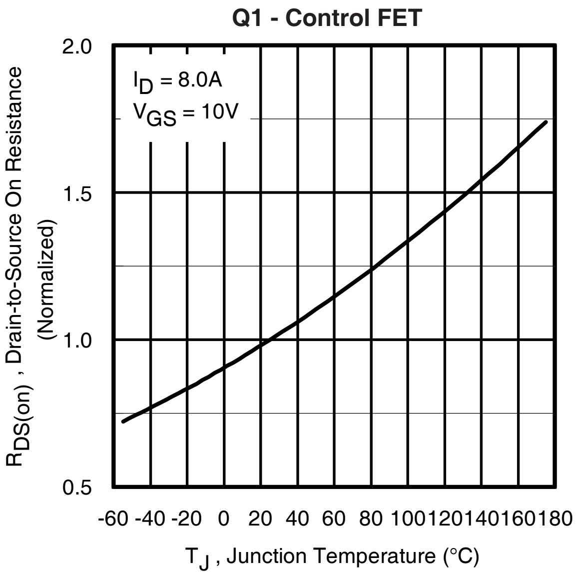


Fig 13. Normalized On-Resistance vs. Temperature

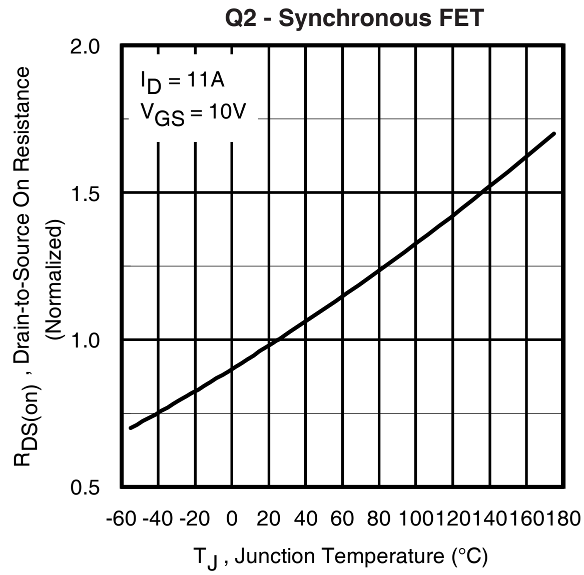


Fig 14. Normalized On-Resistance vs. Temperature

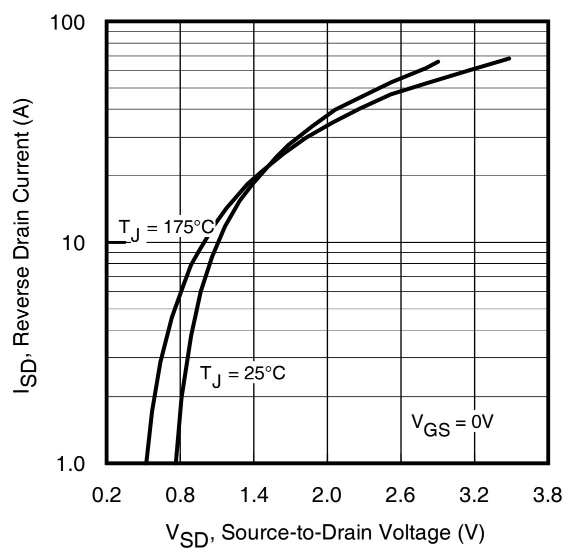


Fig 15. Typical Source-Drain Diode Forward Voltage

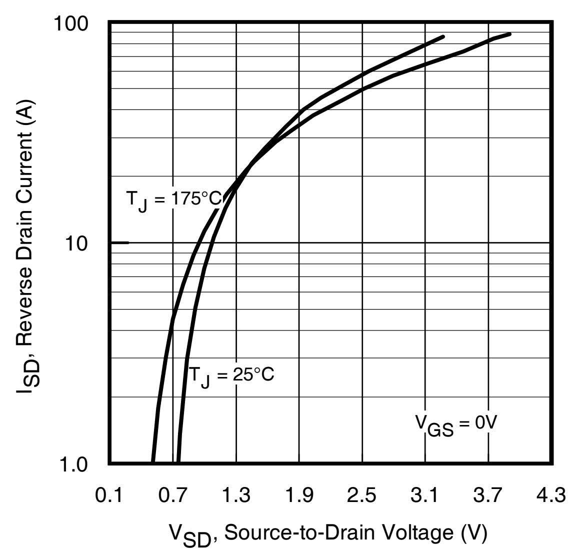


Fig 16. Typical Source-Drain Diode Forward Voltage

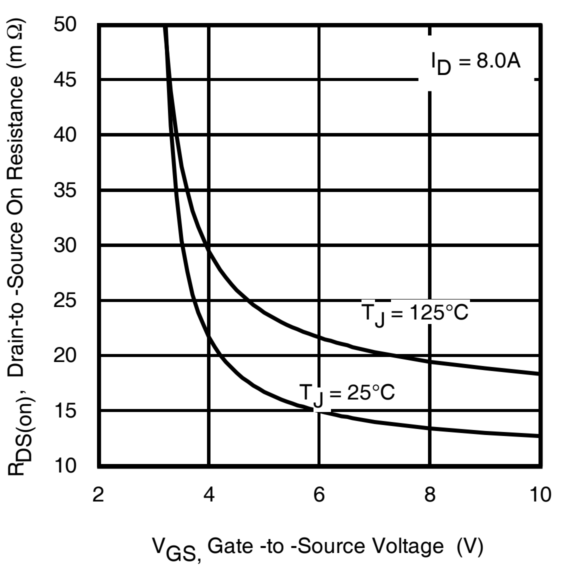


Fig 17. Typical On-Resistance vs.Gate Voltage

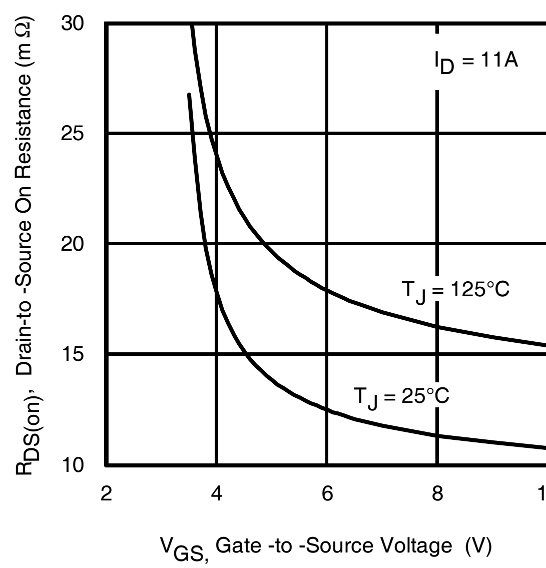


Fig 18. Typical On-Resistance vs.Gate Voltage

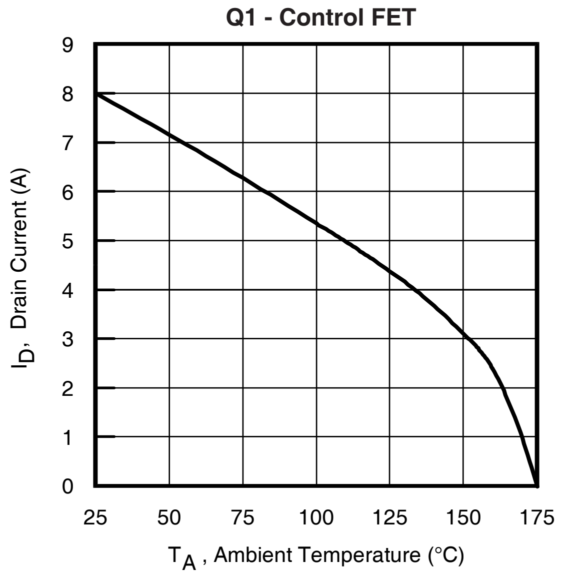


Fig 19. Maximum Drain Current vs. Ambient Temp.

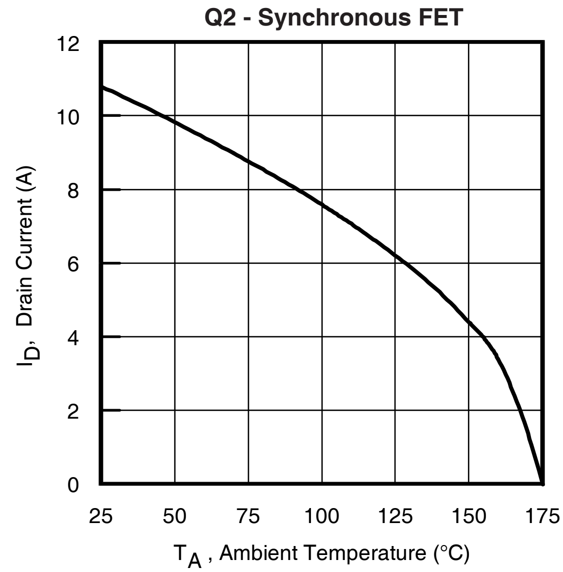


Fig 20. Maximum Drain Current vs. Ambient Temp.

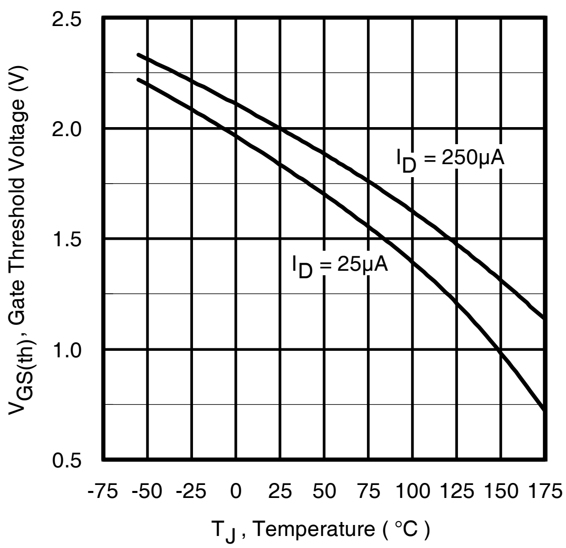


Fig 21. Threshold Voltage vs. Temperature

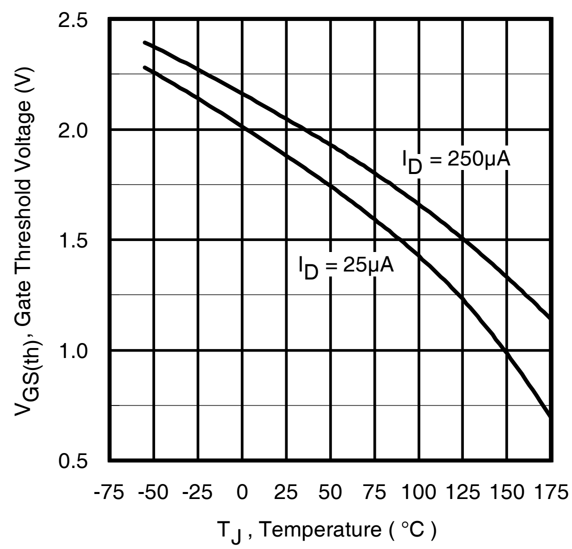


Fig 22. Threshold Voltage vs. Temperature

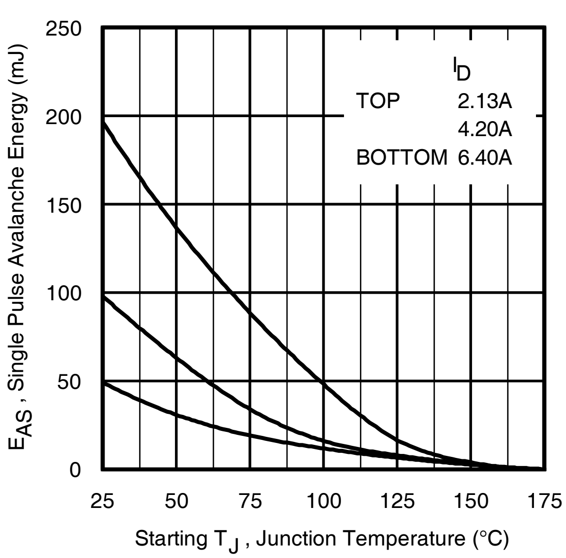


Fig 23. Maximum Avalanche Energy vs. Drain Current

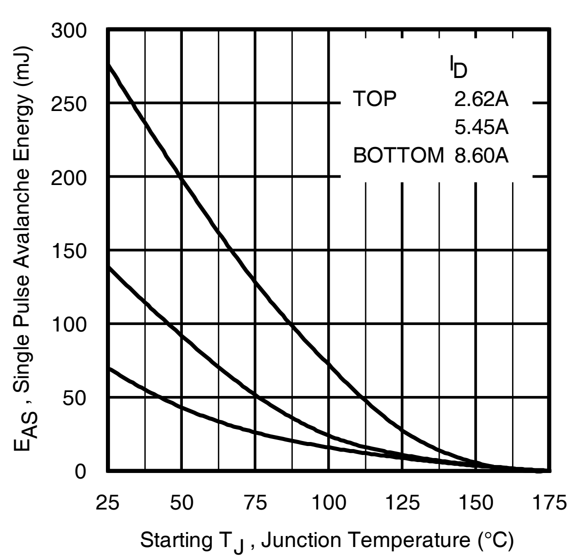


Fig 24. Maximum Avalanche Energy vs. Drain Current

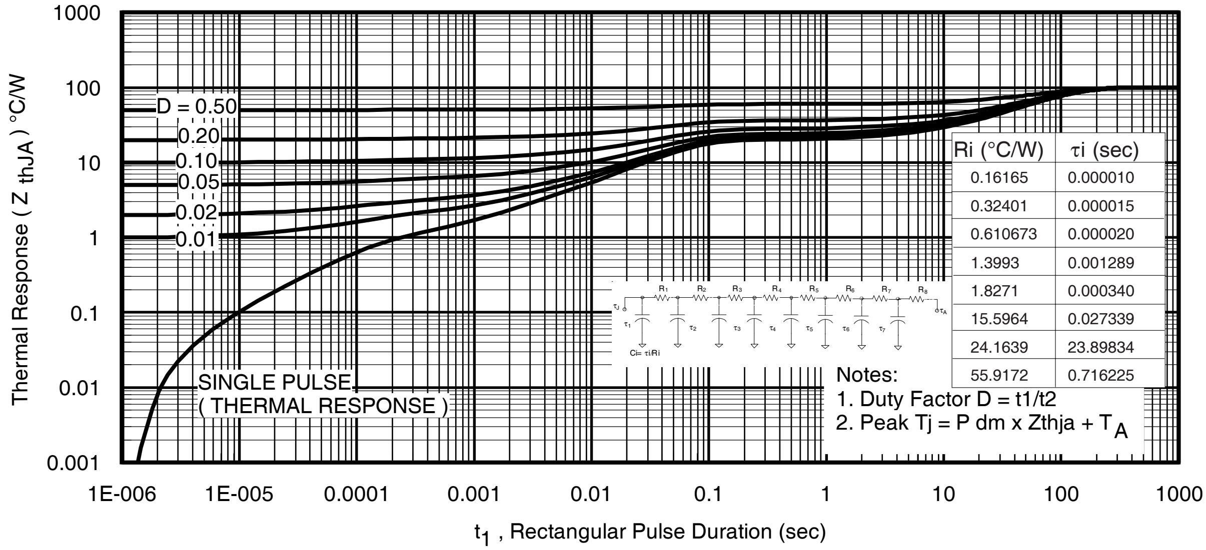


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

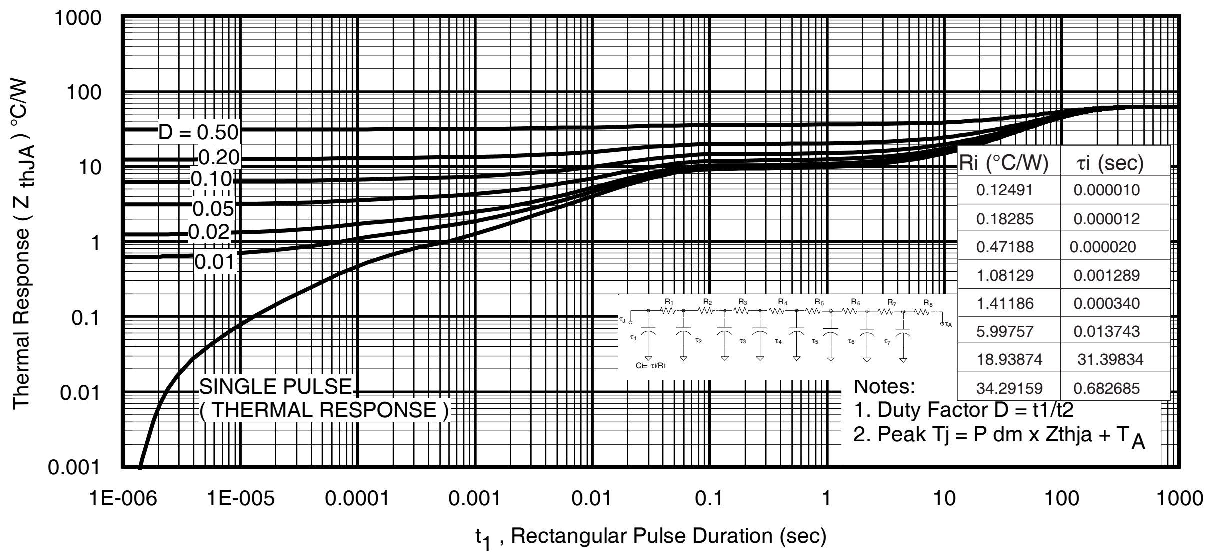


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

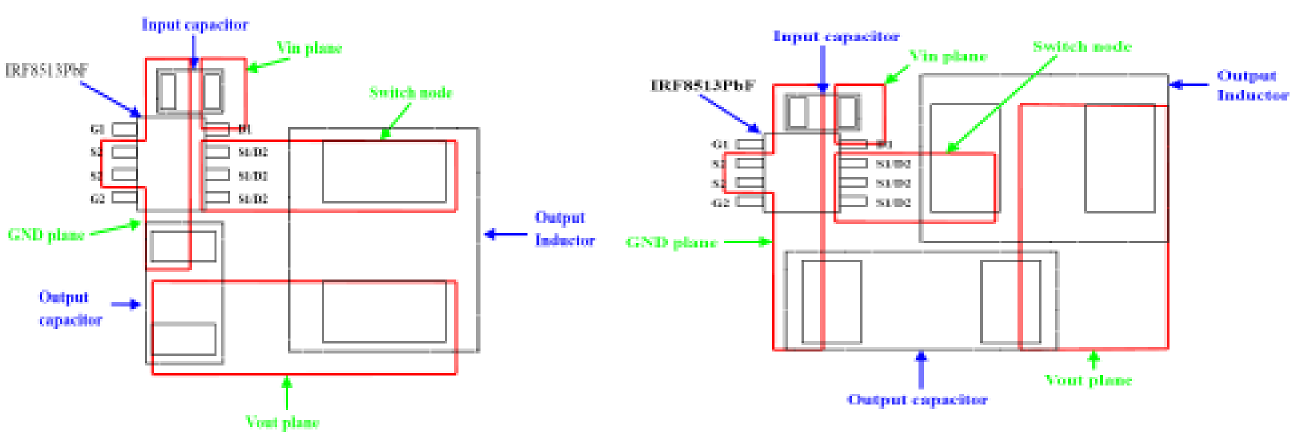
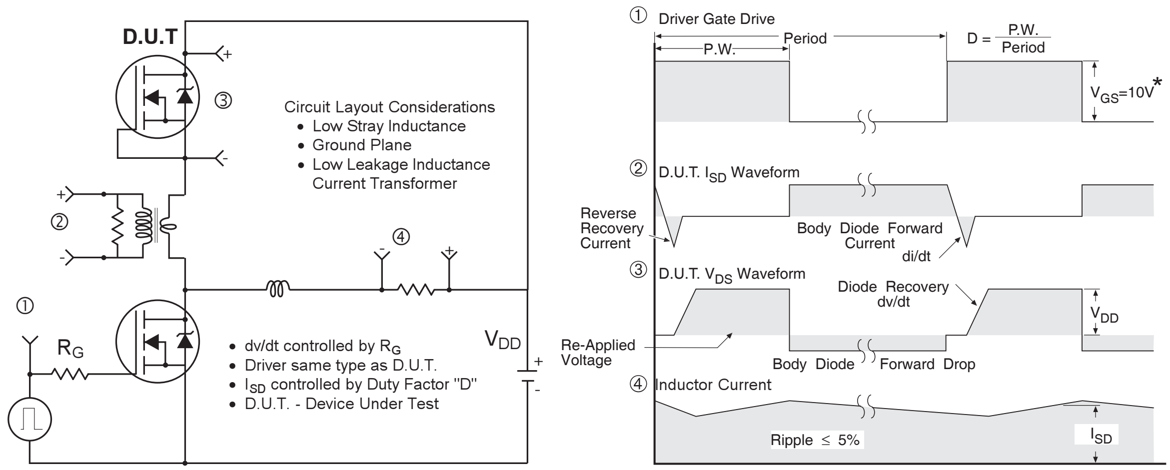


Fig 27. Layout Diagram



* V_{GS} = 5V for Logic Level Devices

Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

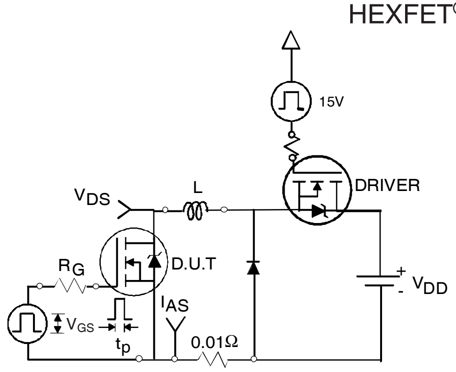


Fig 29a. Unclamped Inductive Test Circuit

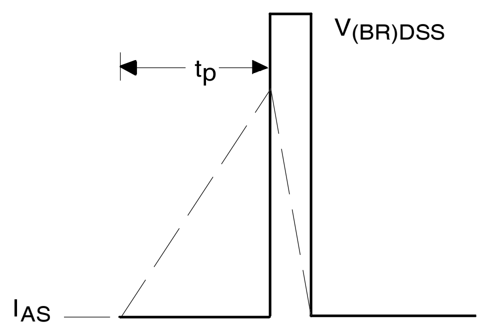


Fig 29b. Unclamped Inductive Waveforms

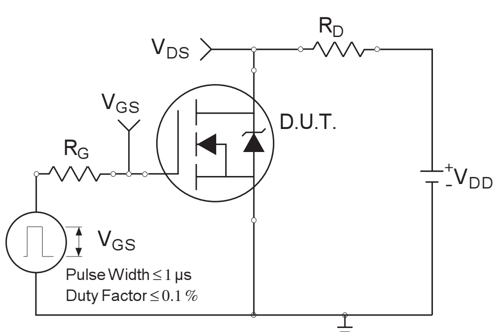


Fig 30a. Switching Time Test Circuit

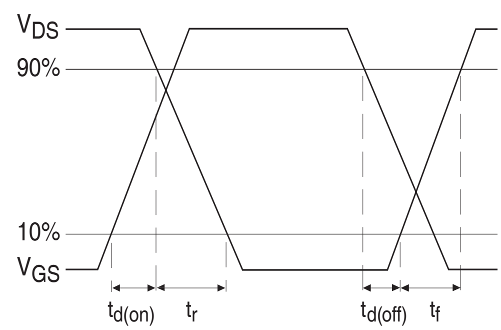


Fig 30b. Switching Time Waveforms

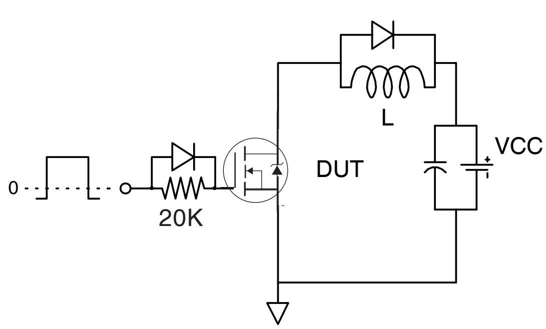


Fig 31a. Gate Charge Test Circuit

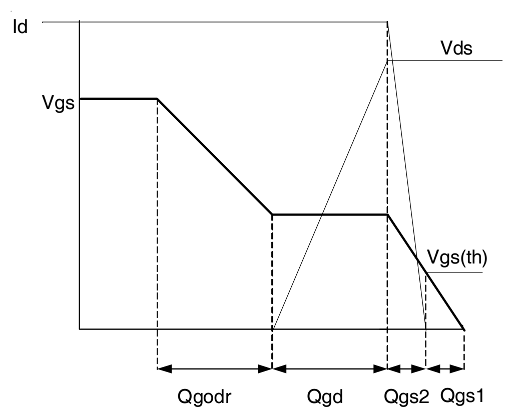
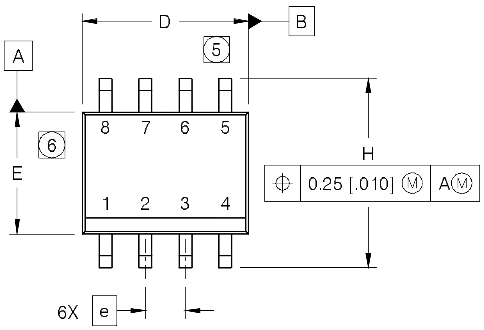


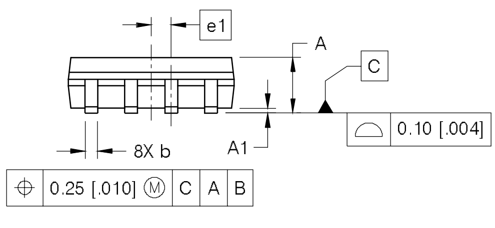
Fig 31b. Gate Charge Waveform

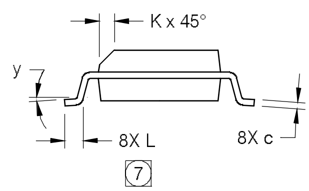
SO-8 Package Outline(Mosfet & Fetky)

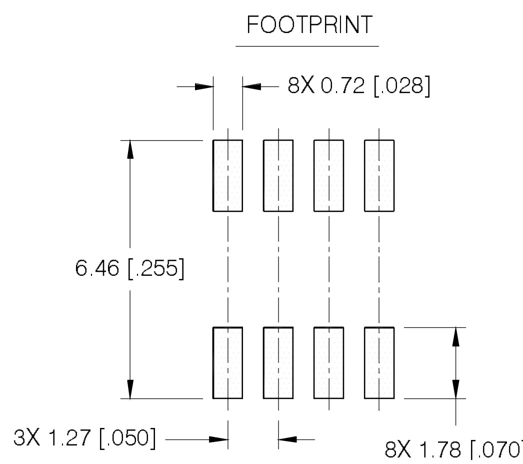
Dimensions are shown in milimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°







NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

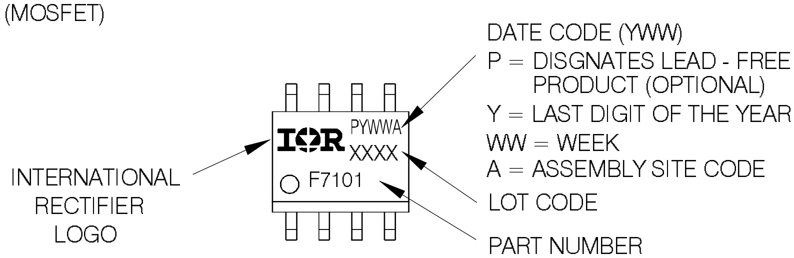
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

SO-8 Part Marking Information

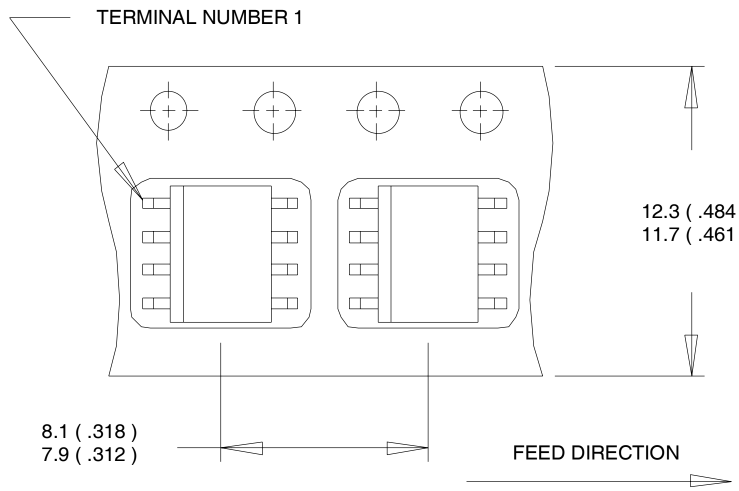
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



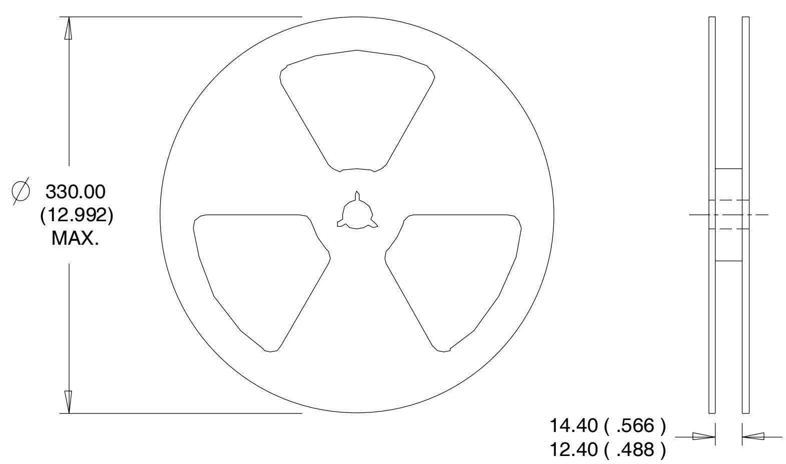
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

SO-8 Tape and Reel

Dimensions are shown in milimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF8513PbF	SO-8	Tube/Bulk	95	
IRF8513TRPbF	SO-8	Tape and Reel	4000	

Qualification Information†

Qualification level	Consumer †† (per JEDEC JESD47F††† guidelines)	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D†††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 2.4mH, R_G = 25Ω, I_{AS} = 6.4A (Q1) & L = 1.87mH, R_G = 25Ω, I_{AS} = 8.6A(Q2)

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.

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